



STL50NH3LL

N-CHANNEL 30 V - 0.011 Ω - 27 A PowerFLAT™(6x5) ULTRA LOW GATE CHARGE STripFET™ MOSFET

PRODUCT PREVIEW

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D (1)
STL50NH3LL	30 V	< 0.013 Ω	27 A (*)

- TYPICAL R_{DS(on)} = 0.011 Ω @ 10V
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- VERY LOW GATE CHARGE
- LOW THRESHOLD DEVICE

DESCRIPTION

This application specific MOSFET is the latest generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

APPLICATIONS

- CONTROL FET IN BUCK CONVERTER

Figure 1: Package

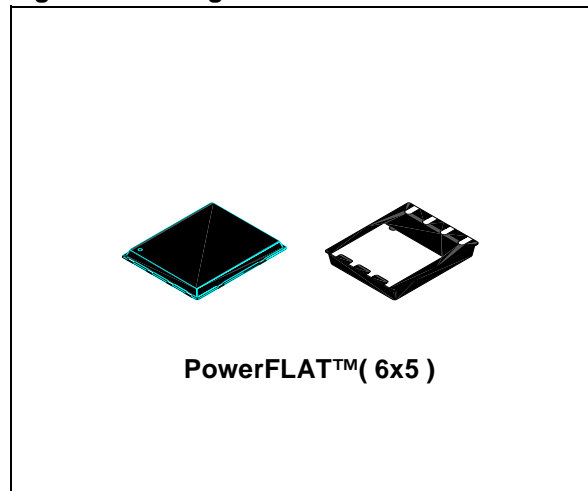


Figure 2: Internal Schematic Diagram

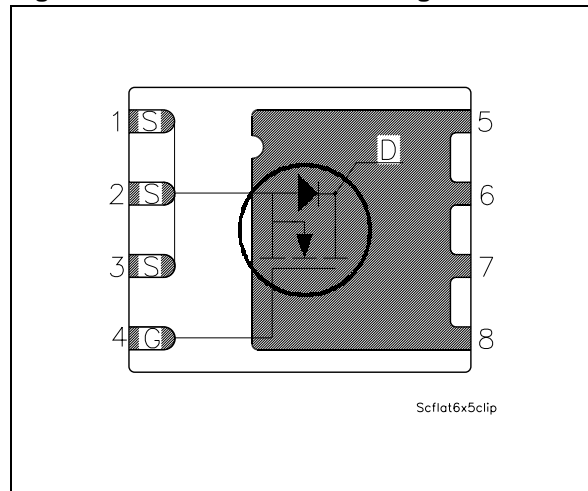


Table 2: Order Codes

Part Number	Marking	Package	Packaging
STL50NH3LL	L50NH3LL	PowerFLAT™ (6x5)	TAPE & REEL

Rev. 1

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate- source Voltage	± 16	V
I _D (1)	Drain Current (continuous) at T _C = 25°C	27	A
I _D (1)	Drain Current (continuous) at T _C = 100°C	27	A
I _{DM} (3)	Drain Current (pulsed)	108	A
I _D (2)	Drain Current (continuous) at T _C = 25°C	13	A
P _{TOT} (2)	Total Dissipation at T _C = 25°C (Steady State)	4	W
P _{TOT} (1)	Total Dissipation at T _C = 25°C	60	W
	Derating Factor	0.03	W/°C
T _{stg}	Storage Temperature	- 55 to 150	°C
T _j	Max. Operating Junction Temperature		

Table 4: Thermal Data

R _{thj-c}	Thermal Resistance Junction-Case (Drain)	2.08	°C/W
R _{thj-pcb} (2)	Thermal Operating Junction-pcb	31.2	°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)**Table 5: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			± 100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 6.5 A V _{GS} = 4.5 V, I _D = 6.5 A		0.011 0.012	0.013 0.015	Ω Ω

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (4)	Forward Transconductance	V _{DS} = 10V, I _D = 6.5A		TBD		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f= 1 MHz, V _{GS} = 0		965		pF
C _{oss}	Output Capacitance			285		pF
C _{rss}	Reverse Transfer Capacitance			38		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 6.5\text{ A}$		15		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 3)		32		ns
Q_g	Total Gate Charge	$V_{DD} = 15\text{ V}$, $I_D = 13\text{ A}$, $V_{GS} = 4.5\text{ V}$		9	12	nC
Q_{gs}	Gate-Source Charge	(see Figure 5)		3.7		nC
Q_{gd}	Gate-Drain Charge			3		nC

Table 8: Switching

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 6.5\text{ A}$,		18		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 3)		8.5		ns

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				13	A
I_{SDM}	Source-drain Current (pulsed)				52	A
$V_{SD(4)}$	Forward On Voltage	$I_{SD} = 13\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		24		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 20\text{ V}$, $T_j = 150^\circ\text{C}$		17.4		nC
I_{RRM}	Reverse Recovery Current	(see Figure 4)		1.45		A

(1) The value is rated according R_{thj-c} and is limited by wire bonding.

(2) When mounted on FR-4 board of 1 in^2 , 2oz Cu, $t < 10\text{ sec}$

(3) Pulse width limited by safe operating area.

(4) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Figure 3: Switching Times Test Circuit For Resistive Load

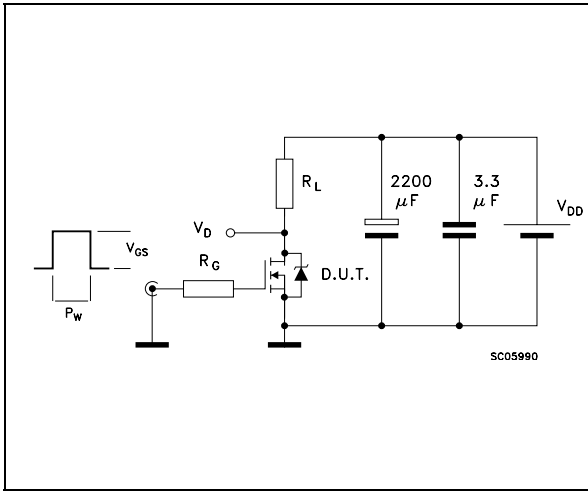


Figure 4: Test Circuit For Diode Recovery Times

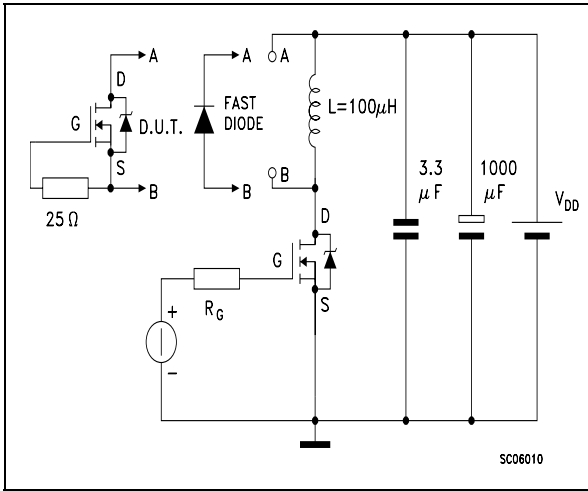
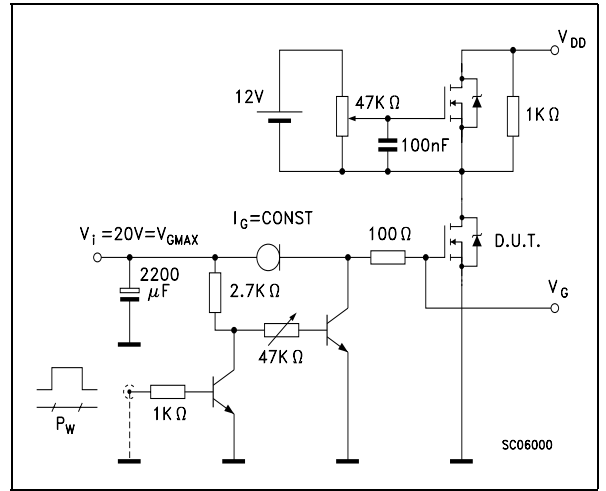


Figure 5: Gate Charge Test Circuit



PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80		0.93	0.031		0.036
A1		0.02			0.0007	0.0019
A3		0.20			0.007	
b	0.35		0.47	0.013		0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15		4.25	0.163		0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43		3.53	0.135		0.139
E4	2.85		2.68	0.101		0.105
e		1.27			0.050	
L	0.70		0.90	0.027		0.035

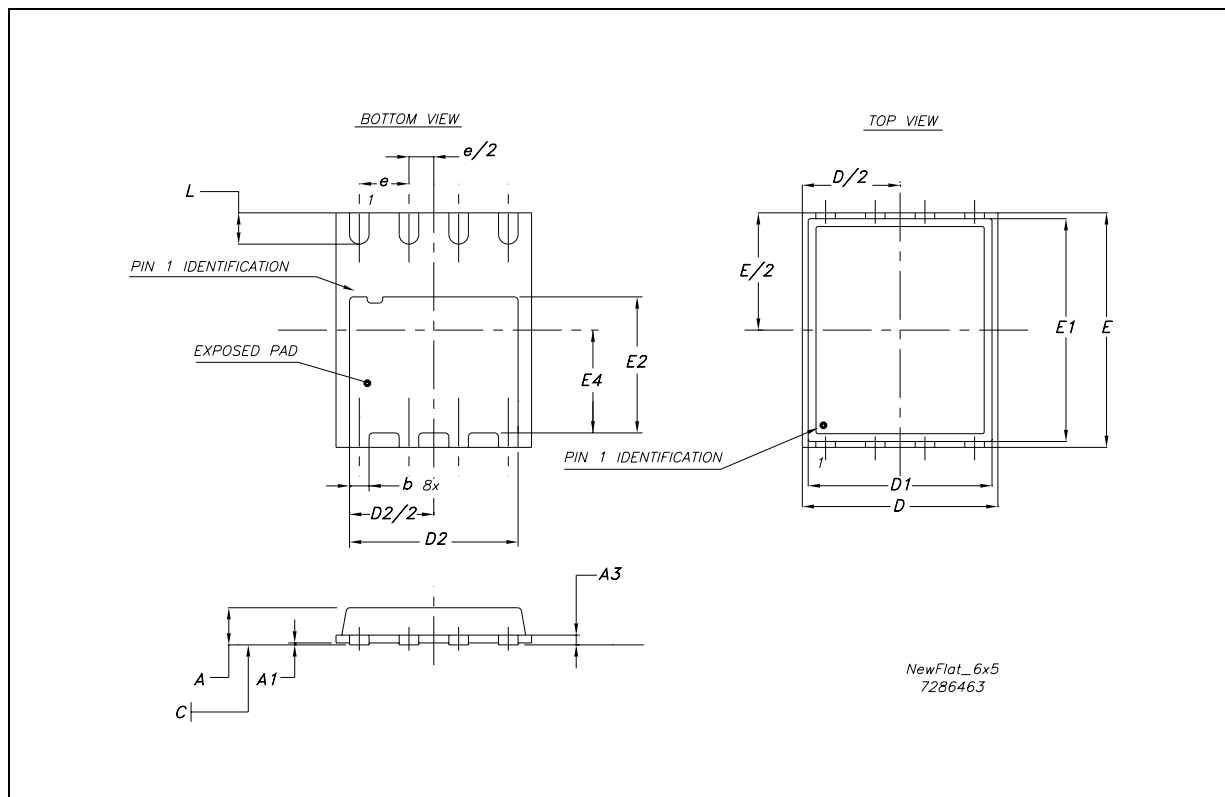


Table 10: Revision History

Date	Revision	Description of Changes
21-July-2004	1	First Release.

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