



STP9NK65Z STP9NK65ZFP

N-CHANNEL 650V - 1Ω - 6.4A TO-220/TO-220FP
Zener-Protected SuperMESH™ Power MOSFET

| TYPE | V _{DSS} | R _{DS(on)} | I _D | P _w |
|-------------|------------------|---------------------|----------------|----------------|
| STP9NK65Z | 650 V | < 1.2 Ω | 6.4 A | 125 W |
| STP9NK65ZFP | 650 V | < 1.2 Ω | 6.4 A | 30 W |

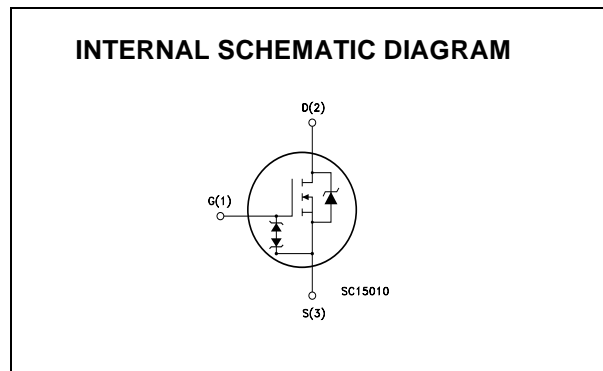
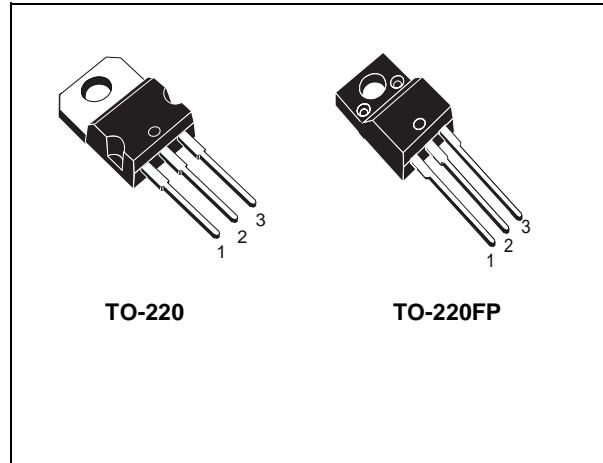
- TYPICAL R_{DS(on)} = 1 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING



ORDERING INFORMATION

| SALES TYPE | MARKING | PACKAGE | PACKAGING |
|-------------|-----------|----------|-----------|
| STP9NK65Z | P9NK65Z | TO-220 | TUBE |
| STP9NK65ZFP | P9NK65ZFP | TO-220FP | TUBE |

STP9NK65Z - STP9NK65ZFP

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | | Unit |
|------------------------------------|---|--------------------------|-------------|----------|
| | | STP9NK65Z | STP9NK65ZFP | |
| V _{DS} | Drain-source Voltage (V _{GS} = 0) | 650 | | V |
| V _{DGR} | Drain-gate Voltage (R _{GS} = 20 kΩ) | 650 | | V |
| V _{GS} | Gate- source Voltage | ± 30 | | V |
| I _D | Drain Current (continuous) at T _C = 25°C | 6.4 | 6.4 (*) | A |
| I _D | Drain Current (continuous) at T _C = 100°C | 4 | 4(*) | A |
| I _{DM} (•) | Drain Current (pulsed) | 25.6 | 25.6 (*) | A |
| P _{TOT} | Total Dissipation at T _C = 25°C | 125 | 30 | W |
| | Derating Factor | 1 | 0.24 | W/°C |
| V _{ESD(G-S)} | Gate source ESD(HBM-C=100pF, R=1.5KΩ) | 4000 | | V |
| dv/dt (1) | Peak Diode Recovery voltage slope | 4.5 | | V/ns |
| V _{ISO} | Insulation Withstand Voltage (DC) | - | 2500 | V |
| T _j T _{stg} | Operating Junction Temperature Storage Temperature | -55 to 150 -55 to 150 | | °C °C |

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 6.4 A, di/dt ≤ 200A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

THERMAL DATA

| | | TO-220 | TO-220FP | |
|-----------------------|--|--------|----------|------|
| R _{thj-case} | Thermal Resistance Junction-case Max | 1 | 4.2 | °C/W |
| R _{thj-amb} | Thermal Resistance Junction-ambient Max | 62.5 | | °C/W |
| T _I | Maximum Lead Temperature For Soldering Purpose | 300 | | °C |

AVALANCHE CHARACTERISTICS

| Symbol | Parameter | Max Value | Unit |
|-----------------|--|-----------|------|
| I _{AR} | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max) | 6.4 | A |
| E _{AS} | Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V) | 200 | mJ |

GATE-SOURCE ZENER DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------|-------------------------------|--------------------------------------|------|------|------|------|
| BV _{GSO} | Gate-Source Breakdown Voltage | I _{gs} = ± 1mA (Open Drain) | 30 | | | V |

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (TCASE =25°C UNLESS OTHERWISE SPECIFIED)
ON/OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D = 1 \text{ mA}, V_{GS} = 0$ | 650 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current ($V_{GS} = 0$) | $V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125 \text{ °C}$ | | | 1 50 | μA μA |
| I_{GSS} | Gate-body Leakage Current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 100\mu\text{A}$ | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS} = 10\text{V}, I_D = 3.2 \text{ A}$ | | 1 | 1.2 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------------|---|--|------|-------------------|------|----------------|
| $g_{fs} (1)$ | Forward Transconductance | $V_{DS} = 15 \text{ V}, I_D = 3.2 \text{ A}$ | | 6 | | S |
| C_{iss} C_{oss} C_{rss} | Input Capacitance Output Capacitance Reverse Transfer Capacitance | $V_{DS} = 25\text{V}, f = 1 \text{ MHz}, V_{GS} = 0$ | | 1145 130 28 | | pF pF pF |
| $C_{oss \text{ eq.}} (3)$ | Equivalent Output Capacitance | $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 400\text{V}$ | | 55 | | pF |

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|--|---|------|-----------------|------|----------------|
| $t_{d(on)}$ t_r | Turn-on Delay Time Rise Time | $V_{DD} = 325 \text{ V}, I_D = 3.2 \text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3) | | 20 12 | | ns ns |
| Q_g Q_{gs} Q_{gd} | Total Gate Charge Gate-Source Charge Gate-Drain Charge | $V_{DD} = 520 \text{ V}, I_D = 6.4 \text{ A},$ $V_{GS} = 10 \text{ V}$ | | 41 7.5 22 | 57 | nC nC nC |

SWITCHING OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------------------|---|--|------|----------------|------|----------------|
| $t_{d(off)}$ t_f | Turn-off Delay Time Fall Time | $V_{DD} = 325 \text{ V}, I_D = 3.2 \text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3) | | 45 15 | | ns ns |
| $t_r(V_{off})$ t_f t_c | Off-voltage Rise Time Fall Time Cross-over Time | $V_{DD} = 520 \text{ V}, I_D = 6.4 \text{ A},$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (Inductive Load see, Figure 5) | | 12 12 20 | | ns ns ns |

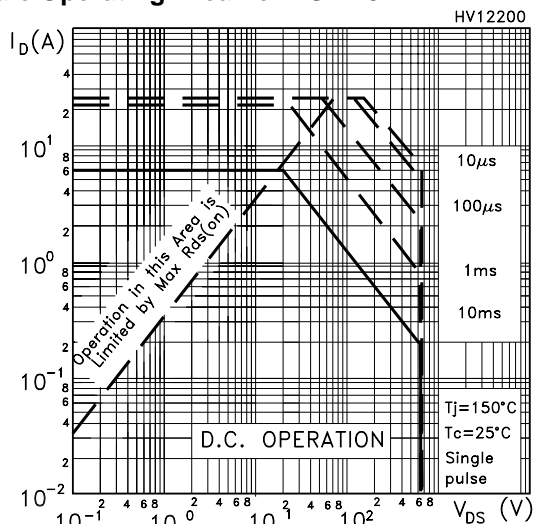
SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--|------|-------------------|-------------|---------------|
| I_{SD} $I_{SDM} (2)$ | Source-drain Current Source-drain Current (pulsed) | | | | 6.4 25.6 | A A |
| $V_{SD} (1)$ | Forward On Voltage | $I_{SD} = 6.4 \text{ A}, V_{GS} = 0$ | | | 1.6 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current | $I_{SD} = 6.4 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 50 \text{ V}, T_j = 150\text{°C}$ (see test circuit, Figure 5) | | 400 2600 13 | | ns nC A |

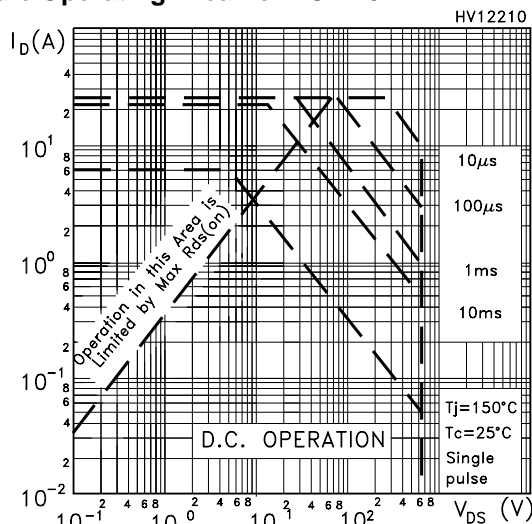
Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .



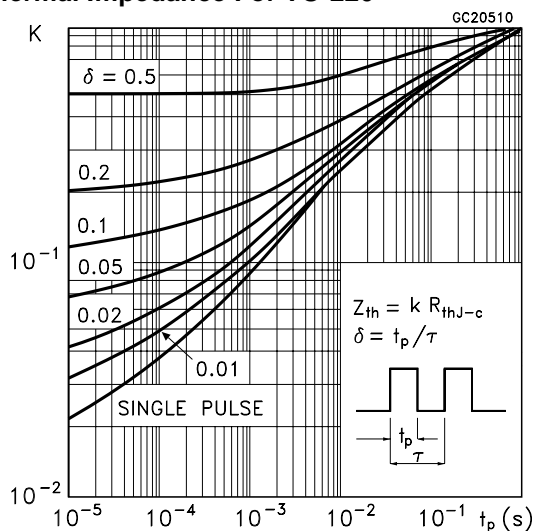
Safe Operating Area For TO-220



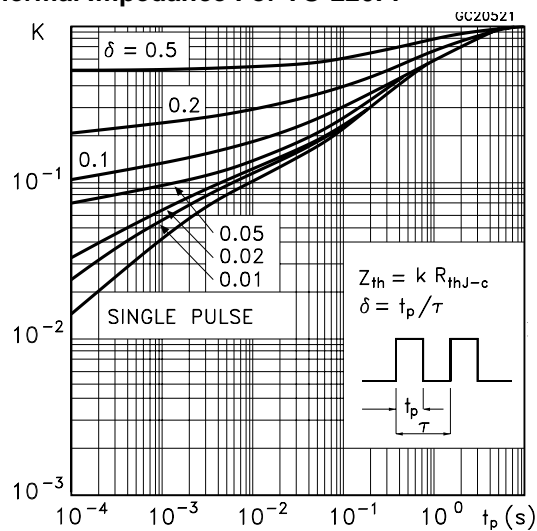
Safe Operating Area For TO-220FP



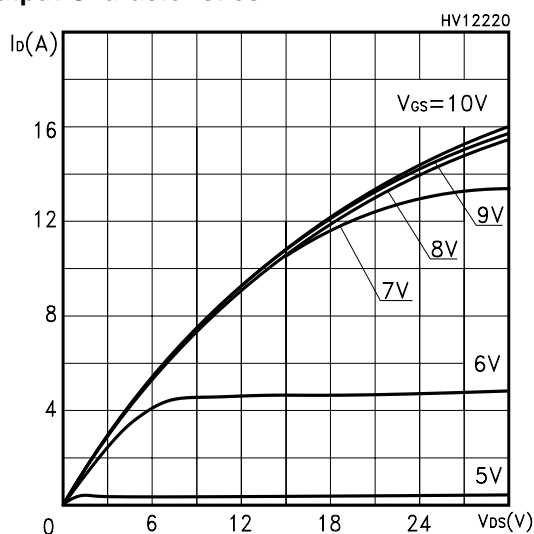
Thermal Impedance For TO-220



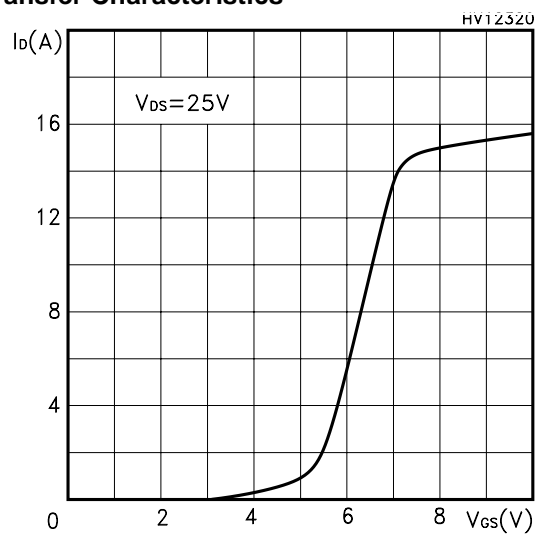
Thermal Impedance For TO-220FP



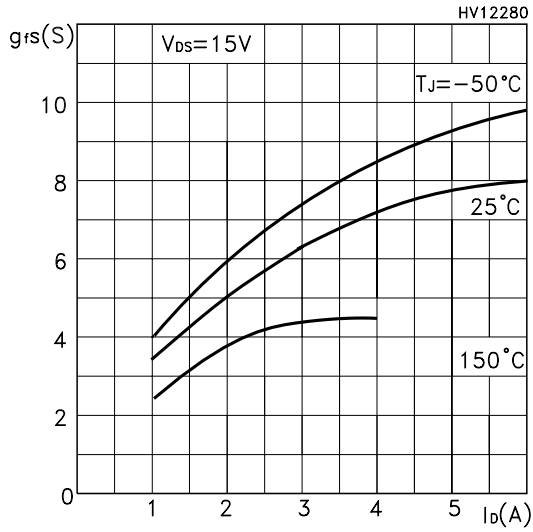
Output Characteristics



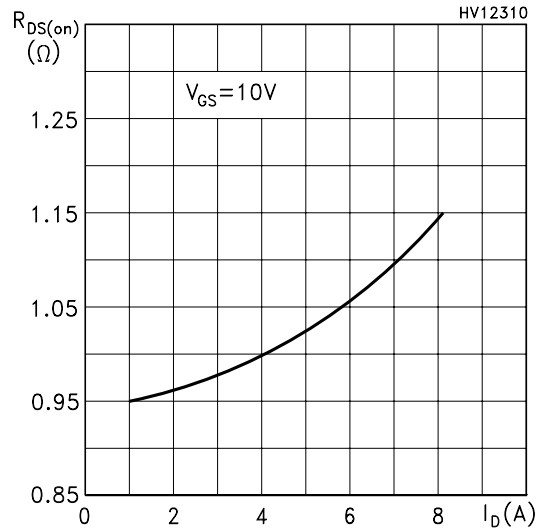
Transfer Characteristics



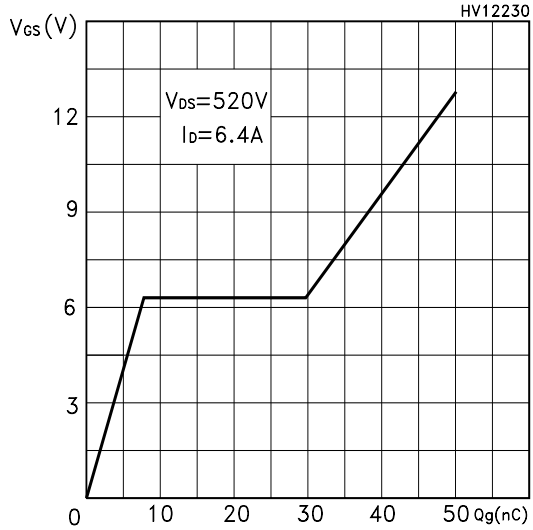
Transconductance



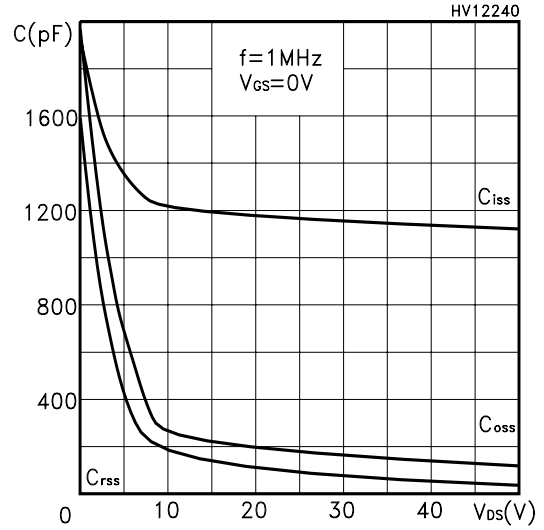
Static Drain-source On Resistance



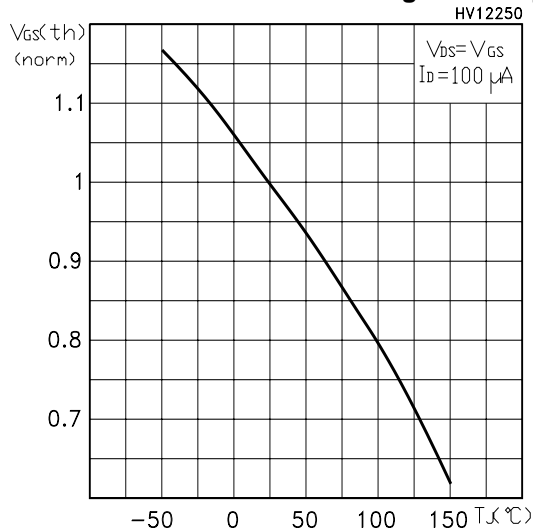
Gate Charge vs Gate-source Voltage



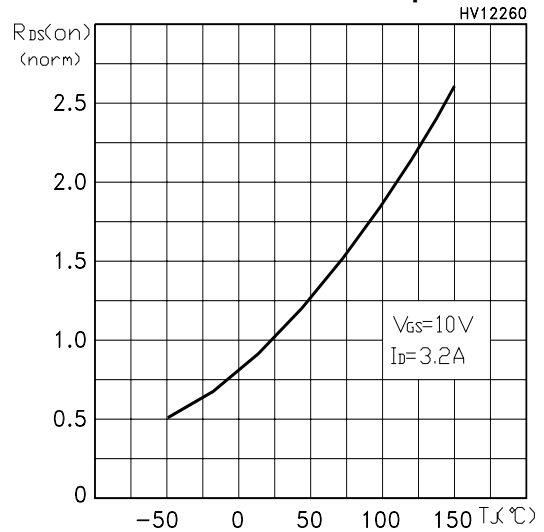
Capacitance Variations



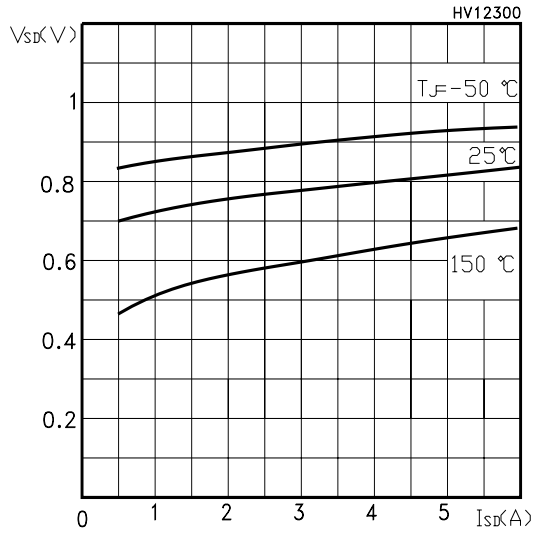
Normalized Gate Threshold Voltage vs Temp.



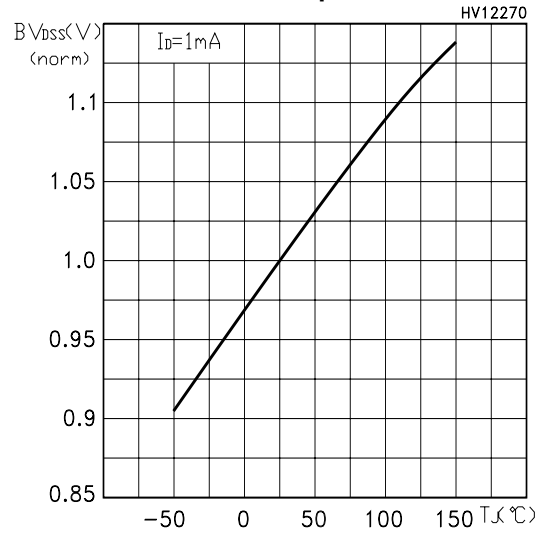
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature

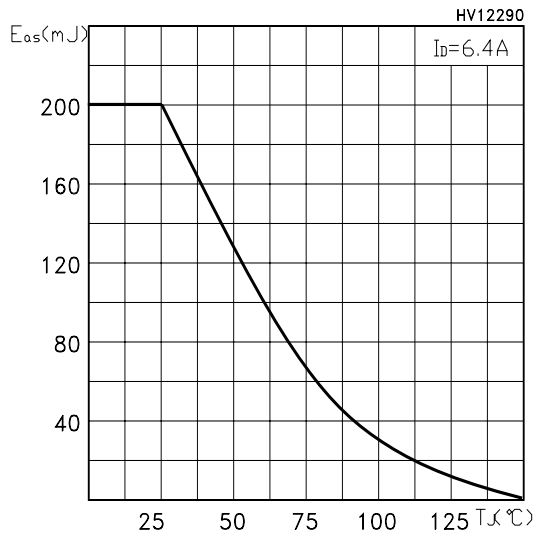


Fig. 1: Unclamped Inductive Load Test Circuit

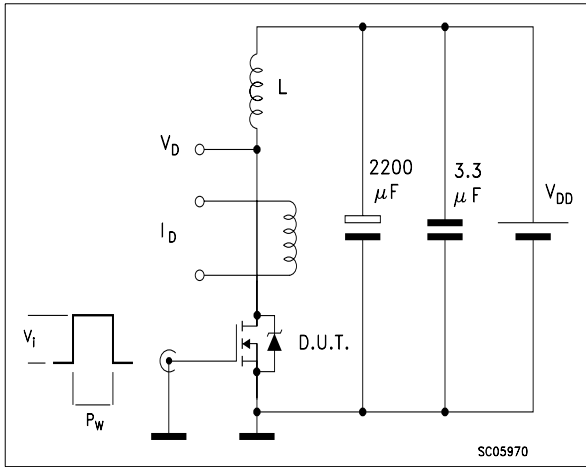


Fig. 2: Unclamped Inductive Waveform

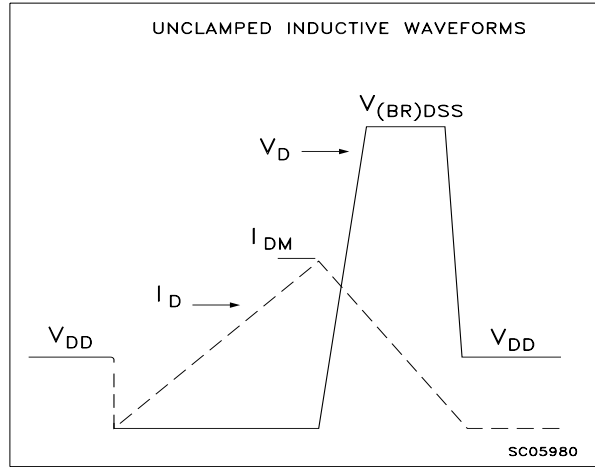


Fig. 3: Switching Times Test Circuit For Resistive Load

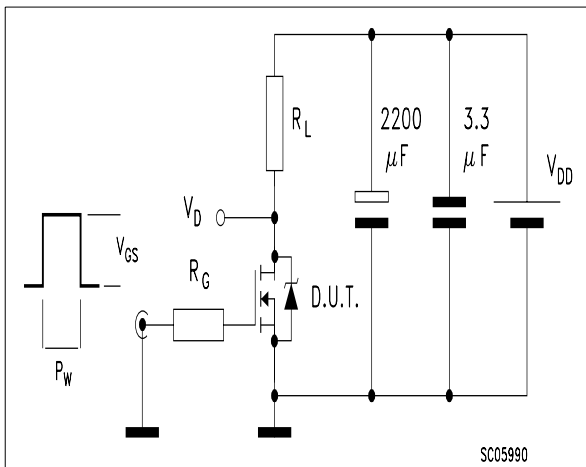


Fig. 4: Gate Charge test Circuit

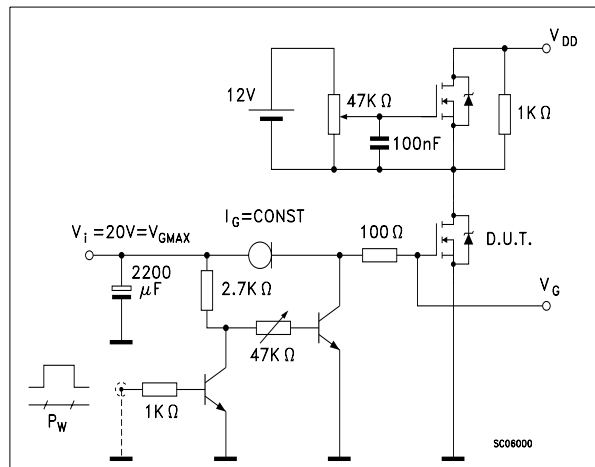
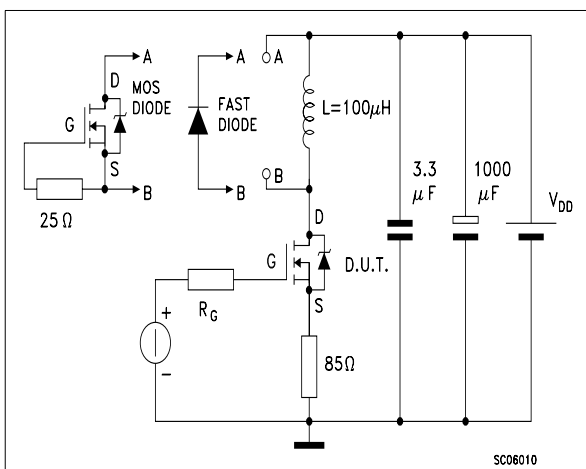
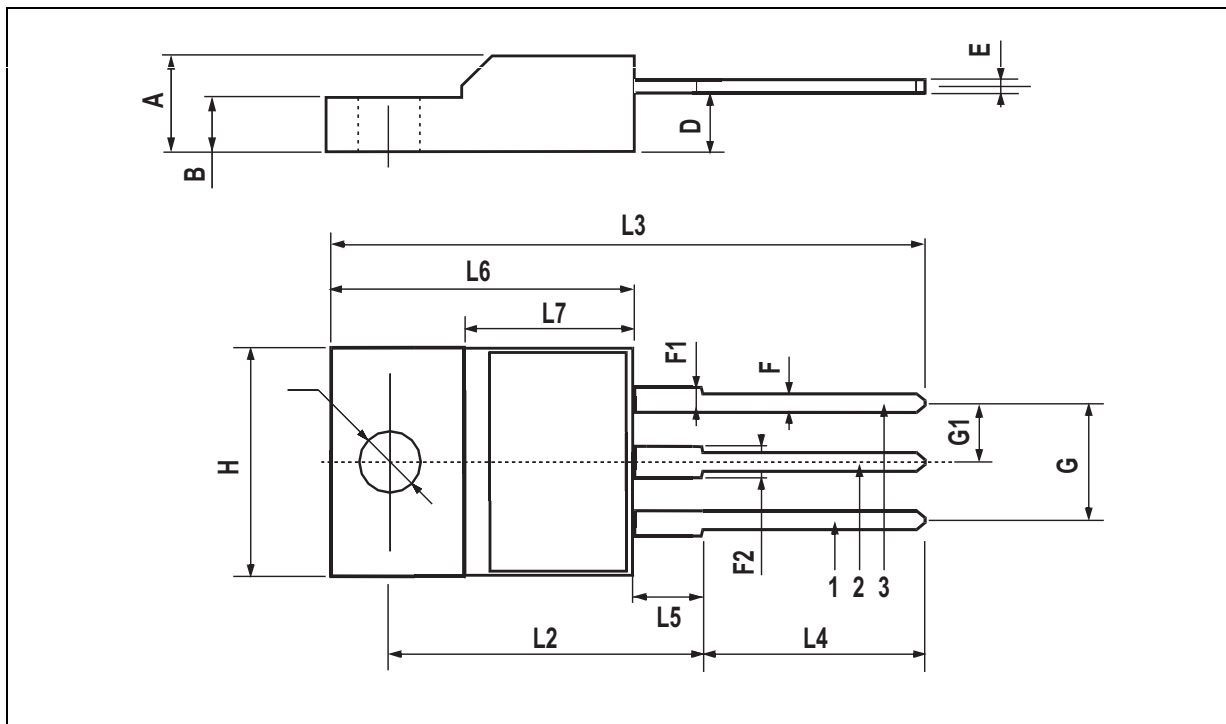


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220FP MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.4 | | 4.6 | 0.173 | | 0.181 |
| B | 2.5 | | 2.7 | 0.098 | | 0.106 |
| D | 2.5 | | 2.75 | 0.098 | | 0.108 |
| E | 0.45 | | 0.7 | 0.017 | | 0.027 |
| F | 0.75 | | 1 | 0.030 | | 0.039 |
| F1 | 1.15 | | 1.5 | 0.045 | | 0.067 |
| F2 | 1.15 | | 1.5 | 0.045 | | 0.067 |
| G | 4.95 | | 5.2 | 0.195 | | 0.204 |
| G1 | 2.4 | | 2.7 | 0.094 | | 0.106 |
| H | 10 | | 10.4 | 0.393 | | 0.409 |
| L2 | | 16 | | | 0.630 | |
| L3 | 28.6 | | 30.6 | 1.126 | | 1.204 |
| L4 | 9.8 | | 10.6 | .0385 | | 0.417 |
| L5 | 2.9 | | 3.6 | 0.114 | | 0.141 |
| L6 | 15.9 | | 16.4 | 0.626 | | 0.645 |
| L7 | 9 | | 9.3 | 0.354 | | 0.366 |
| Ø | 3 | | 3.2 | 0.118 | | 0.126 |



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>