



STS7DNF30L

DUAL N-CHANNEL 30V - 0.018 Ω - 7A SO-8 STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS7DNF30L	30 V	<0.022 Ω	7 A

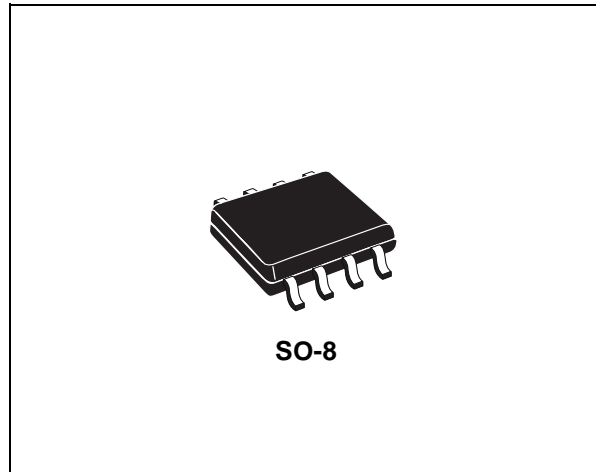
- TYPICAL R_{DS(on)} = 0.018Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

DESCRIPTION

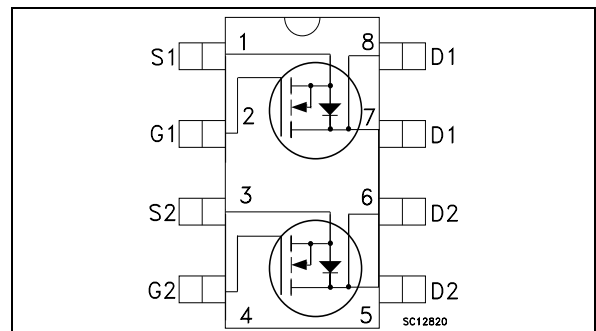
This application specific Power MOSFET is the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR DRIVE
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN PORTABLE/DESKTOP PC_S



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate- source Voltage	± 16	V
I _D	Drain Current (continuous) at T _C = 25°C Single Operation	7	A
	Drain Current (continuous) at T _C = 100°C Single Operation	4	
I _{DM} (●)	Drain Current (pulsed)	28	A
P _{tot}	Total Dissipation at T _C = 25°C Dual operating	2	W
	Total Dissipation at T _C = 25°C Single operating	1.6	

(●) Pulse width limited by safe operating area.

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THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-ambient	Single Operating	78	°C/W
		Dual Operating	62.5	°C/W
T _j	Maximum Operating Junction Temperature		150	°C
T _{stg}	Storage Temperature		-65 to 150	°C

(*) When mounted on FR-4 board with 0.5 in² pad of Cu.

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1	1.6	2.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 3.5 A V _{GS} = 4.5 V I _D = 3.5 A		0.018 0.021	0.022 0.026	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} I _D = 3.5 A		10		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1050		pF
C _{oss}	Output Capacitance			250		pF
C _{rss}	Reverse Transfer Capacitance			85		pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 3.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)		22 60		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 24\text{ V}$ $I_D = 8\text{ A}$ $V_{GS} = 5\text{ V}$ (see test circuit, Figure 2)		17.5 4 7	23	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ $I_D = 3.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 1)		42 10		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{clamp} = 24\text{ V}$ $I_D = 7\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (Inductive Load, Figure 3)		11 12 25		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				8 32	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 7\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 7\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 3)		50 40 1.6		ns nC A

(*)Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(\bullet)Pulse width limited by safe operating area.

Fig. 1: Switching Times Test Circuits For Resistive Load

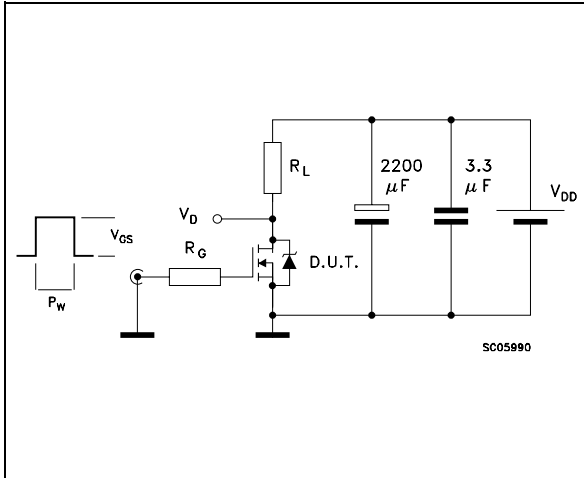


Fig. 2: Gate Charge test Circuit

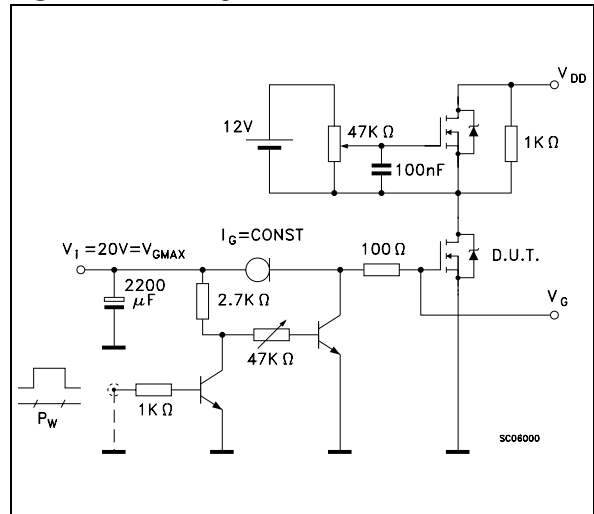
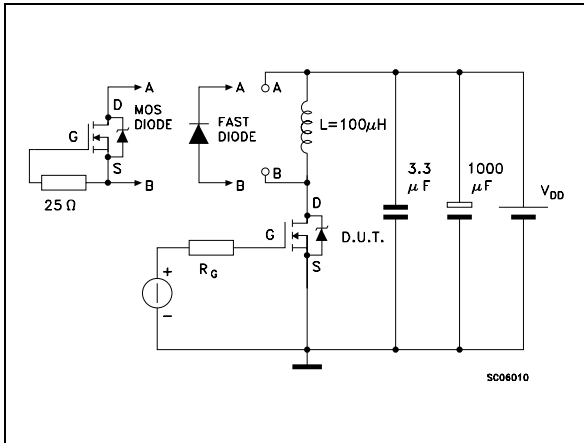
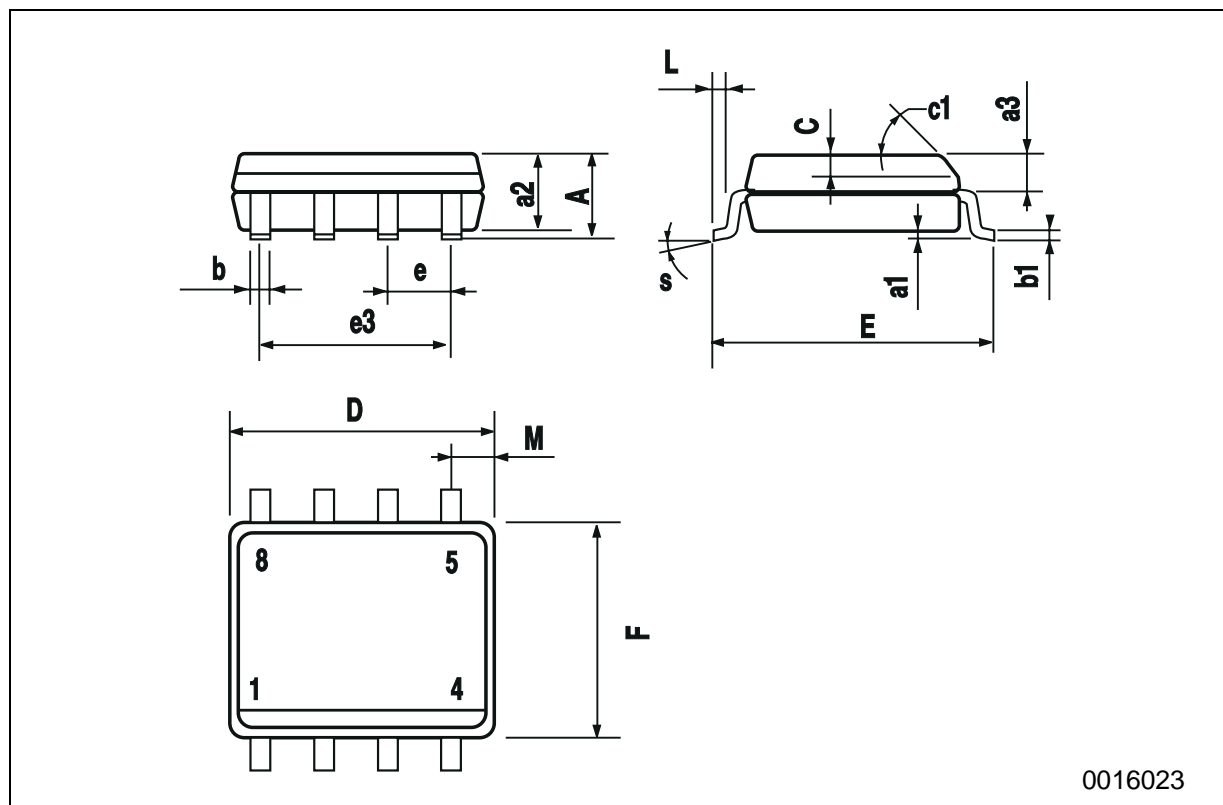


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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