



STSJ25NF3LL

N-CHANNEL 30V - 0.009Ω - 25A PowerSO-8™ LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STSJ25NF3LL	30 V	< 0.011 Ω	25 A

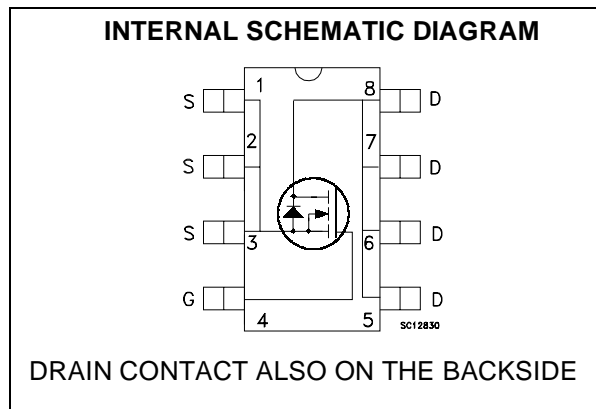
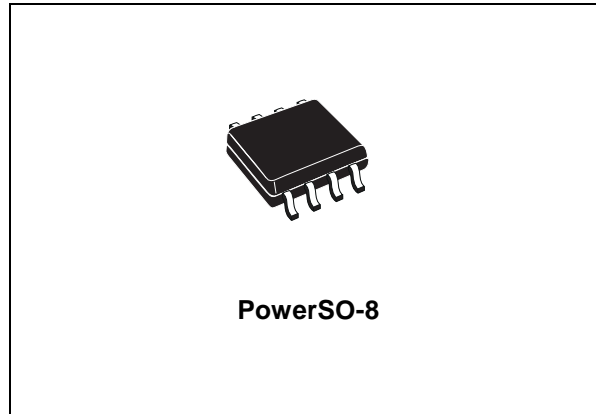
- IMPROVED JUNCTION-CASE THERMAL RESISTANCE
- TYPICAL R_{DS(on)} = 0.009Ω
- TYPICAL Q_g = 21 nC
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. This silicon, housed in thermally improved SO-8 package, exhibits optimal on-resistance versus gate charge trade-off plus lower R_{thj-c}.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PCs



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate- source Voltage	± 16	V
I _D	Drain Current (continuous) at T _C = 25°C (*)	25	A
	Drain Current (continuous) at T _A = 25°C (#)	12	A
	Drain Current (continuous) at T _C = 100°C	16	A
I _{DM} (●)	Drain Current (pulsed)	100	A
P _{TOT}	Total Dissipation at T _C = 25°C	70	W
	Total Dissipation at T _A = 25°C (#)	3	W

(●) Pulse width limited by safe operating area

(*) Value limited by wires bonding

STSJ25NF3LL

THERMAL DATA

Rthj-c	Thermal Resistance Junction-case Max	1.8	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max (#)	42	°C/W
T _j	Max. Operating Junction Temperature	150	°C
T _{stg}	Storage Temperature	- 55 to 150	°C

(#) When mounted on 1 inch² FR4 Board, 2oz of Cu, t ≤ 10 sec.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	30			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 16V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 12.5 A V _{GS} = 4.5 V, I _D = 12.5 A		0.009 0.011	0.011 0.013	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 5.5 A		20		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		1700		pF
C _{oss}	Output Capacitance			500		pF
C _{rss}	Reverse Transfer Capacitance			115		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 12.5\text{ A}$		47		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		60		ns
Q_g	Total Gate Charge	$V_{DD} = 15\text{ V}$, $I_D = 25\text{ A}$,		21	28	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 4.5\text{ V}$		10		nC
Q_{gd}	Gate-Drain Charge			8.4		nC

SWITCHING OFF

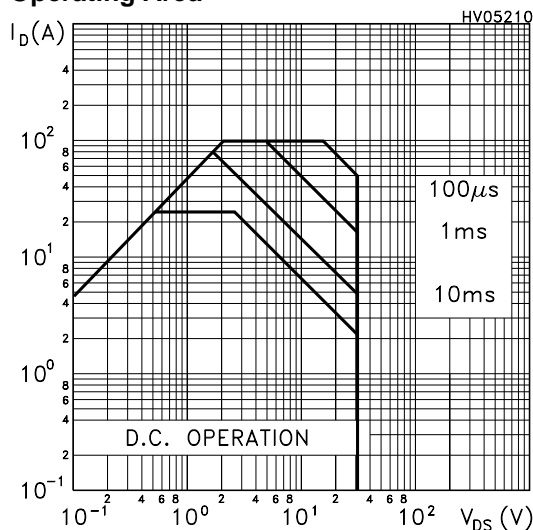
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 24\text{ V}$, $I_D = 12.5\text{ A}$,		34		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		24		ns

SOURCE DRAIN DIODE

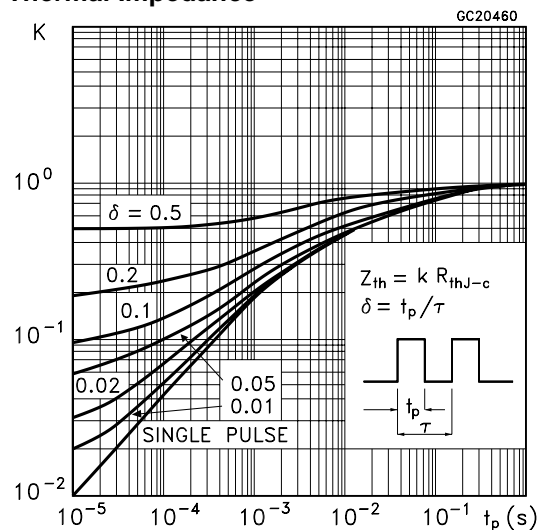
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				25	A
$I_{SDM(1)}$	Source-drain Current (pulsed)				100	A
$V_{SD(2)}$	Forward On Voltage	$I_{SD} = 25\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 25\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,		40		ns
Q_{rr}		$V_{DD} = 15\text{ V}$, $T_j = 150^\circ\text{C}$		52		nC
I_{RRM}		(see test circuit, Figure 5)		2.4		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.

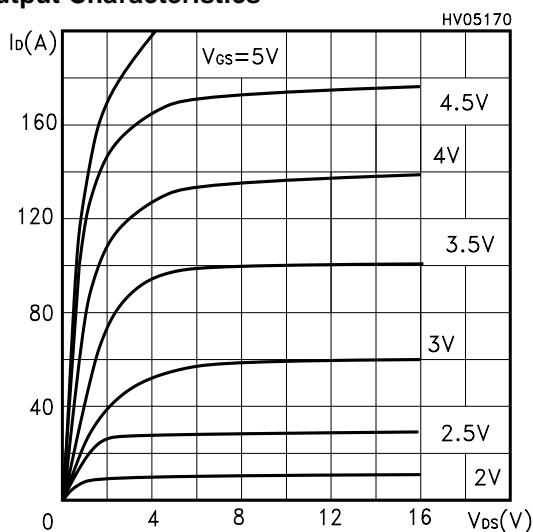
Safe Operating Area



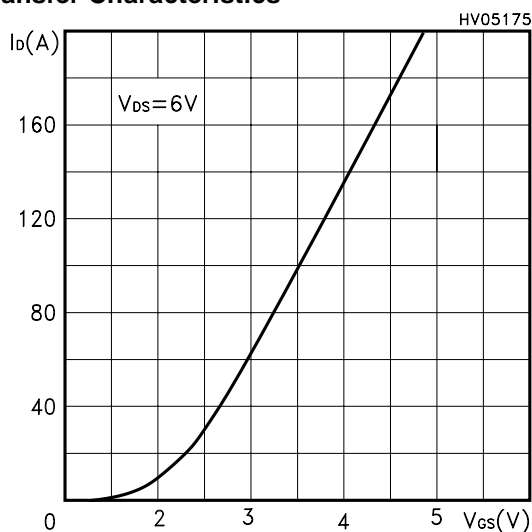
Thermal Impedance



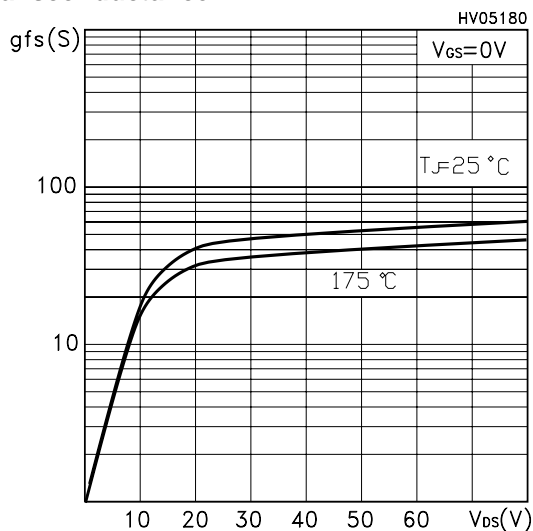
Output Characteristics



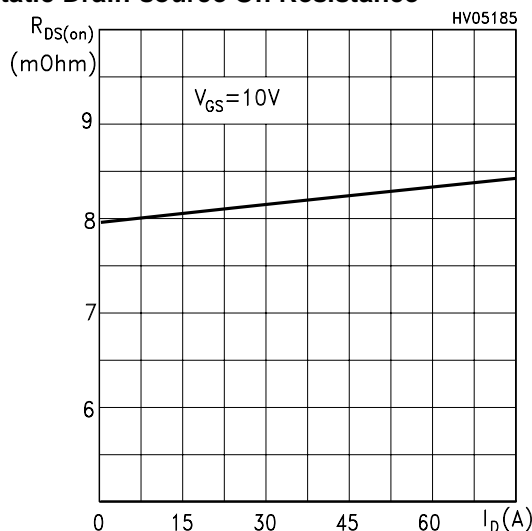
Transfer Characteristics



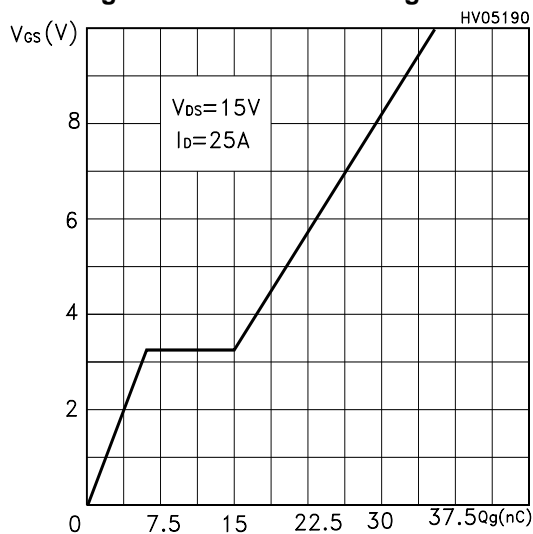
Transconductance



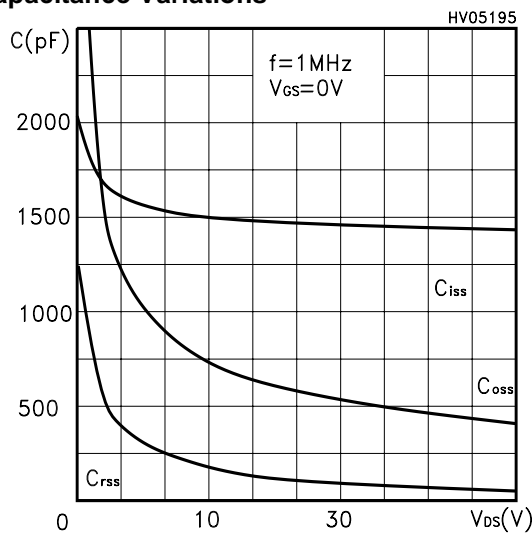
Static Drain-source On Resistance



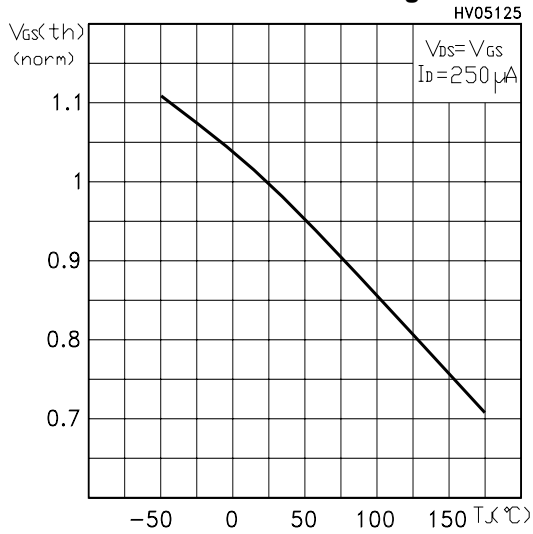
Gate Charge vs Gate-source Voltage



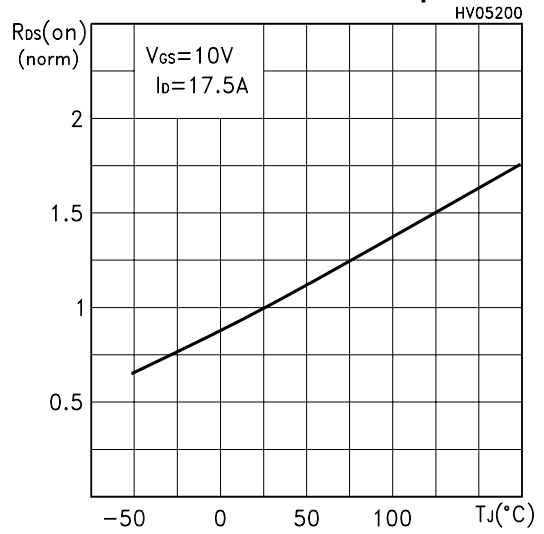
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

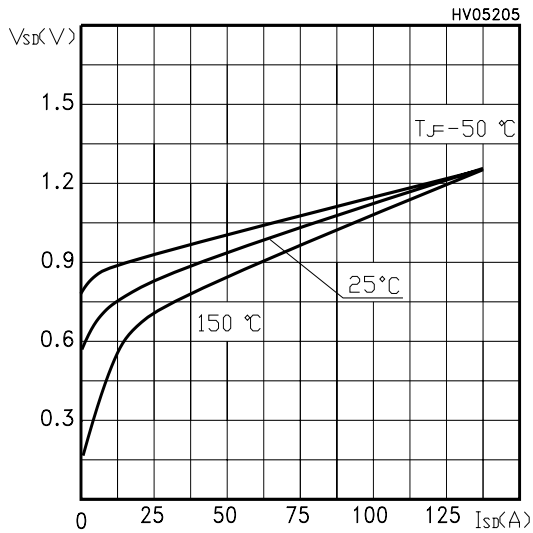


Fig. 1: Unclamped Inductive Load Test Circuit

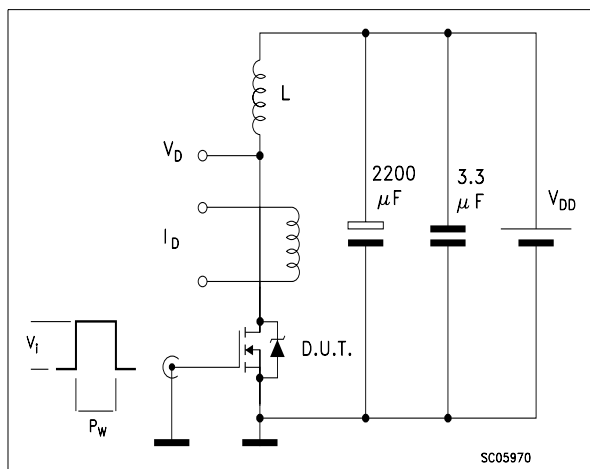


Fig. 2: Unclamped Inductive Waveform

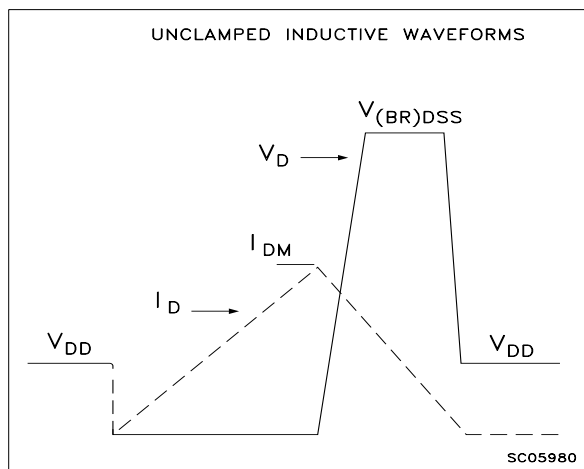


Fig. 3: Switching Times Test Circuit For Resistive Load

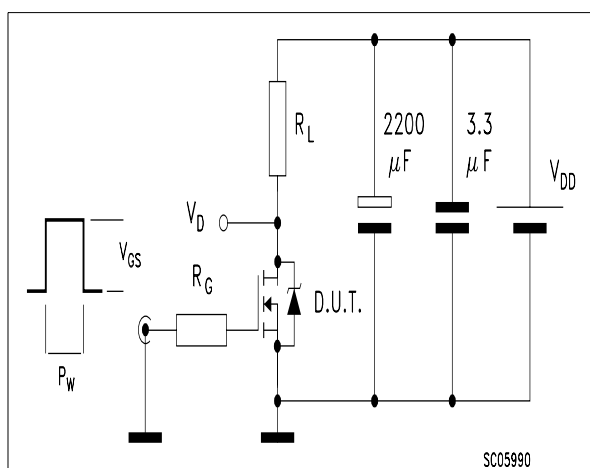


Fig. 4: Gate Charge test Circuit

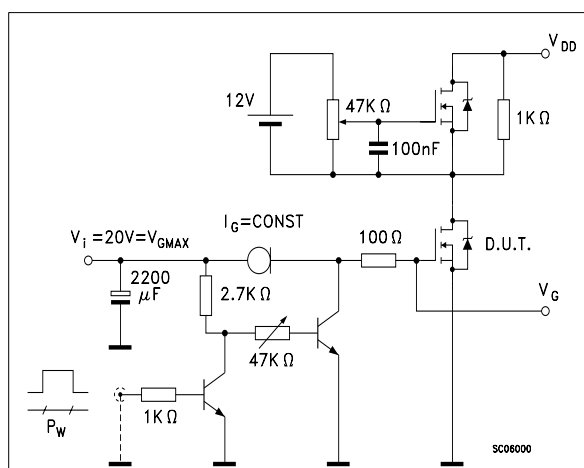
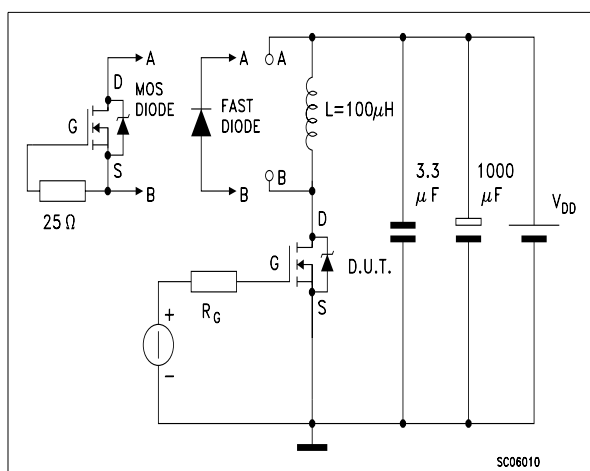
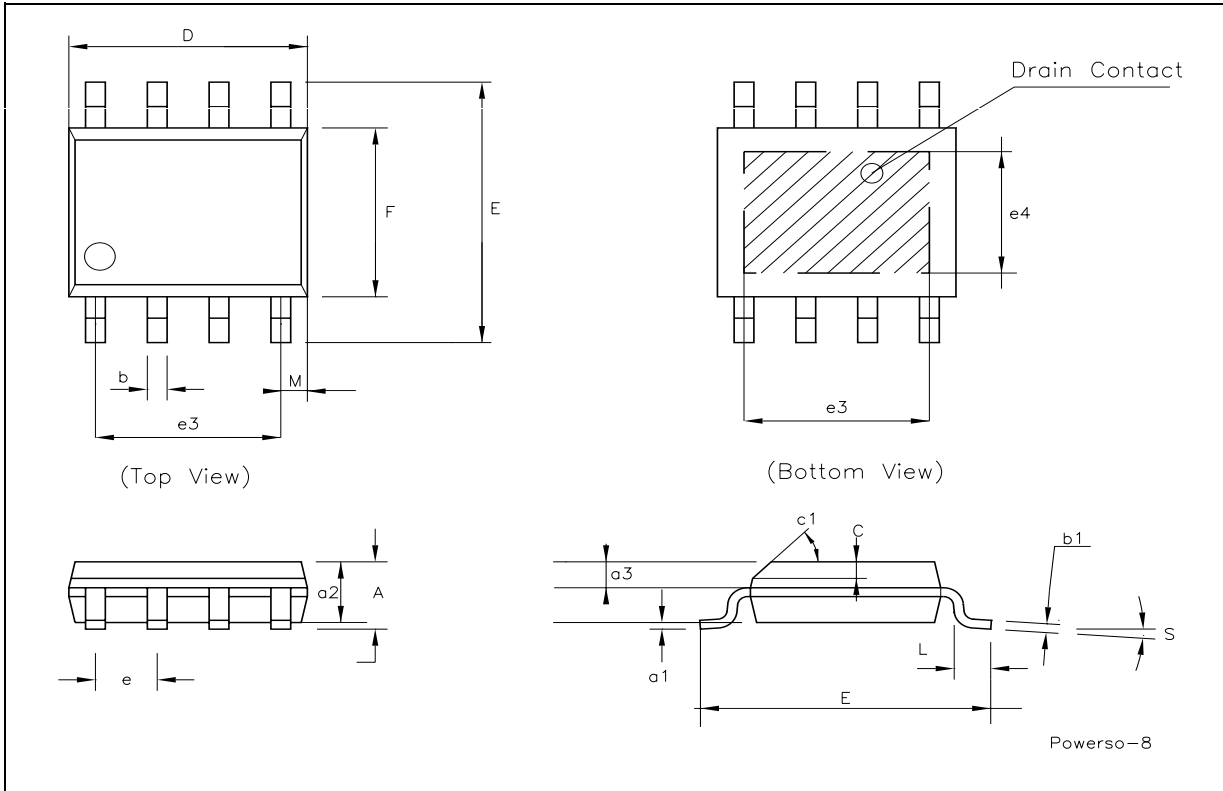


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerSO-8™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



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