



TS271C,I,M

CMOS PROGRAMMABLE LOW POWER SINGLE OPERATIONAL AMPLIFIER

- OFFSET NULL CAPABILITY (by external compensation)
- DYNAMIC CHARACTERISTICS
ADJUSTABLE I_{SET}
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- OUTPUT VOLTAGE CAN SWING TO GROUND
- VERY LARGE I_{SET} RANGE
- STABLE AND LOW OFFSET VOLTAGE
- THREE INPUT OFFSET VOLTAGE SELECTIONS

DESCRIPTION

The TS271 is a low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifier uses the ST silicon gate CMOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.

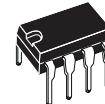
The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and supply current can be minimized according to the required speed. This device is specified for the following I_{SET} current values : 1.5 μ A, 25 μ A, 130 μ A.

This CMOS amplifier offers very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 3).

ORDER CODE

Part Number	Temperature Range	Package	
		N	D
TS271C/AC/BC	0°C, +70°C	•	•
TS271I/AI/BI	-40°C, +125°C	•	•
TS271M/AM/BM	-55°C, +125°C	•	•
Example : TS271ACN			

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

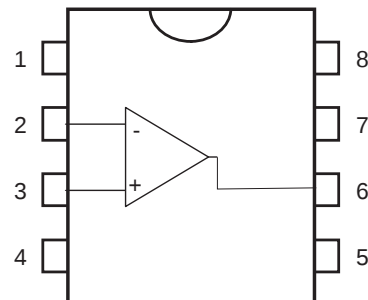


**N
DIP8**
(Plastic Package)



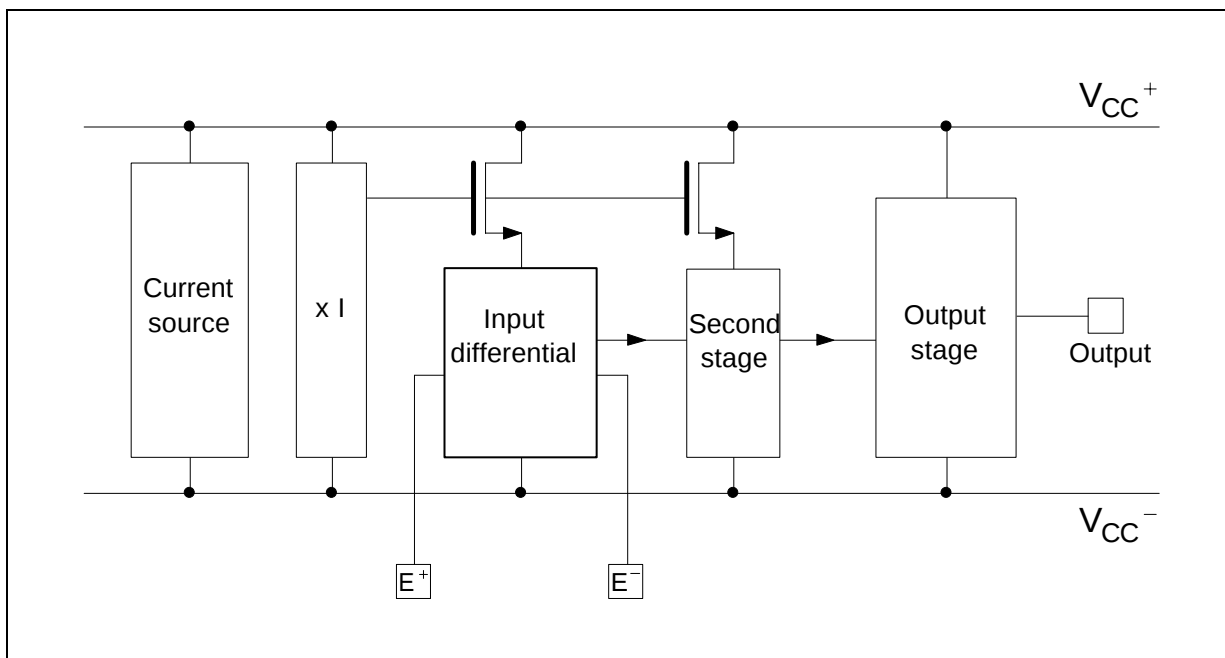
**D
SO8**
(Plastic Micropackage)

PIN CONNECTIONS (top view)



- 1 - Offset Null 1
- 2 - Inverting Input 1
- 3 - Non-inverting Input 1
- 4 - V_{CC}^-
- 5 - Offset Null 2
- 6 - Output
- 7 - V_{CC}^+
- 8 - I_{Set}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	TS271C/AC/BC	TS271I/AI/BI	TS271M/AM/BM	Unit
V_{CC}^+	Supply Voltage ¹⁾	18			V
V_{id}	Differential Input Voltage ²⁾	± 18			V
V_i	Input Voltage ³⁾	-0.3 to 18			V
I_o	Output Current for $V_{CC}^+ \geq 15V$	± 30			mA
I_{in}	Input Current	± 5			mA
T_{oper}	Operating Free-Air Temperature Range	0 to +70	-40 to +125	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. All values, except differential voltage are with respect to network ground terminal.

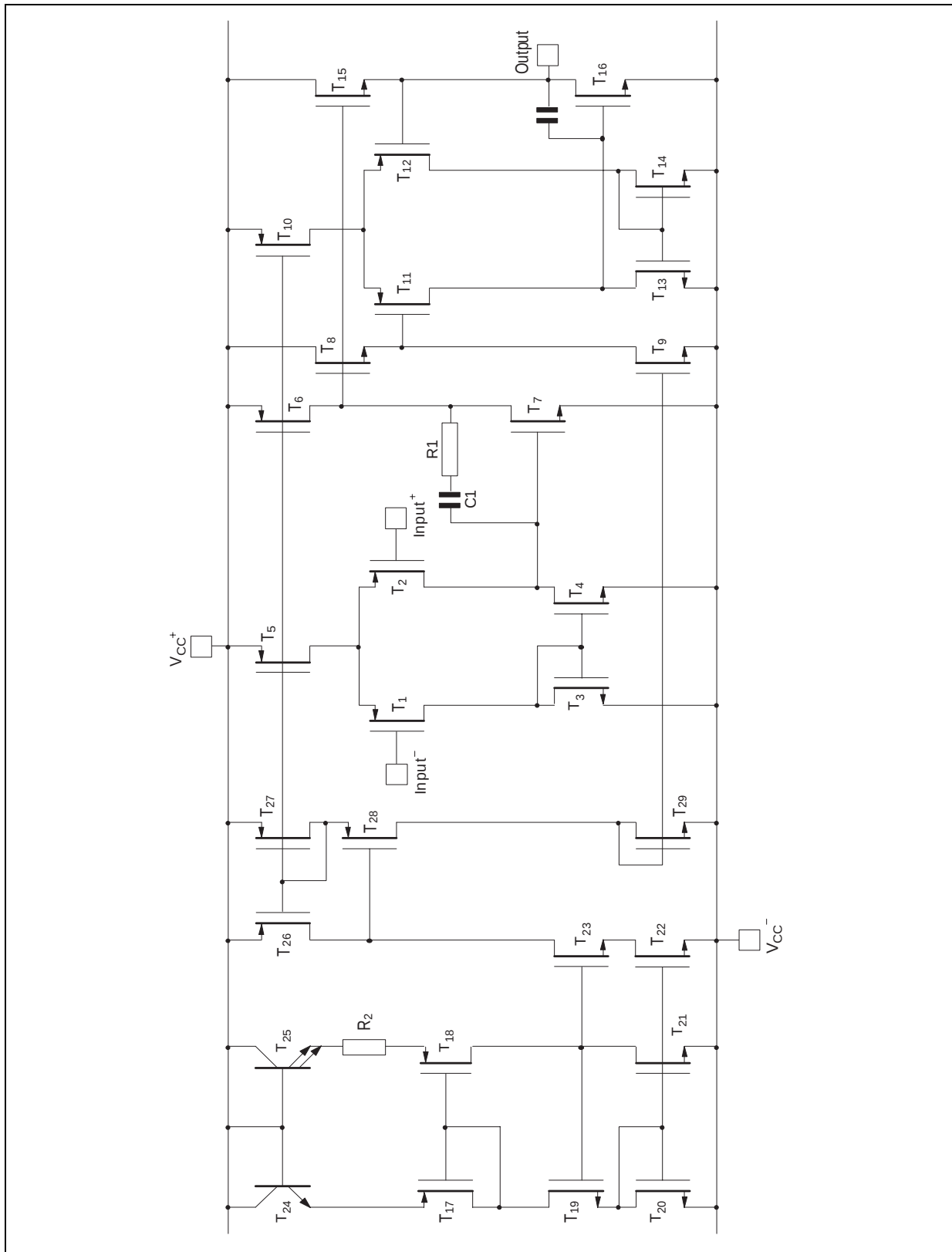
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

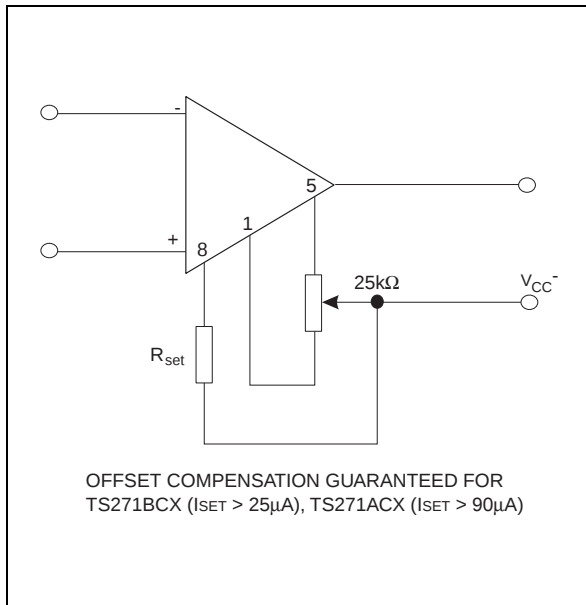
OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply Voltage	3 to 16	V
V_{icm}	Common Mode Input Voltage Range	0 to $V_{CC}^+ - 1.5$	V

SCHEMATIC DIAGRAM



OFFSET VOLTAGE NULL CIRCUIT



RESISTOR BIASING

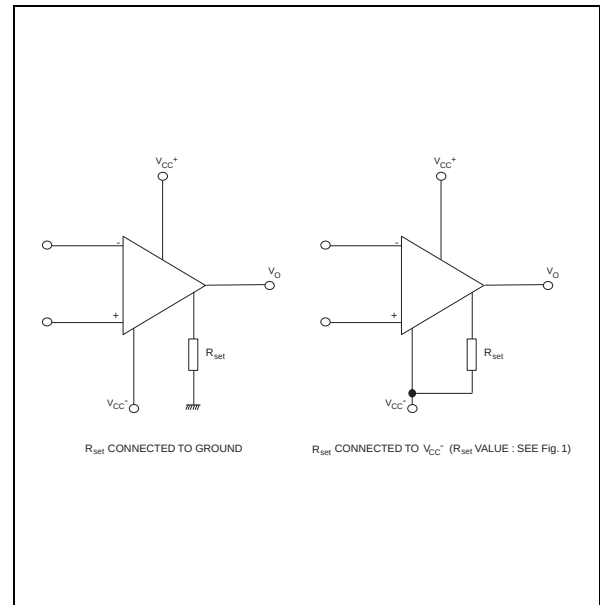
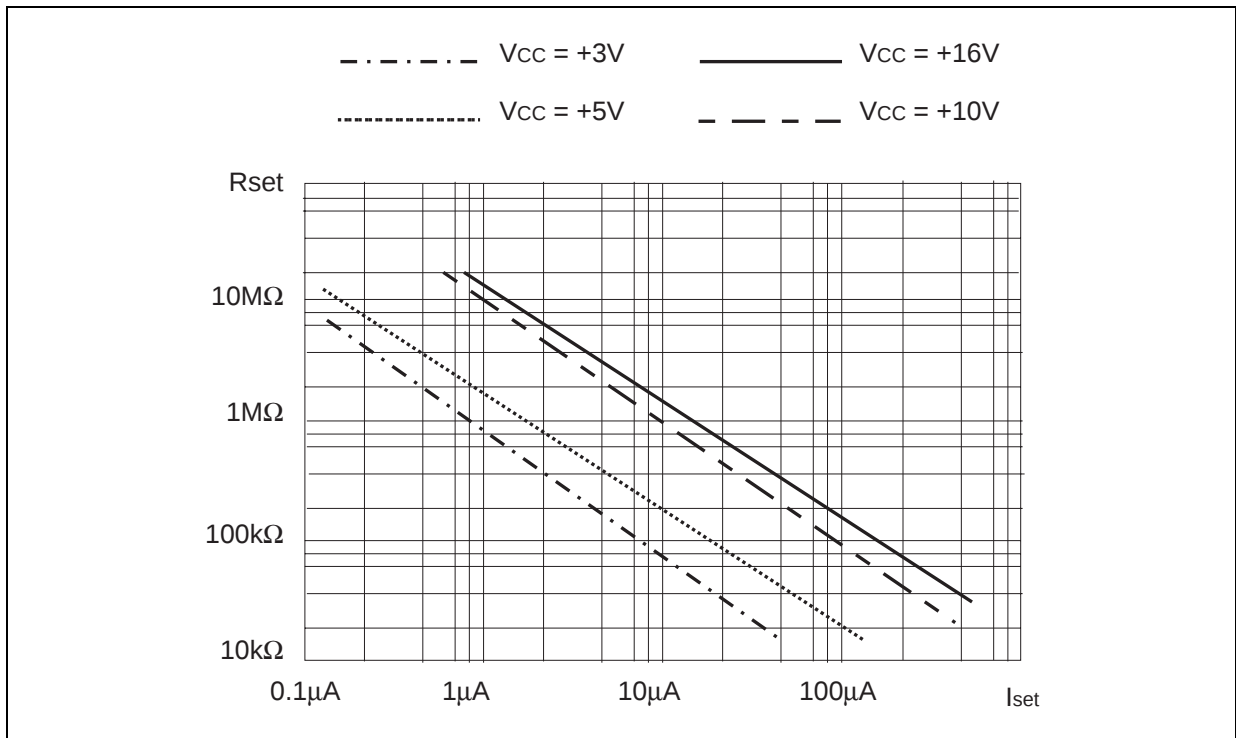


Figure 1 : R_{SET} Connected to V_{CC-}



ELECTRICAL CHARACTERISTICS for $I_{SET} = 1.5\mu A$ $V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = +25^\circ C$ (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_{ic} = 0V$ TS271C/I/M TS271AC/AI/AM TS271B/C/I/M $T_{min} \leq T_{amb} \leq T_{max}$ TS271C/I/M TS271AC/AI/AM TS271B/C/I/M		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		$\mu V/^\circ C$
I_{io}	Input Offset Current note 1) $V_{ic} = 5V$, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1	100		1	200	pA
I_{ib}	Input Bias Current - see note 1 $V_{ic} = 5V$, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1	150		1	300	pA
V_{OH}	High Level Output Voltage $V_{id} = 100mV$, $R_L = 1M\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	8.8 8.7	9		8.8 8.6	9		V
V_{OL}	Low Level Output Voltage $V_{id} = -100mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_{ic} = 5V$, $R_L = 1M\Omega$, $V_O = 1V$ to $6V$ $T_{min} \leq T_{amb} \leq T_{max}$	30 20	100		30 20	100		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$, $f_{in} = 100kHz$		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio $V_{ic} = 1V$ to $7.4V$, $V_O = 1.4V$	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_O = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		10	15 17		10	15 18	μA
I_o	Output Short Circuit Current $V_O = 0V$, $V_{id} = 100mV$		60			60		mA
I_{sink}	Output Sink Current $V_O = V_{CC}$, $V_{id} = -100mV$		45			45		mA
SR	Slew Rate at Unity Gain $R_L = 1M\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		0.04			0.04		V/ μs
ϕ_m	Phase Margin at Unity Gain $A_v = 40dB$, $R_L = 1M\Omega$ $C_L = 10pF$ $C_L = 100pF$		35 10			35 10		Degrees
K_{OV}	Overshoot Factor $A_v = 40dB$, $R_L = 1M\Omega$ $C_L = 10pF$ $C_L = 100pF$		40 70			40 70		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_s = 100\Omega$		30			30		$\frac{nV}{\sqrt{Hz}}$

1. Maximum values including unavoidable inaccuracies of the industrial test.

TYPICAL CHARACTERISTICS for $I_{SET} = 1.5\mu A$

Figure 2 : Supply Current versus Supply Voltage

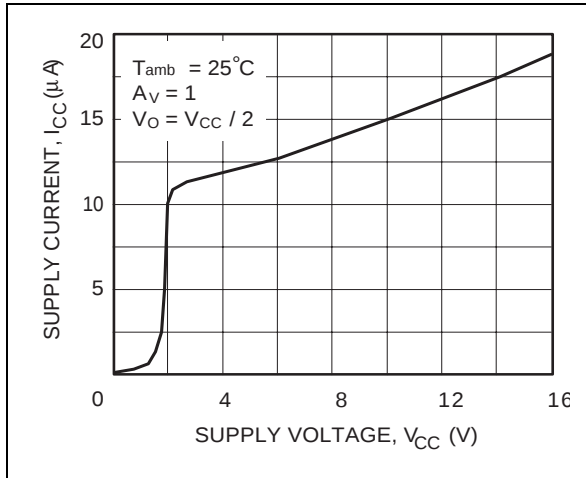


Figure 3 : Input Bias Current versus Free Air Temperature

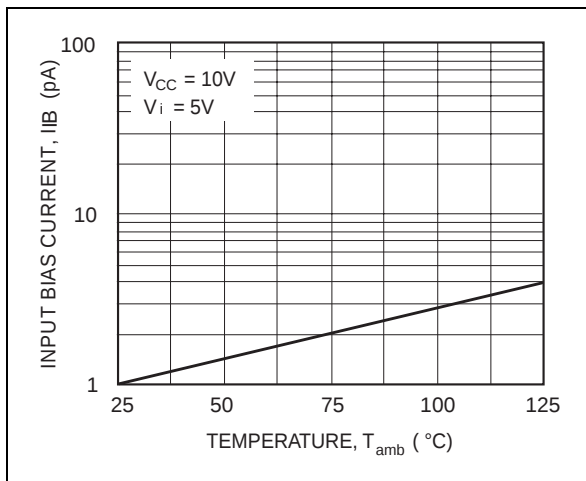


Figure 4 : High Level Output Voltage versus High Level Output Current

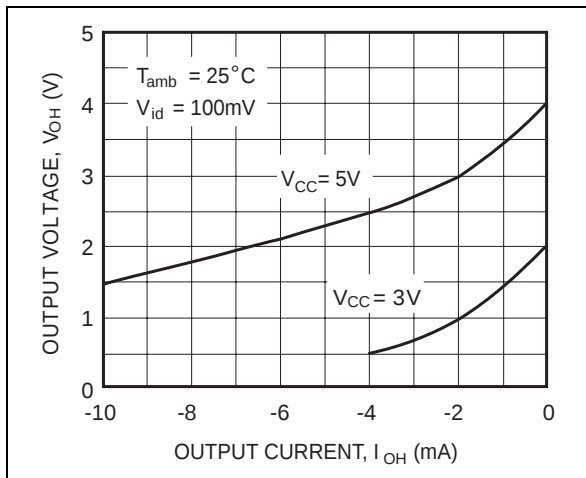


Figure 4b : High Level Output Voltage versus High Level Output Current

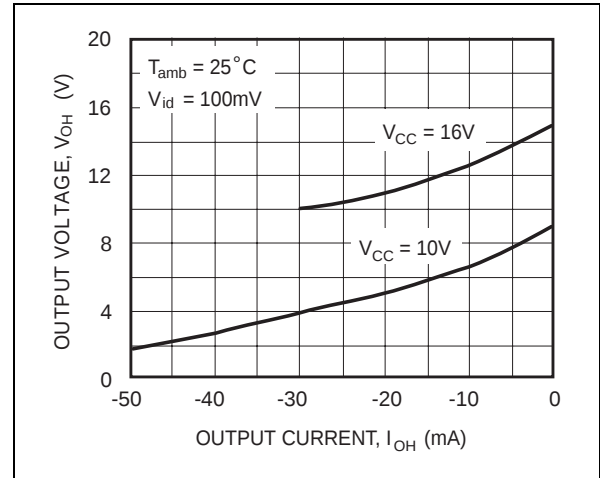


Figure 5a : Low Level Output Voltage versus Low Level Output Current

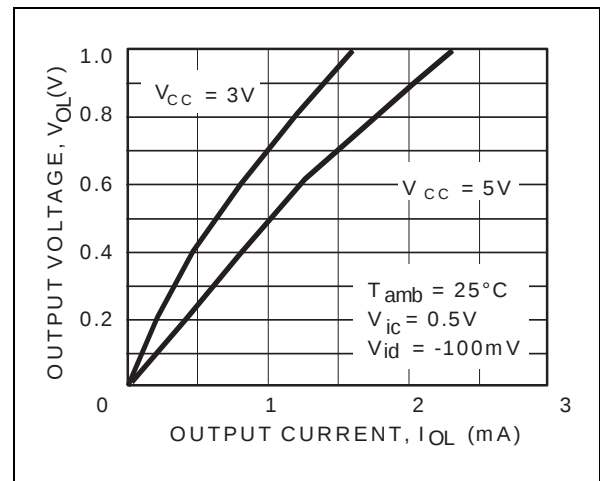


Figure 5b : Low Level Output Voltage versus Low Level Output Current

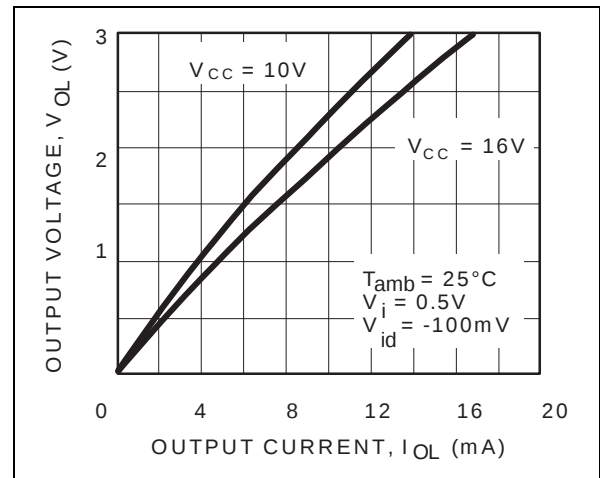
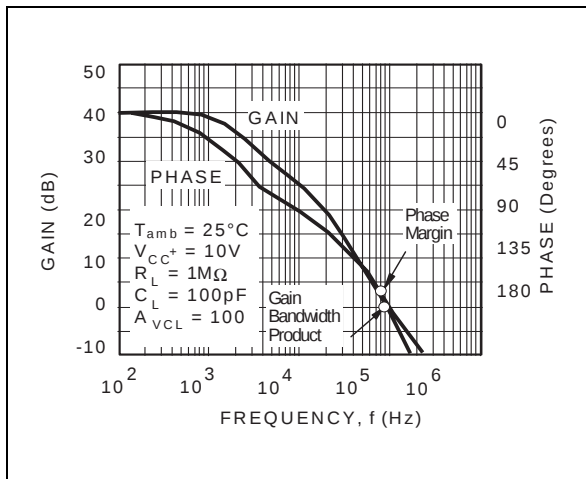
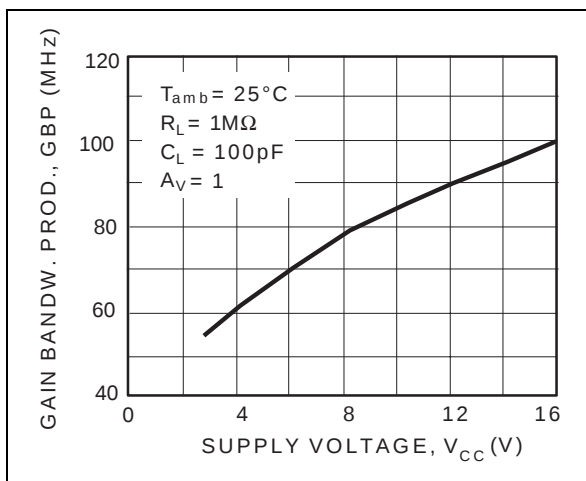
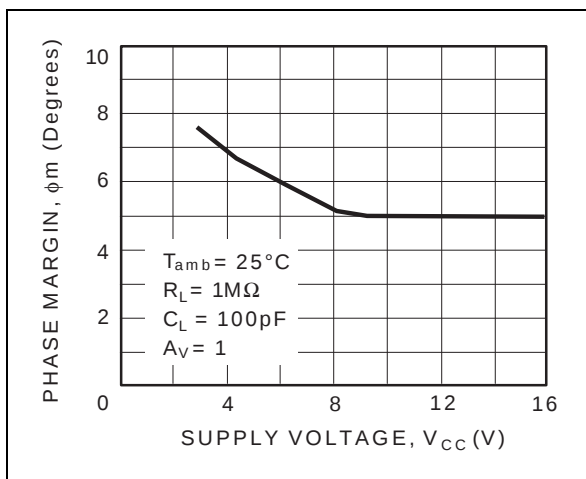
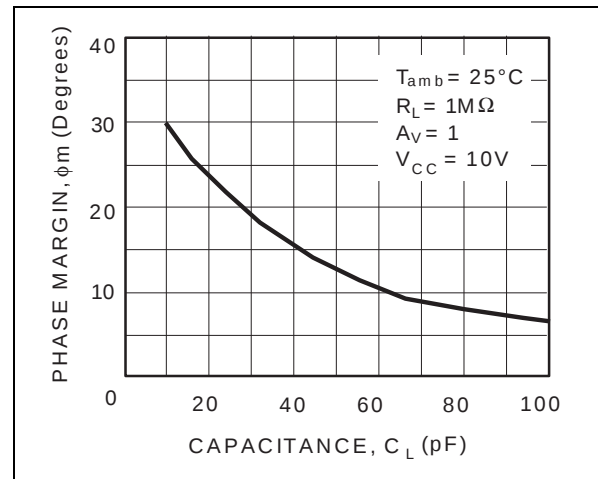
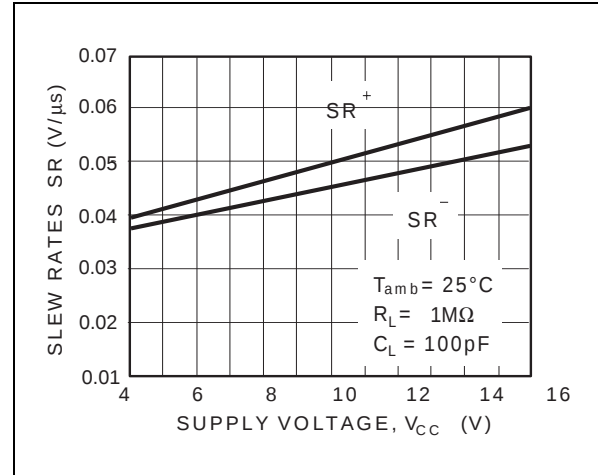


Figure 6 : Open Loop Frequency Response and Phase Shift**Figure 7 : Gain Bandwidth Product versus Supply Voltage****Figure 8 : Phase Margin versus Supply Voltage****Figure 9 : Phase Margin versus Capacitive Load****Figure 10 : Slew Rate versus Supply Voltage**

ELECTRICAL CHARACTERISTICS for $I_{SET} = 25\mu A$
 $V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = +25^\circ C$ (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_{ic} = 0V$ TS271C/I/M TS271AC/AI/AM TS271C/I/M $T_{min} \leq T_{amb} \leq T_{max}$ TS271B/C/I/M TS271AC/AI/AM TS271B/C/I/M		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		$\mu V/^\circ C$
I_{io}	Input Offset Current note ¹⁾ $V_{ic} = 5V$, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1	100		1	200	pA
I_{ib}	Input Bias Current - see note 1 $V_{ic} = 5V$, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1	150		1	300	pA
V_{OH}	High Level Output Voltage $V_{id} = 100mV$, $R_L = 100k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
V_{OL}	Low Level Output Voltage $V_{id} = -100mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_{ic} = 5V$, $R_L = 100k\Omega$, $V_O = 1V$ to $6V$ $T_{min} \leq T_{amb} \leq T_{max}$	30 20	50		30 10	50		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 100pF$, $f_{in} = 100kHz$		0.7			0.7		MHz
CMR	Common Mode Rejection Ratio $V_{ic} = 1V$ to $7.4V$, $V_O = 1.4V$	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_O = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		150	200 250		150	200 300	μA
I_o	Output Short Circuit Current $V_O = 0V$, $V_{id} = 100mV$		60			60		mA
I_{sink}	Output Sink Current $V_O = V_{CC}$, $V_{id} = -100mV$		45			45		mA
SR	Slew Rate at Unity Gain $R_L = 100k\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		0.6			0.6		V/ μs
ϕ_m	Phase Margin at Unity Gain $A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 10pF$ $C_L = 100pF$		50 30			50 30		Degrees
K_{OV}	Overshoot Factor $A_v = 40dB$, $R_L = 100k\Omega$, $C_L = 10pF$ $C_L = 100pF$		30 50			30 50		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_s = 100\Omega$		38			38		$\frac{nV}{\sqrt{Hz}}$

1. Maximum values including unavoidable inaccuracies of the industrial test.

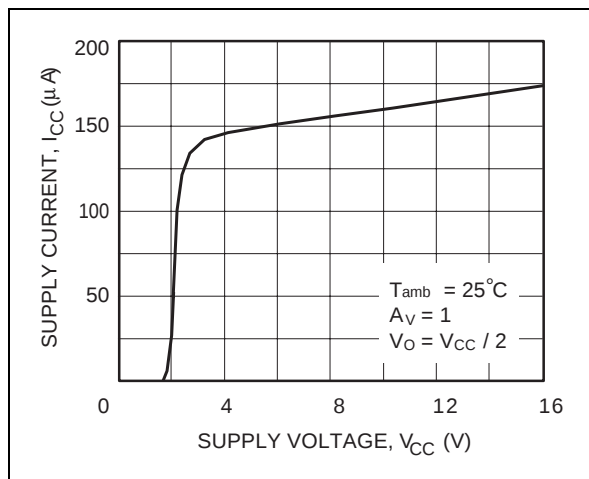
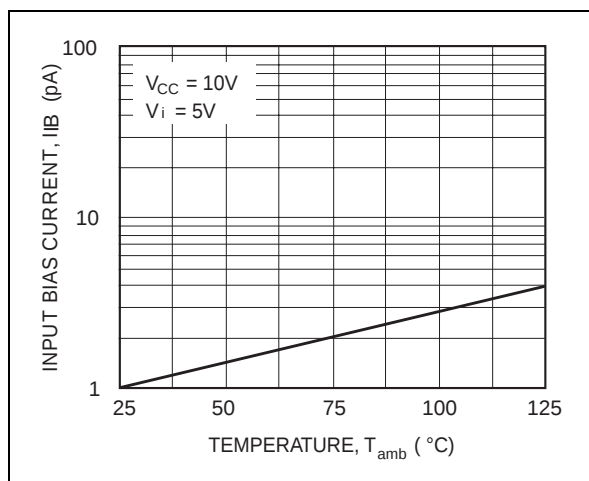
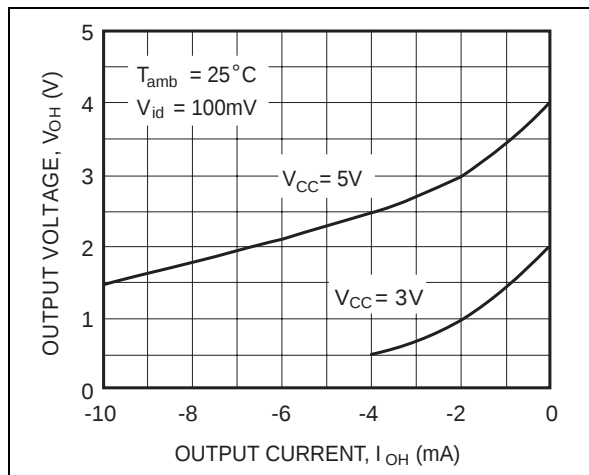
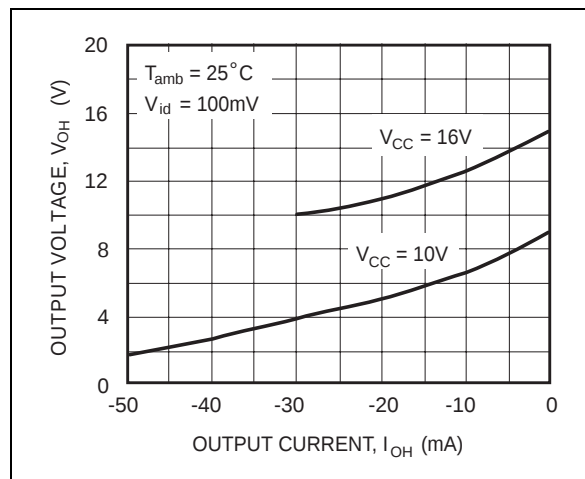
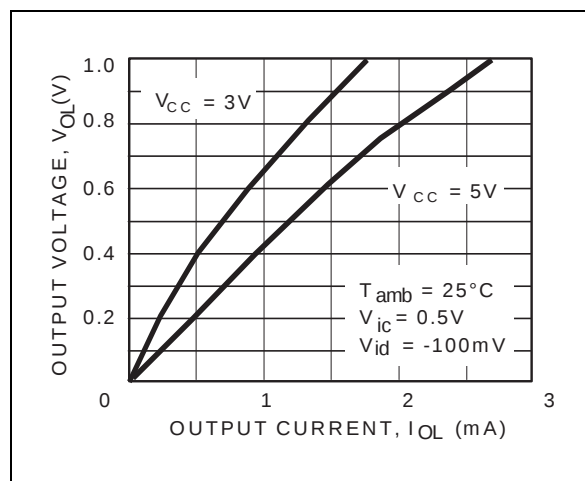
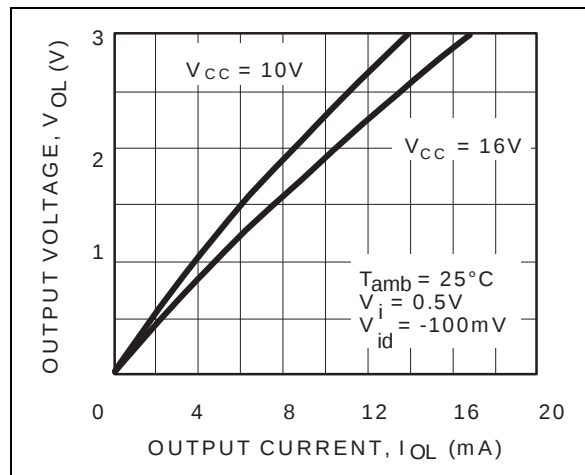
TYPICAL CHARACTERISTICS for $I_{SET} = 25\mu A$ **Figure 11** : Supply Current versus Supply Voltage**Figure 12** : Input Bias Current versus Free Air Temperature**Figure 13a** : High Level Output Voltage versus High Level Output Current**Figure 13b** : High Level Output Voltage versus High Level Output Current**Figure 14a** : Low Level Output Voltage versus Low Level Output Current**Figure 14b** : Low Level Output Voltage versus Low Level Output Current

Figure 15 : Open Loop Frequency Response and Phase Shift

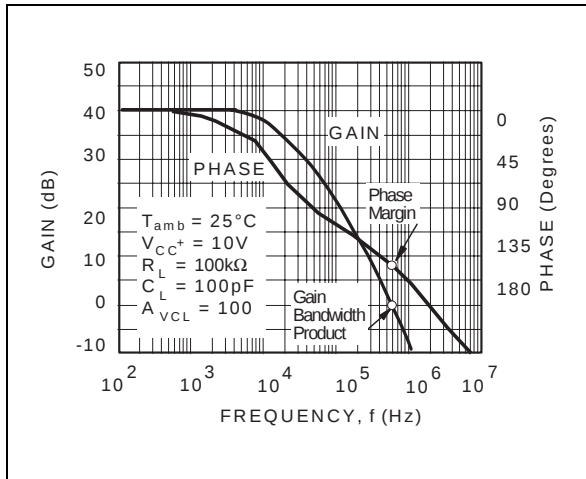


Figure 16 : Gain Bandwidth Product versus Supply Voltage

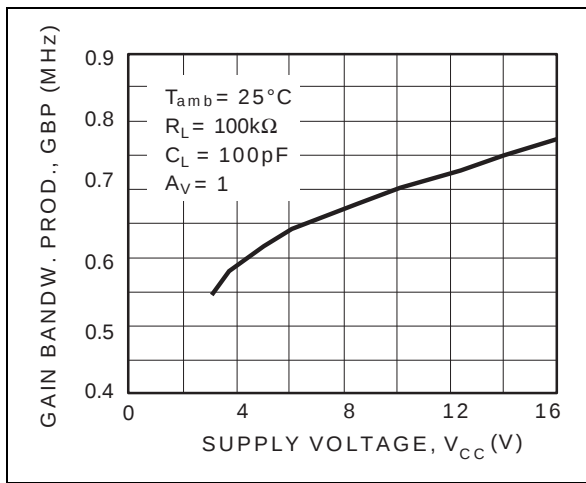


Figure 17 : Phase Margin versus Supply Voltage

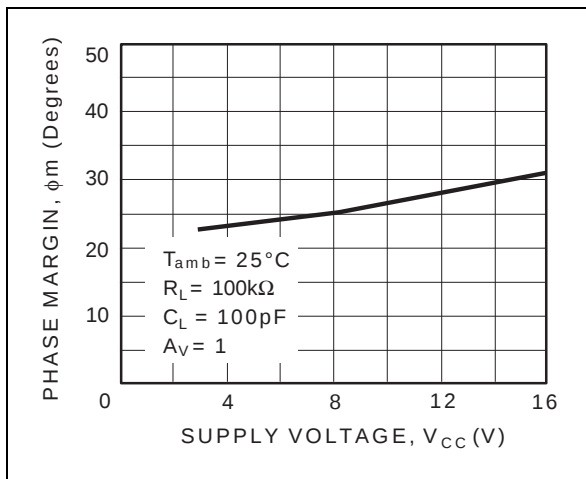


Figure 18 : Phase Margin versus Capacitive Load

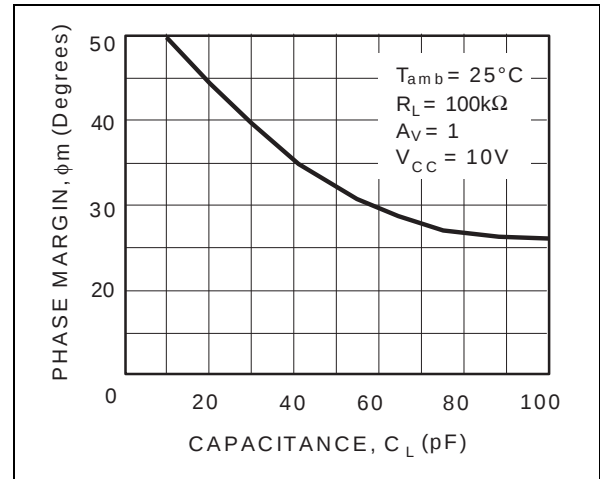
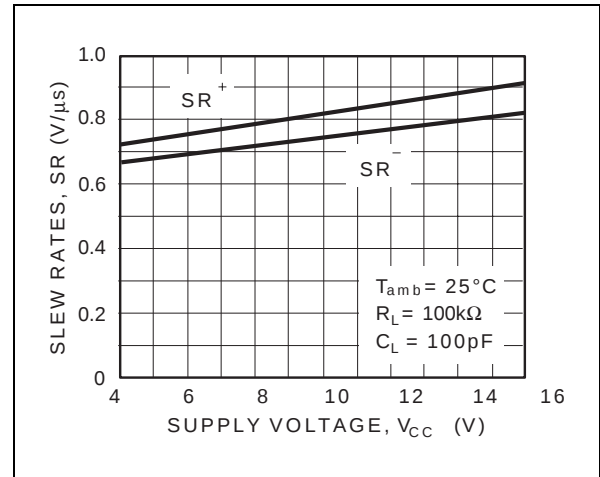


Figure 19 : Slew Rate versus Supply Voltage



ELECTRICAL CHARACTERISTICS for $I_{SET} = 130\mu A$ $V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = +25^\circ C$ (unless otherwise specified)

Symbol	Parameter	TS271C/AC/BC			TS271I/AI/BI TS271M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage $V_O = 1.4V$, $V_{ic} = 0V$ TS271C/I/M TS271AC/AI/AM TS271B/C/I/M $T_{min} \leq T_{amb} \leq T_{max}$ TS271C/I/M TS271AC/AI/AM TS271B/C/I/M		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
DV_{io}	Input Offset Voltage Drift		2			2		$\mu V/^\circ C$
I_{io}	Input Offset Current note 1) $V_{ic} = 5V$, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1	100		1	200	pA
I_{ib}	Input Bias Current - see note 1 $V_{ic} = 5V$, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1	150		1	300	pA
V_{OH}	High Level Output Voltage $V_{id} = 100mV$, $R_L = 10k\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
V_{OL}	Low Level Output Voltage $V_{id} = -100mV$			50			50	mV
A_{vd}	Large Signal Voltage Gain $V_{ic} = 5V$, $R_L = 10k\Omega$, $V_O = 1V$ to $6V$ $T_{min} \leq T_{amb} \leq T_{max}$	10 7	15		10 6	15		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$, $R_L = 10k\Omega$, $C_L = 100pF$, $f_{in} = 100kHz$		2.3			2.3		MHz
CMR	Common Mode Rejection Ratio $V_{ic} = 1V$ to $7.4V$, $V_O = 1.4V$	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$, $V_O = 1.4V$	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		800	1300 1400		800	1300 1500	μA
I_o	Output Short Circuit Current $V_O = 0V$, $V_{id} = 100mV$		60			60		mA
I_{sink}	Output Sink Current $V_O = V_{CC}$, $V_{id} = -100mV$		45			45		mA
SR	Slew Rate at Unity Gain $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		4.5			4.5		V/ μs
ϕ_m	Phase Margin at Unity Gain $A_v = 40dB$, $R_L = 10k\Omega$ $C_L = 10pF$ $C_L = 100pF$		65 30			65 30		Degrees
K_{OV}	Overshoot Factor $A_v = 40dB$, $R_L = 10k\Omega$ $C_L = 10pF$ $C_L = 100pF$		30 50			30 50		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_s = 100\Omega$		30			30		$\frac{nV}{\sqrt{Hz}}$

1. Maximum values including unavoidable inaccuracies of the industrial test.

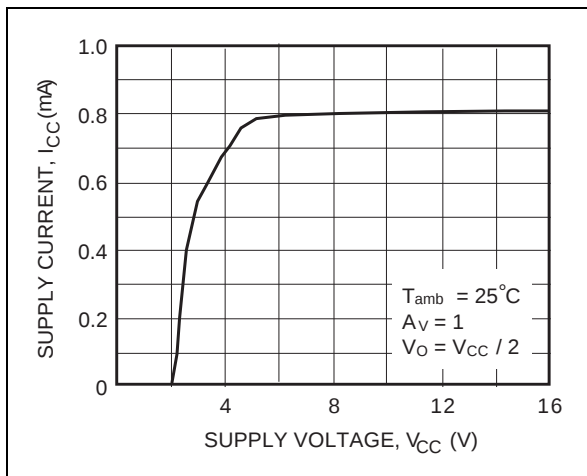
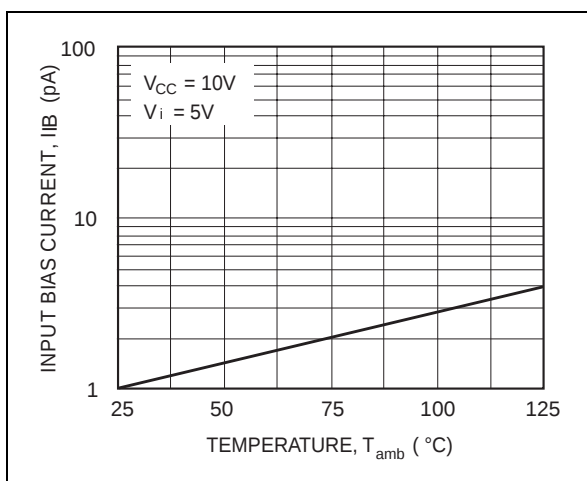
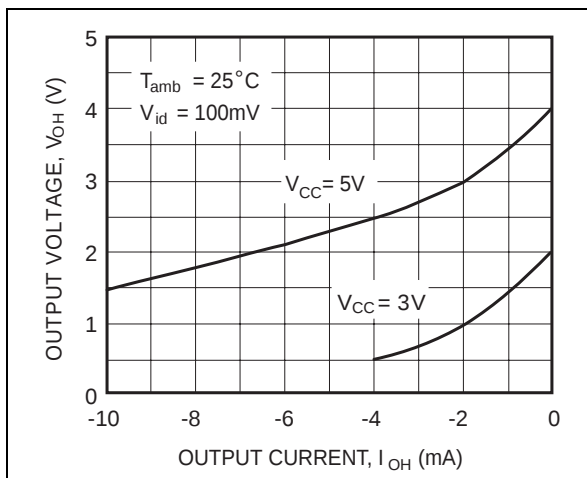
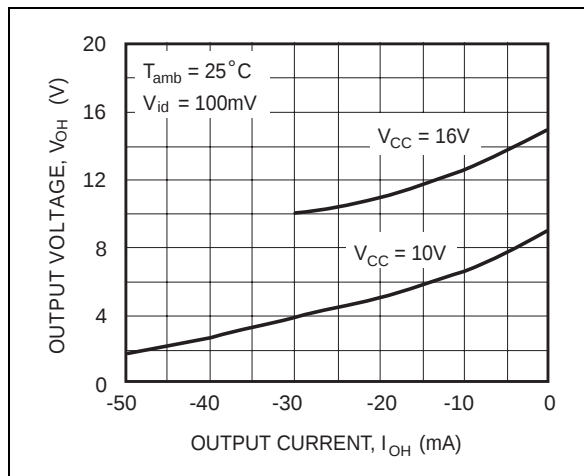
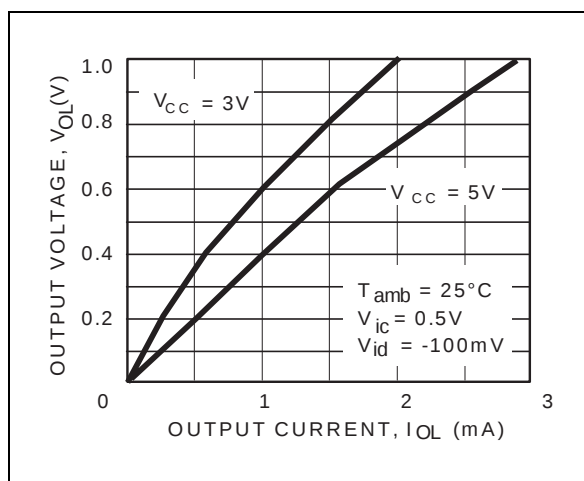
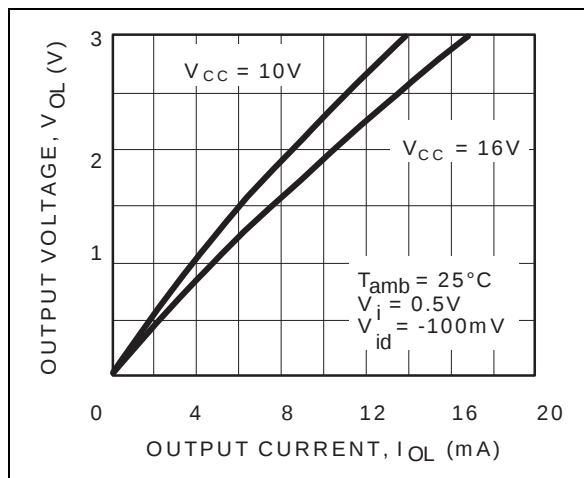
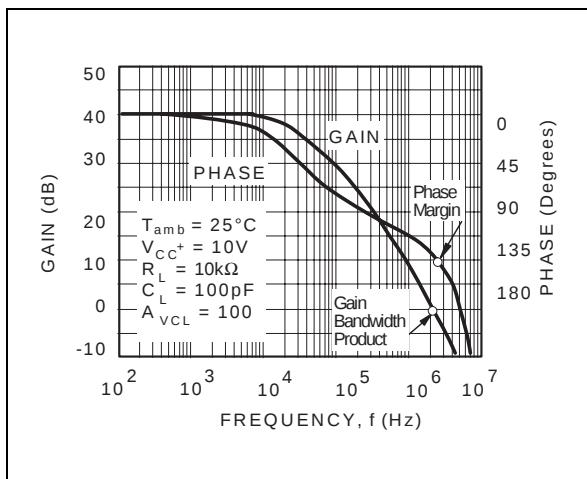
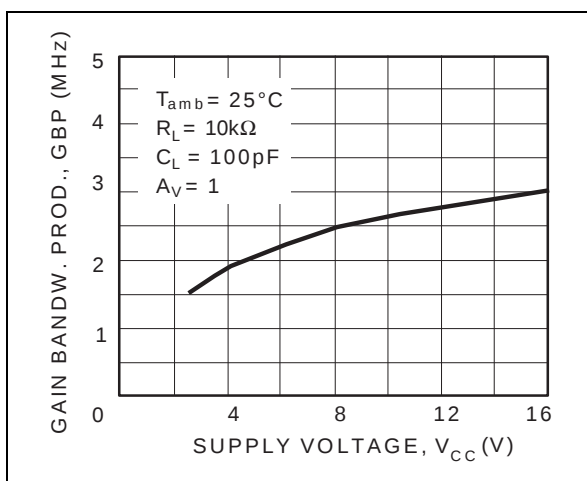
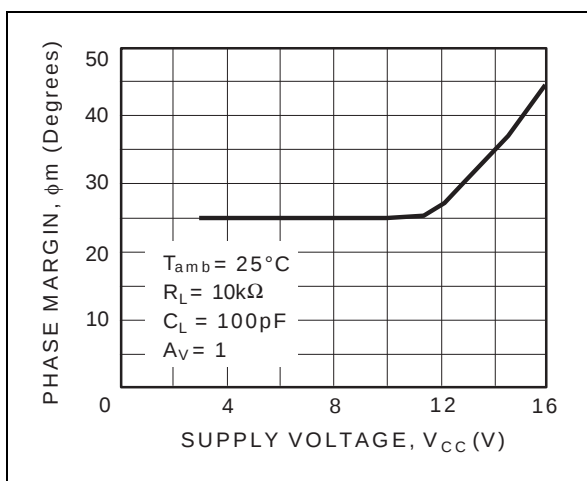
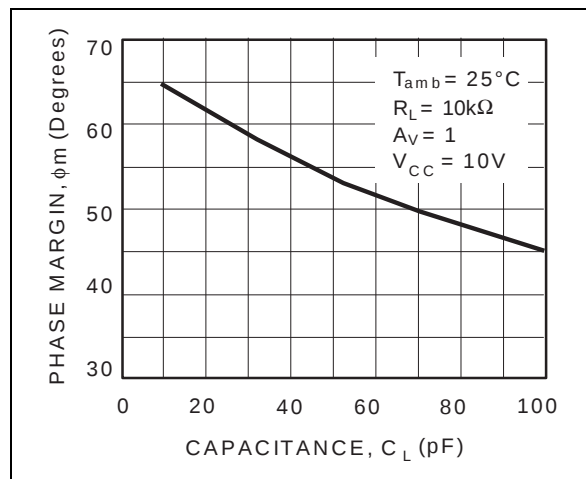
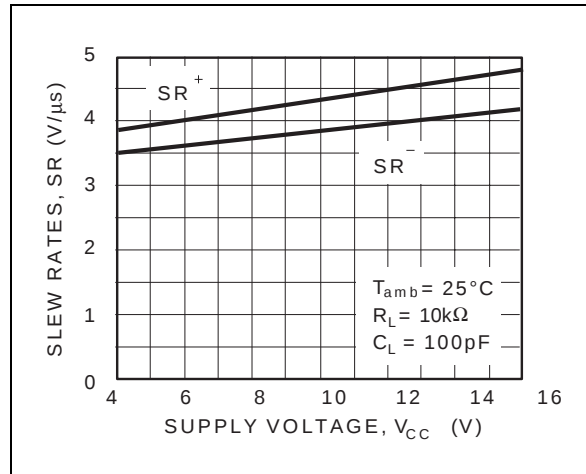
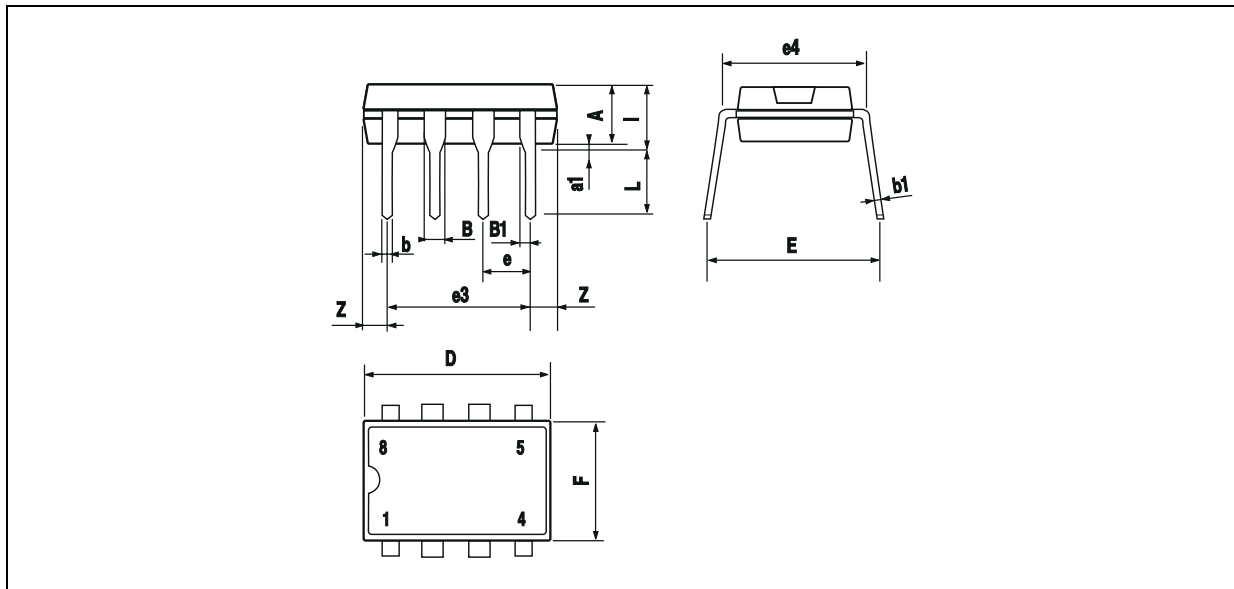
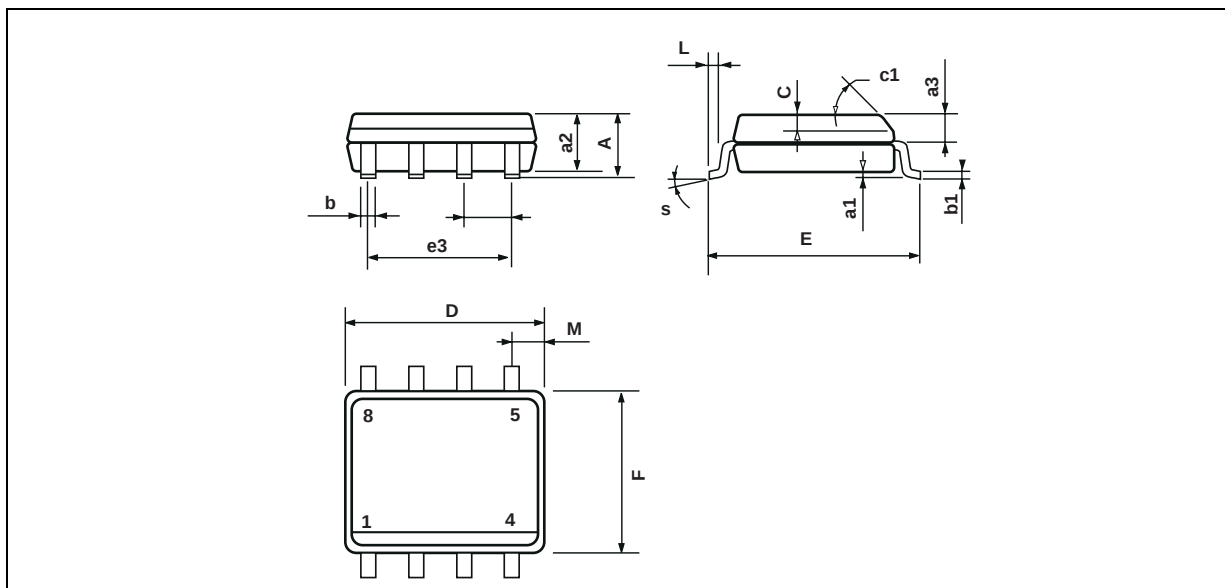
TYPICAL CHARACTERISTICS for $I_{SET} = 130\mu A$ **Figure 20** : Supply Current (each amplifier) versus Supply Voltage**Figure 21** : Input Bias Current versus Free Air Temperature**Figure 22a** : High Level Output Voltage versus High Level Output Current**Figure 22b** : High Level Output Voltage versus High Level Output Current**Figure 23a** : Low Level Output Voltage versus Low Level Output Current**Figure 23b** : Low Level Output Voltage versus Low Level Output Current

Figure 24 : Open Loop Frequency Response and Phase Shift**Figure 25 : Gain Bandwidth Product versus Supply Voltage****Figure 26 : Phase Margin versus Supply Voltage****Figure 27 : Phase Margin versus Capacitive Load****Figure 28 : Slew Rate versus Supply Voltage**

PACKAGE MECHANICAL DATA
 8 PINS - PLASTIC DIP


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

PACKAGE MECHANICAL DATA **8 PINS - PLASTIC MICROPACKAGE (SO)**



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

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