



# TS27L2C,I,M

## PRECISION VERY LOW POWER CMOS DUAL OPERATIONAL AMPLIFIERS

■ VERY LOW POWER CONSUMPTION :  
10µA/op

■ OUTPUT VOLTAGE CAN SWING TO GROUND

■ EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS

■ STABLE AND LOW OFFSET VOLTAGE

■ THREE INPUT OFFSET VOLTAGE SELECTIONS

### DESCRIPTION

These devices are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the ST silicon gate CMOS process allowing an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio:

- $I_{CC} = 10\mu\text{A}/\text{amp.}$ : TS27L2 (very low power)
- $I_{CC} = 150\mu\text{A}/\text{amp.}$ : TS27M2 (low power)
- $I_{CC} = 1\text{mA}/\text{amp.}$ : TS272 (standard)

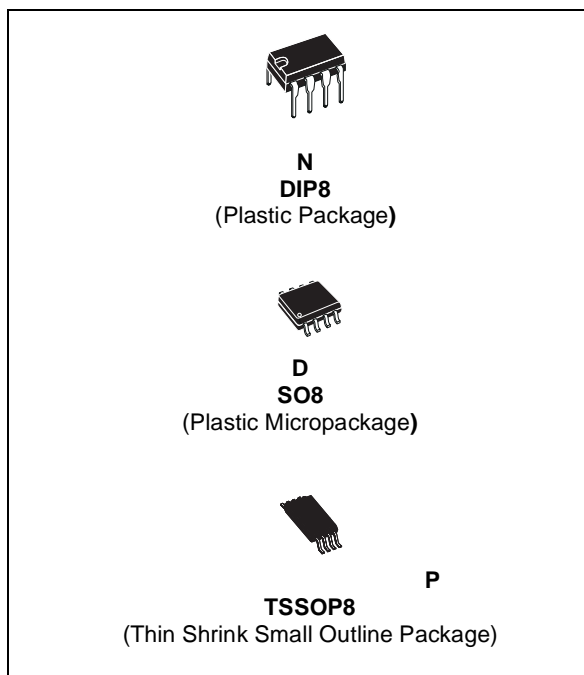
These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input currents drift with temperature (see figure 2).

### ORDER CODE

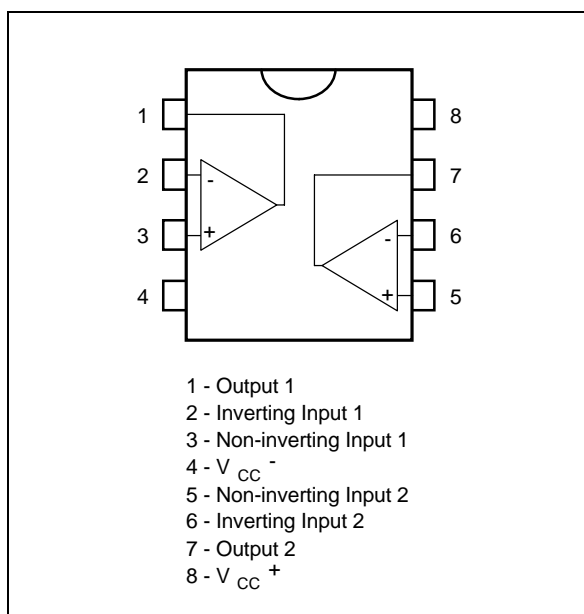
Part Number	Temperature Range	Package		
		N	D	P
TS27L2C/AC/BC	0°C, +70°C	•	•	•
TS27L2I/AI/BI	-40°C, +125°C	•	•	•
TS27L2M/AM/BM	-55°C, +125°C	•	•	•

**Example** : TS27L2ACN

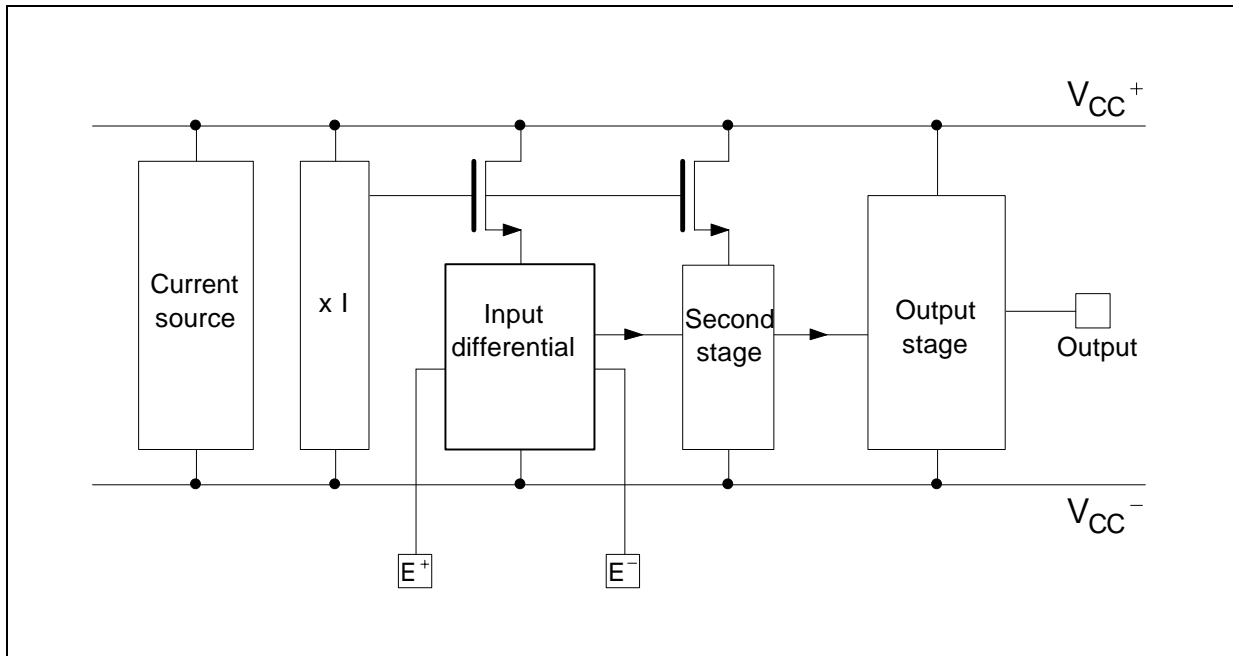
**N** = Dual in Line Package (DIP)  
**D** = Small Outline Package (SO) - also available in Tape & Reel (DT)  
**P** = Thin Shrink Small Outline Package (TSSOP) - only available in Tape & Reel (PT)



### PIN CONNECTIONS (top view)



**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

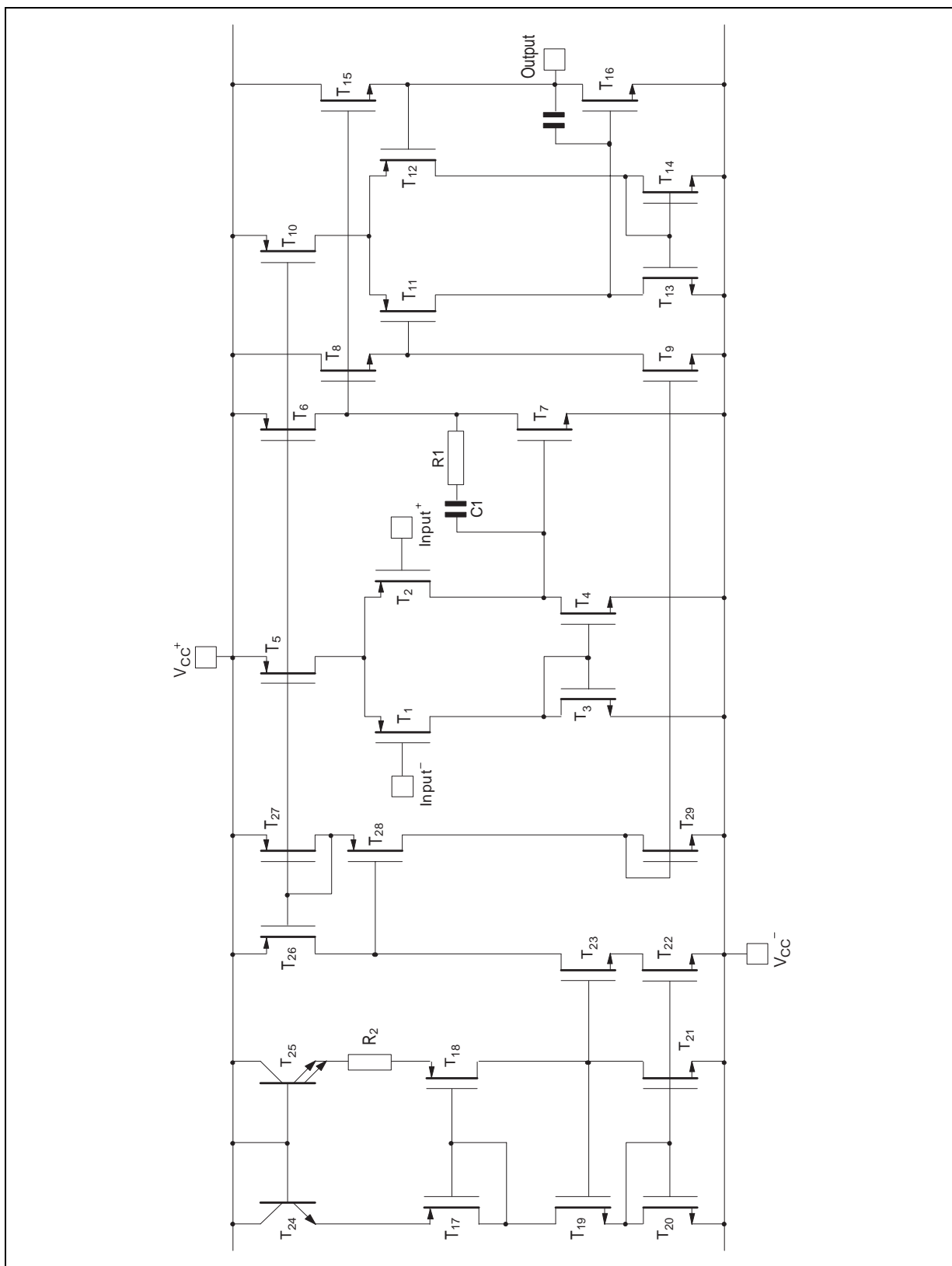
Symbol	Parameter	TS27L2C/AC/BC	TS27L2I/AI/BI	TS27L2M/AM/BM	Unit
$V_{CC}^+$	Supply Voltage <sup>1)</sup>	18			V
$V_{id}$	Differential Input Voltage <sup>2)</sup>	$\pm 18$			V
$V_i$	Input Voltage <sup>3)</sup>	-0.3 to 18			V
$I_o$	Output Current for $V_{CC}^+ \geq 15V$	$\pm 30$			mA
$I_{in}$	Input Current	$\pm 5$			mA
$T_{oper}$	Operating Free-Air Temperature Range	0 to +70	-40 to +125	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150			$^{\circ}C$

1. All values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

**OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}^+$	Supply Voltage	3 to 16	V
$V_{icm}$	Common Mode Input Voltage Range	0 to $V_{CC}^+ - 1.5$	V

**SCHEMATIC DIAGRAM** (for 1/2 TS27L2)



# TS27L2C,I,M

## ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = +10V$ ,  $V_{CC}^- = 0V$ ,  $T_{amb} = +25^\circ C$  (unless otherwise specified)

Symbol	Parameter	TS27L2C/AC/BC			TS27L2I/AI/BI TS27L2M/AM/BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$V_{io}$	Input Offset Voltage $V_O = 1.4V$ , $V_{ic} = 0V$ TS27L2C/I/M TS27L2AC/AI/AM TS27L2B/C/I/M $T_{min} \leq T_{amb} \leq T_{max}$ TS27L2C/I/M TS27L2AC/AI/AM TS27L2B/C/I/M		1.1 0.9 0.25	10 5 2 12 6.5 3		1.1 0.9 0.25	10 5 2 12 6.5 3.5	mV
$DV_{io}$	Input Offset Voltage Drift		2			2		$\mu V/^\circ C$
$I_{io}$	Input Offset Current note 1) $V_{ic} = 5V$ , $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1	100		1	200	pA
$I_{ib}$	Input Bias Current - see note 1 $V_{ic} = 5V$ , $V_O = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1	150		1	300	pA
$V_{OH}$	High Level Output Voltage $V_{id} = 100mV$ , $R_L = 1M\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	8.8 8.7	9		8.8 8.6	9		V
$V_{OL}$	Low Level Output Voltage $V_{id} = -100mV$			50			50	mV
$A_{vd}$	Large Signal Voltage Gain $V_{ic} = 5V$ , $R_L = 1M\Omega$ , $V_o = 1V$ to $6V$ $T_{min} \leq T_{amb} \leq T_{max}$	60 45	100		60 40	100		V/mV
GBP	Gain Bandwidth Product $A_v = 40dB$ , $R_L = 1M\Omega$ , $C_L = 100pF$ , $f_{in} = 100kHz$		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio $V_{ic} = 1V$ to $7.4V$ , $V_o = 1.4V$	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio $V_{CC}^+ = 5V$ to $10V$ , $V_o = 1.4V$	60	80		60	80		dB
$I_{CC}$	Supply Current (per amplifier) $A_v = 1$ , no load, $V_o = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		10	15 17		10	15 18	$\mu A$
$I_o$	Output Short Circuit Current $V_o = 0V$ , $V_{id} = 100mV$		60			60		mA
$I_{sink}$	Output Sink Current $V_o = V_{CC}$ , $V_{id} = -100mV$		45			45		mA
SR	Slew Rate at Unity Gain $R_L = 1M\Omega$ , $C_L = 100pF$ , $V_i = 3$ to $7V$		0.04			0.04		$V/\mu s$
$\phi_m$	Phase Margin at Unity Gain $A_v = 40dB$ , $R_L = 1M\Omega$ , $C_L = 100pF$		45			45		Degrees
$K_{OV}$	Overshoot Factor		30			30		%
$e_n$	Equivalent Input Noise Voltage $f = 1kHz$ , $R_s = 100\Omega$		68			68		$\frac{nV}{\sqrt{Hz}}$
$V_{o1}/V_{o2}$	Channel Separation		120			120		dB

1. Maximum values including unavoidable inaccuracies of the industrial test.

TYPICAL CHARACTERISTICS

Figure 1 : Supply Current (each amplifier) versus Supply Voltage

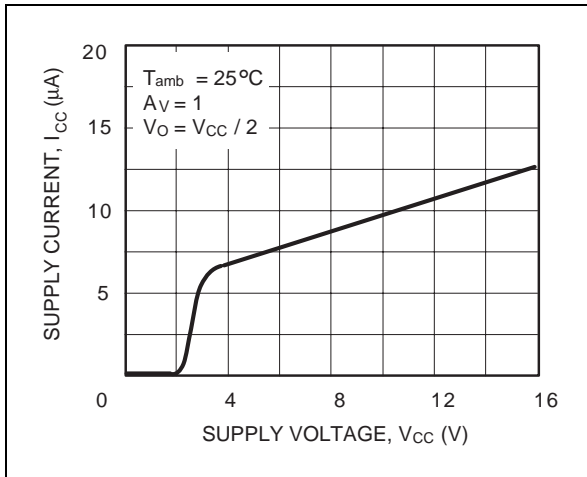


Figure 2 : Input Bias Current versus Free Air Temperature

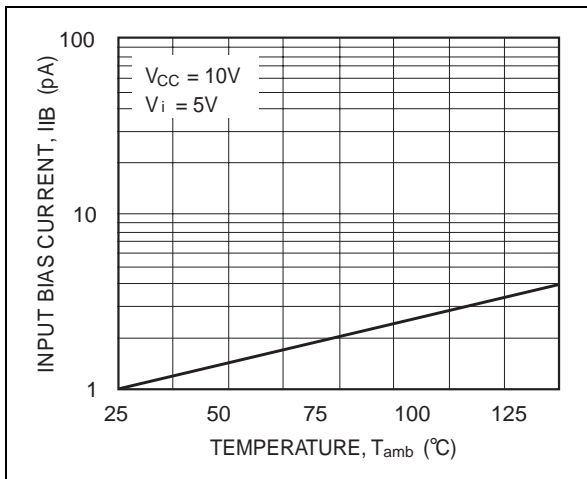


Figure 3a : High Level Output Voltage versus High Level Output Current

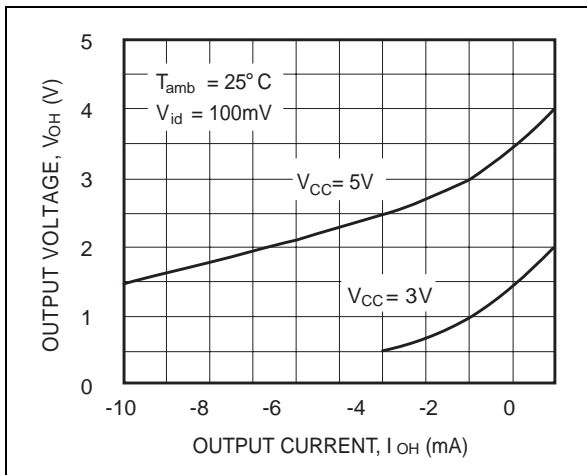


Figure 3b : High Level Output Voltage versus High Level Output Current

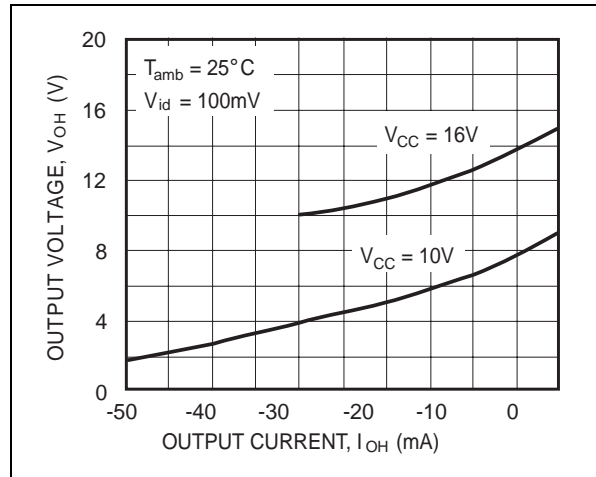


Figure 4a : Low Level Output Voltage versus Low Level Output Current

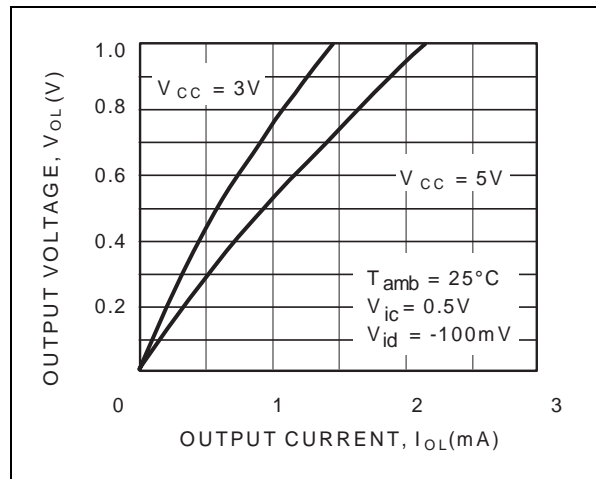
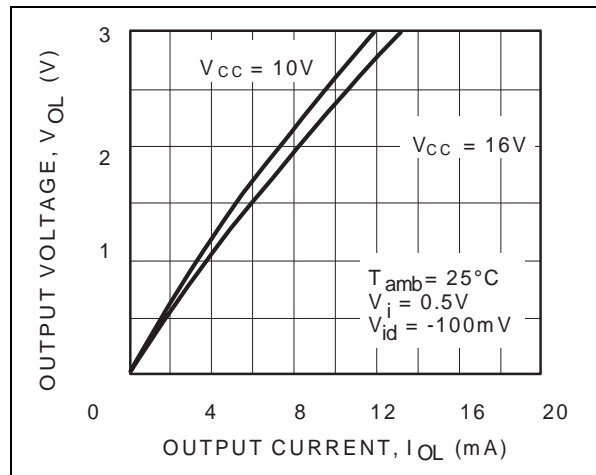
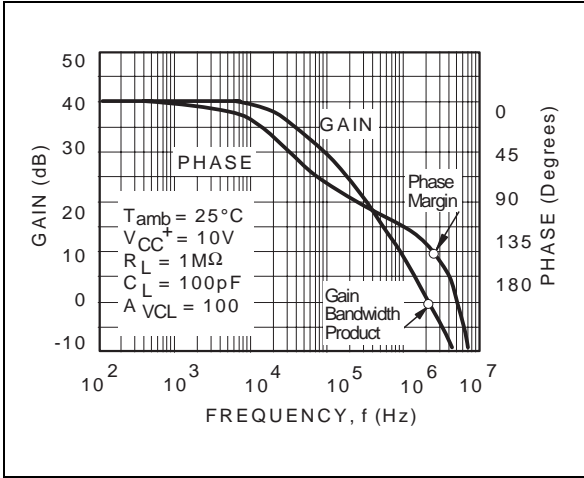


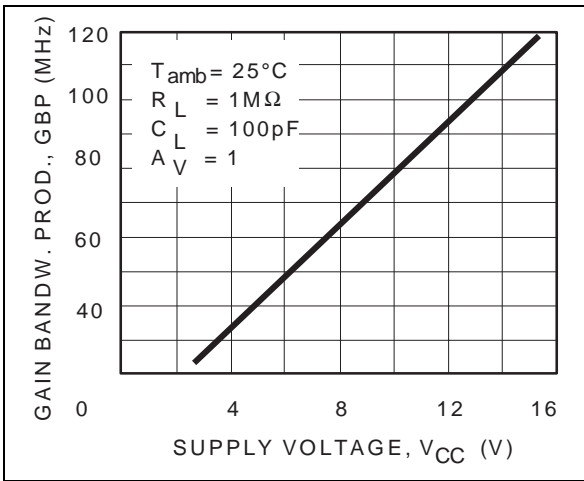
Figure 4b : Low Level Output Voltage versus Low Level Output Current



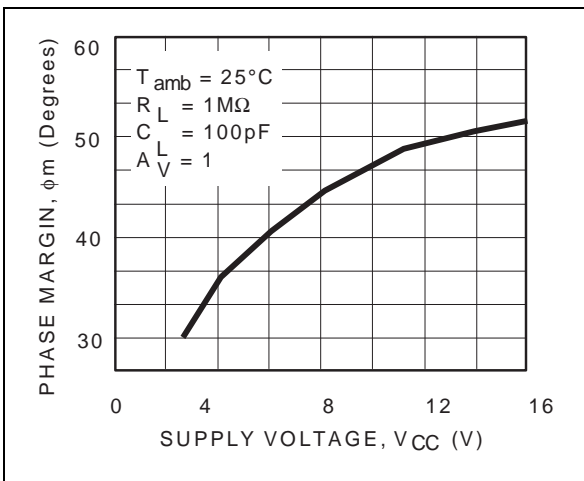
**Figure 5** : Open Loop Frequency Response and Phase Shift



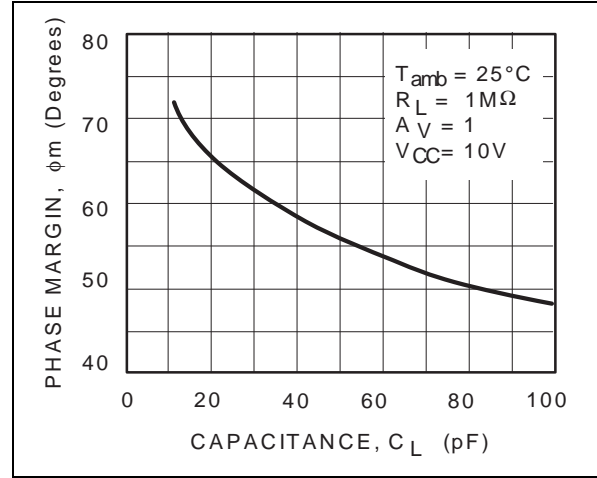
**Figure 6** : Gain Bandwidth Product versus Supply Voltage



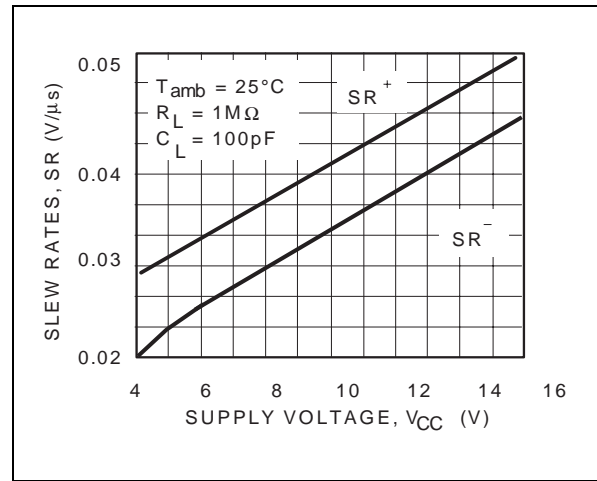
**Figure 7** : Phase Margin versus Supply Voltage



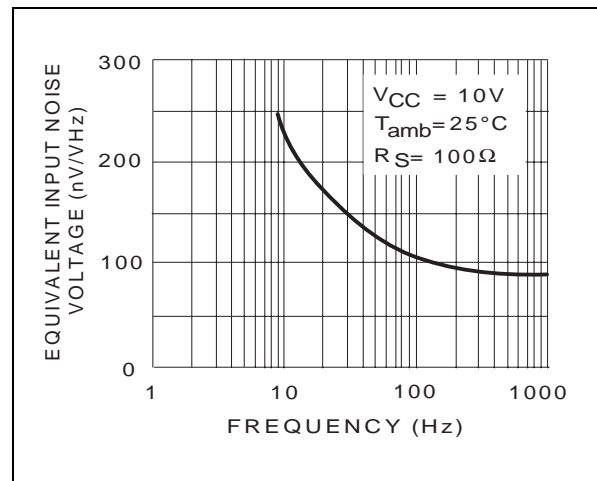
**Figure 8** : Phase Margin versus Capacitive Load



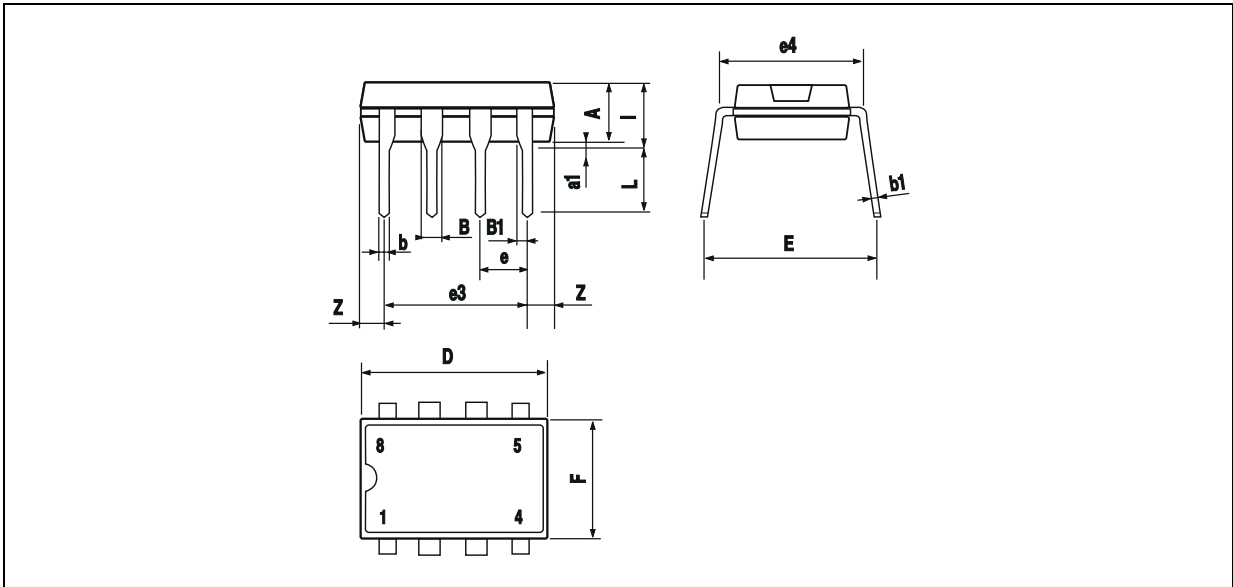
**Figure 9** : Slew Rate versus Supply Voltage



**Figure 10** : Input Voltage Noise versus Frequency



**PACKAGE MECHANICAL DATA**  
8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

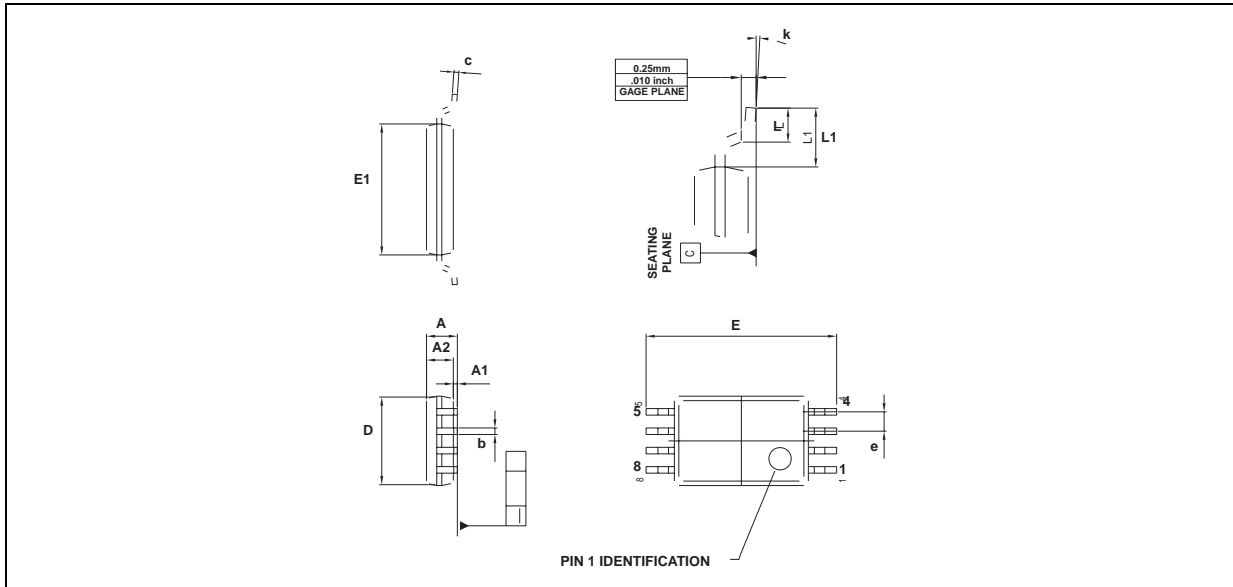
**PACKAGE MECHANICAL DATA**  
8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					



**PACKAGE MECHANICAL DATA**  
**8 PINS - THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)**



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0°		8°	0°		8°
l	0.50	0.60	0.75	0.09	0.0236	0.030
L	0.45	0.600	0.75	0.018	0.024	0.030
L1		1.000			0.039	

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