



TS4890

RAIL TO RAIL OUTPUT 1W AUDIO POWER AMPLIFIER WITH STANDBY MODE ACTIVE LOW

- OPERATING FROM $V_{CC} = 2.2V$ to $5.5V$
- **1W** RAIL TO RAIL OUTPUT POWER @ $V_{CC}=5V$, THD=1%, $f=1kHz$, with 8Ω Load
- ULTRA LOW CONSUMPTION IN STANDBY MODE (**10nA**)
- **75dB** PSRR @ 217Hz from 5 to 2.2V
- POP & CLICK REDUCTION CIRCUITRY
- ULTRA LOW DISTORTION (**0.1%**)
- UNITY GAIN STABLE
- AVAILABLE IN **SO8**, **MiniSO8** & **QFN8**

DESCRIPTION

The TS4890 (MiniSO8 & SO8) is an Audio Power Amplifier capable of delivering 1W of continuous RMS. output power into 8Ω load @ 5V.

This Audio Amplifier is exhibiting 0.1% distortion level (THD) from a 5V supply for a $P_{out} = 250mW$ RMS. An external standby mode control reduces the supply current to less than 10nA. An internal thermal shutdown protection is also provided.

The TS4890 have been designed for high quality audio applications such as mobile phones and to minimize the number of external components.

The unity-gain stable amplifier can be configured by external gain setting resistors.

APPLICATIONS

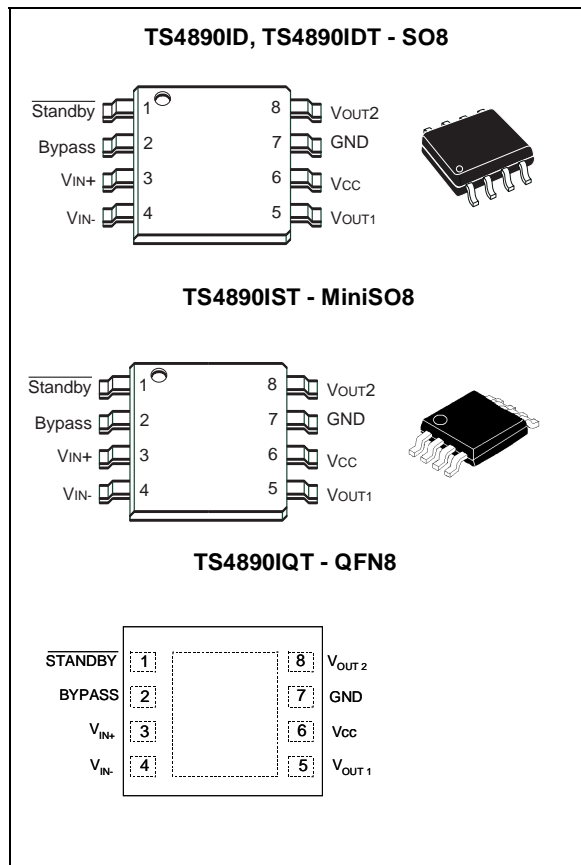
- Mobile Phones (Cellular / Cordless)
- Laptop / Notebook Computers
- PDAs
- Portable Audio Devices

ORDER CODE

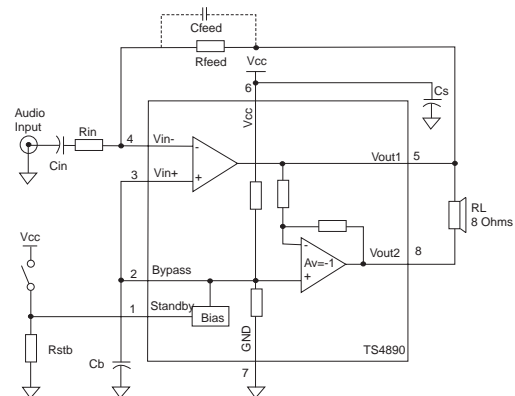
| Part Number | Temperature Range | Package | | |
|-------------|-------------------|---------|---|-----|
| | | S | D | Q |
| TS4890 | -40, +85°C | • | | |
| | | | • | |
| | | | | tba |

MiniSO & QFN only available in Tape & Reel: with T suffix.
SO is available in Tube (D) and of Tape & Reel (DT)

PIN CONNECTIONS (Top View)



TYPICAL APPLICATION SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------|--|--------------------------------------|------|
| V_{CC} | Supply voltage ¹⁾ | 6 | V |
| V_i | Input Voltage ²⁾ | G_{ND} to V_{CC} | V |
| T_{oper} | Operating Free Air Temperature Range | -40 to + 85 | °C |
| T_{stg} | Storage Temperature | -65 to +150 | °C |
| T_j | Maximum Junction Temperature | 150 | °C |
| R_{thja} | Thermal Resistance Junction to Ambient ³⁾ SO8 MiniSO8 QFN8 | 175 215 70 | °C/W |
| P_d | Power Dissipation ⁴⁾ | See Power Derating Curves Fig. 24 | W |
| ESD | Human Body Model | 2 | kV |
| ESD | Machine Model | 200 | V |
| | Latch-up Immunity | Class A | |
| | Lead Temperature (soldering, 10sec) | 260 | °C |

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed $V_{CC} + 0.3V / G_{ND} - 0.3V$
3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4. Exceeding the power derating curves during a long period may involve abnormal working of the device.

OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|------------|--|--|----------|
| V_{CC} | Supply Voltage | 2.2 to 5.5 | V |
| V_{ICM} | Common Mode Input Voltage Range | $G_{ND} + 1V$ to V_{CC} | V |
| V_{STB} | Standby Voltage Input : Device ON Device OFF | $1.5 \leq V_{STB} \leq V_{CC}$ $G_{ND} \leq V_{STB} \leq 0.5$ | V |
| R_L | Load Resistor | 4 - 32 | Ω |
| R_{thja} | Thermal Resistance Junction to Ambient ¹⁾ SO8 MiniSO8 QFN8 ²⁾ | 150 190 41 | °C/W |

1. This thermal resistance can be reduced with a suitable PCB layout (see Power Derating Curves Fig. 24)
2. When mounted on a 4 layers PCB

ELECTRICAL CHARACTERISTICS $V_{CC} = +5V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|---------|
| I_{CC} | Supply Current No input signal, no load | | 6 | 8 | mA |
| $I_{STANDBY}$ | Standby Current ¹⁾ No input signal, $V_{stdby} = G_{ND}$, $R_L = 8\Omega$ | | 10 | 1000 | nA |
| V_{OO} | Output Offset Voltage No input signal, $R_L = 8\Omega$ | | 5 | 20 | mV |
| P_o | Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$ | | 1 | | W |
| THD + N | Total Harmonic Distortion + Noise $P_o = 250mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$ | | 0.15 | | % |
| PSRR | Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, $V_{ripple} = 200mV$ rms | | 77 | | dB |
| Φ_M | Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$ | | 70 | | Degrees |
| GM | Gain Margin $R_L = 8\Omega$, $C_L = 500pF$ | | 20 | | dB |
| GBP | Gain Bandwidth Product $R_L = 8\Omega$ | | 2 | | MHz |

1. Standby mode is activated when V_{stdby} is tied to GND 2. Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$. V_{ripple} is the surimposed sinus signal to V_{CC} @ $f = 217Hz$ $V_{CC} = +3.3V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|---------|
| I_{CC} | Supply Current No input signal, no load | | 5.5 | 8 | mA |
| $I_{STANDBY}$ | Standby Current ¹⁾ No input signal, $V_{stdby} = G_{ND}$, $R_L = 8\Omega$ | | 10 | 1000 | nA |
| V_{OO} | Output Offset Voltage No input signal, $R_L = 8\Omega$ | | 5 | 20 | mV |
| P_o | Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$ | | 450 | | mW |
| THD + N | Total Harmonic Distortion + Noise $P_o = 250mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$ | | 0.15 | | % |
| PSRR | Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, $V_{ripple} = 200mV$ rms | | 77 | | dB |
| Φ_M | Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$ | | 70 | | Degrees |
| GM | Gain Margin $R_L = 8\Omega$, $C_L = 500pF$ | | 20 | | dB |
| GBP | Gain Bandwidth Product $R_L = 8\Omega$ | | 2 | | MHz |

1. Standby mode is activated when V_{stdby} is tied to GND 2. Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$. V_{ripple} is the surimposed sinus signal to V_{CC} @ $f = 217Hz$

$V_{CC} = 2.6V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------|--|------|------|------|---------|
| I_{CC} | Supply Current No input signal, no load | | 5 | 8 | mA |
| $I_{STANDBY}$ | Standby Current ¹⁾ No input signal, $V_{stdby} = G_{ND}$, $R_L = 8\Omega$ | | 10 | 1000 | nA |
| V_{oo} | Output Offset Voltage No input signal, $R_L = 8\Omega$ | | 5 | 20 | mV |
| P_o | Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$ | | 260 | | mW |
| THD + N | Total Harmonic Distortion + Noise $P_o = 200mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$ | | 0.15 | | % |
| PSRR | Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, Vripple = 200mV rms | | 77 | | dB |
| Φ_M | Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$ | | 70 | | Degrees |
| GM | Gain Margin $R_L = 8\Omega$, $C_L = 500pF$ | | 20 | | dB |
| GBP | Gain Bandwidth Product $R_L = 8\Omega$ | | 2 | | MHz |

1. Standby mode is activated when V_{stdby} is tied to GND

2. Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$. Vripple is the surimposed sinus signal to V_{cc} @ $f = 217Hz$

$V_{CC} = 2.2V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------|--|------|------|------|---------|
| I_{CC} | Supply Current No input signal, no load | | 5 | 8 | mA |
| $I_{STANDBY}$ | Standby Current ¹⁾ No input signal, $V_{stdby} = G_{ND}$, $R_L = 8\Omega$ | | 10 | 1000 | nA |
| V_{oo} | Output Offset Voltage No input signal, $R_L = 8\Omega$ | | 5 | 20 | mV |
| P_o | Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$ | | 180 | | mW |
| THD + N | Total Harmonic Distortion + Noise $P_o = 200mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$ | | 0.15 | | % |
| PSRR | Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, Vripple = 100mV rms | | 77 | | dB |
| Φ_M | Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$ | | 70 | | Degrees |
| GM | Gain Margin $R_L = 8\Omega$, $C_L = 500pF$ | | 20 | | dB |
| GBP | Gain Bandwidth Product $R_L = 8\Omega$ | | 2 | | MHz |

1. Standby mode is activated when V_{stdby} is tied to GND

2. Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$. Vripple is the surimposed sinus signal to V_{cc} @ $f = 217Hz$

| Components | Functional Description |
|------------|---|
| Rin | Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin ($f_c = 1 / (2 \times \text{Pi} \times \text{Rin} \times \text{Cin})$) |
| Cin | Input coupling capacitor which blocks the DC voltage at the amplifier input terminal |
| Rfeed | Feed back resistor which sets the closed loop gain in conjunction with Rin |
| Cs | Supply Bypass capacitor which provides power supply filtering |
| Cb | Bypass pin capacitor which provides half supply filtering |
| Cfeed | Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency $1 / (2 \times \text{Pi} \times \text{Rfeed} \times \text{Cfeed})$) |
| Rstb | Pull-down resistor which fixes the right supply level on the standby pin |
| Gv | Closed loop gain in BTL configuration = $2 \times (\text{Rfeed} / \text{Rin})$ |

REMARKS

- All measurements, except PSRR measurements, are made with a supply bypass capacitor $C_s = 100\mu\text{F}$.
- External resistors are not needed for having better stability when supply @ V_{cc} down to 3V. The quiescent current still remains the same.
- The standby response time is about $1\mu\text{s}$.

Fig. 1 : Open Loop Frequency Response

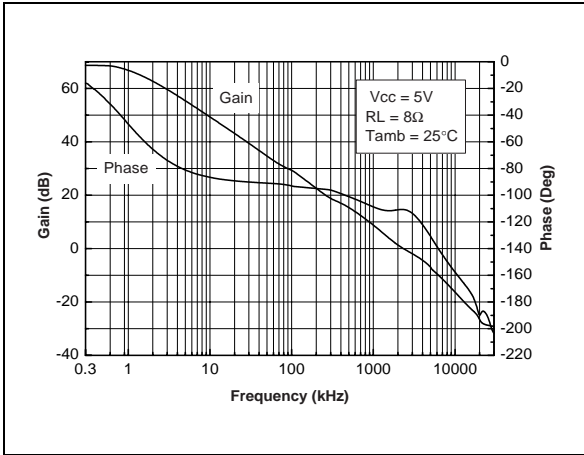


Fig. 2 : Open Loop Frequency Response

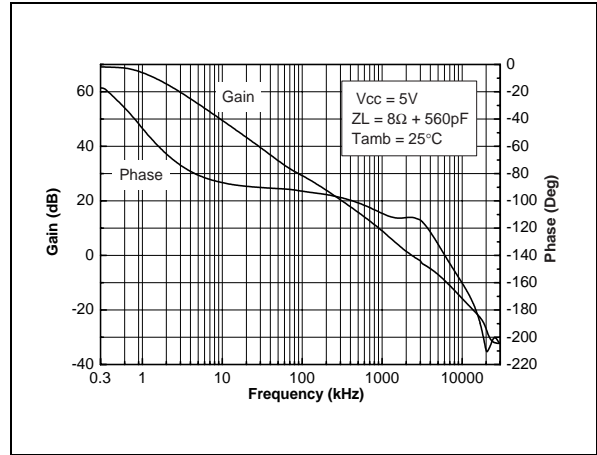


Fig. 3 : Open Loop Frequency Response

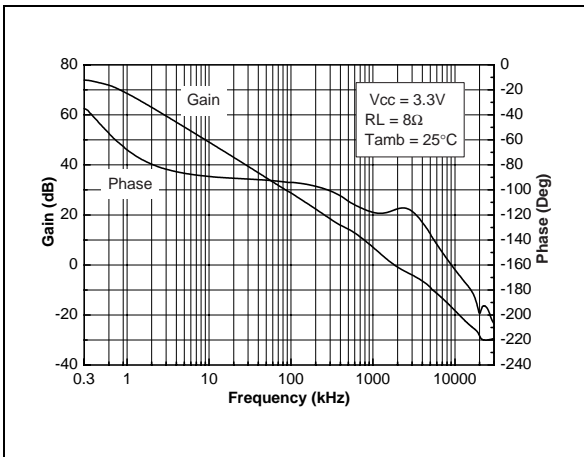


Fig. 4 : Open Loop Frequency Response

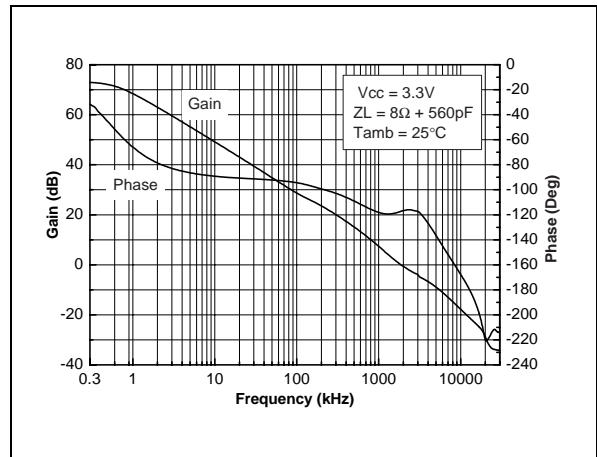


Fig. 5 : Open Loop Frequency Response

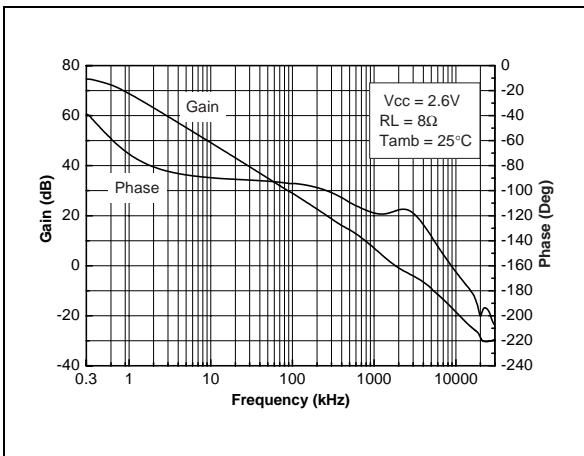


Fig. 6 : Open Loop Frequency Response

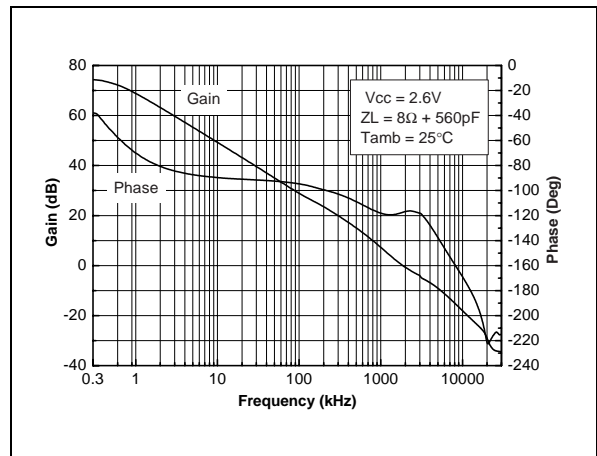


Fig. 7 : Open Loop Frequency Response

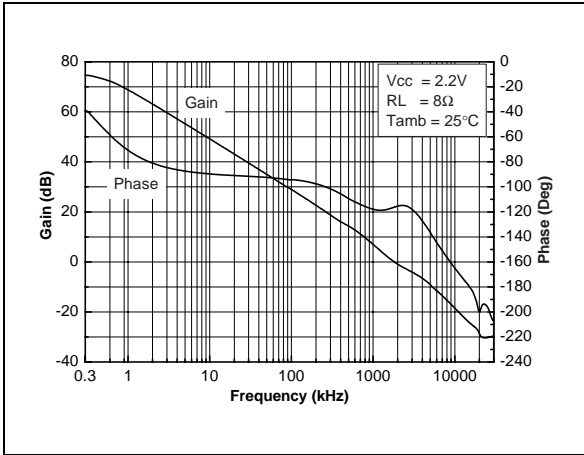


Fig. 8 : Open Loop Frequency Response

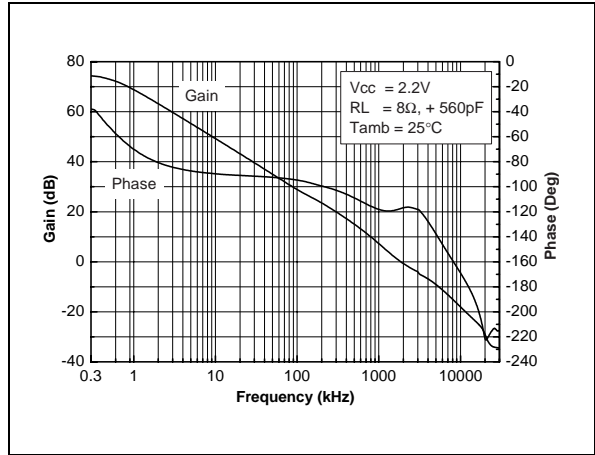


Fig. 9 : Open Loop Frequency Response

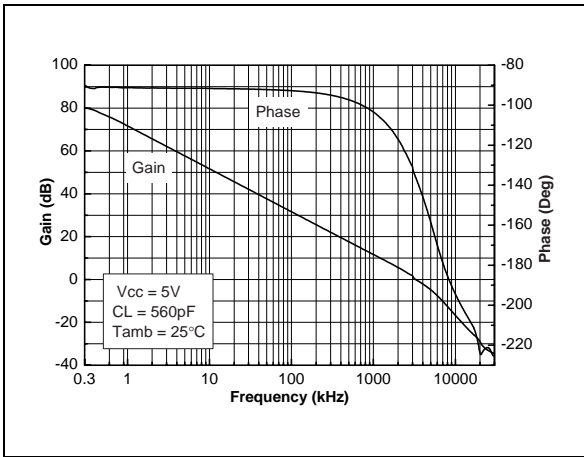


Fig. 10 : Open Loop Frequency Response

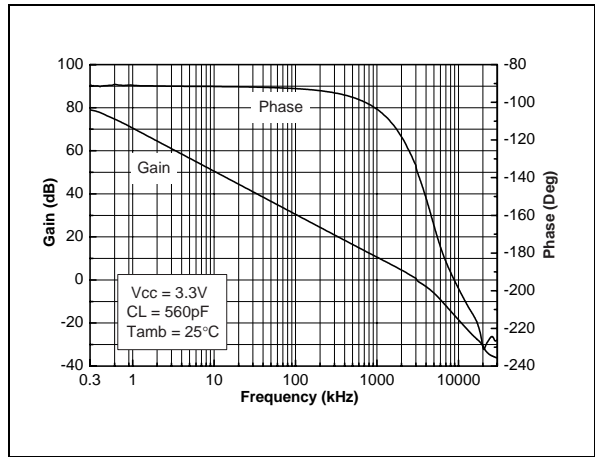


Fig. 11 : Open Loop Frequency Response

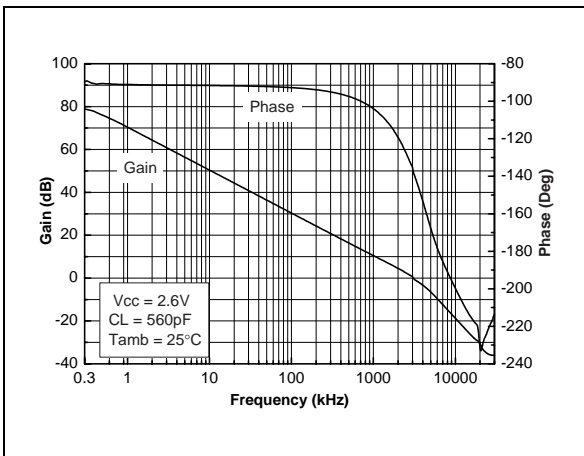


Fig. 12 : Open Loop Frequency Response

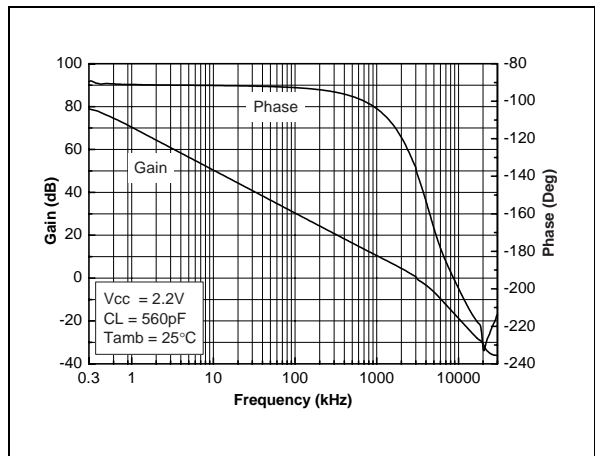


Fig. 13 : Power Supply Rejection Ratio (PSRR) vs Power supply

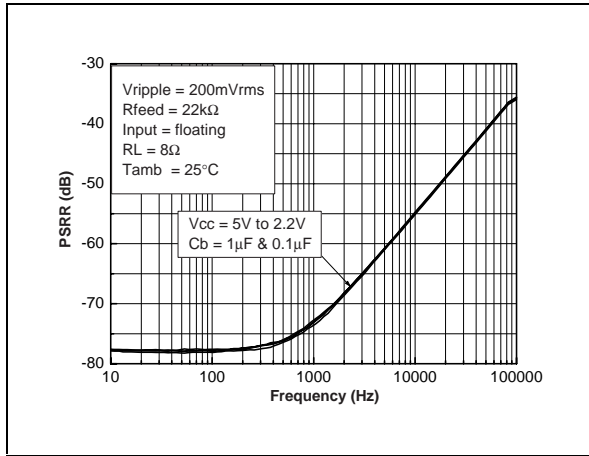


Fig. 14 : Power Supply Rejection Ratio (PSRR) vs Feedback Capacitor

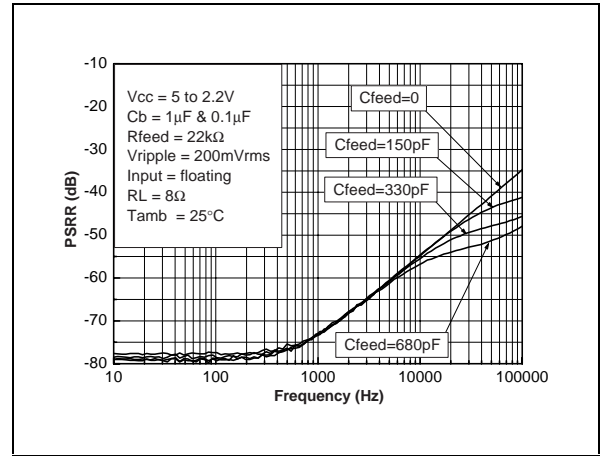


Fig. 15 : Power Supply Rejection Ratio (PSRR) vs Bypass Capacitor

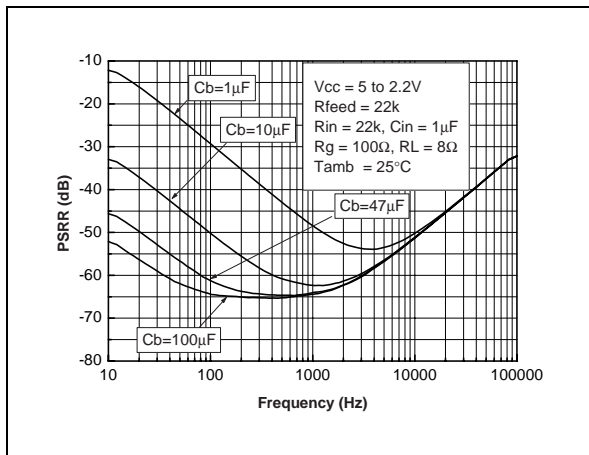


Fig. 16 : Power Supply Rejection Ratio (PSRR) vs Input Capacitor

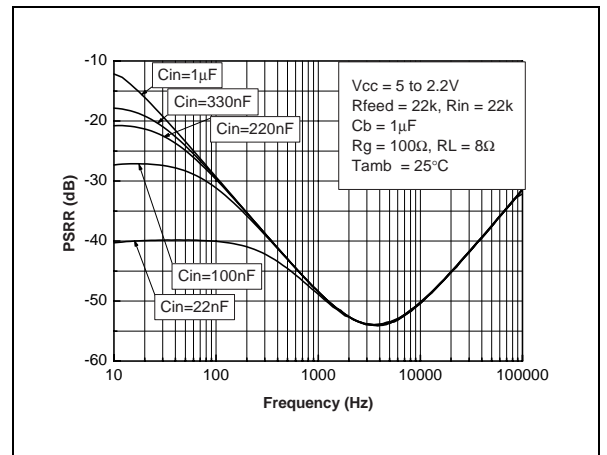


Fig. 17 : Power Supply Rejection Ratio (PSRR) vs Feedback Resistor

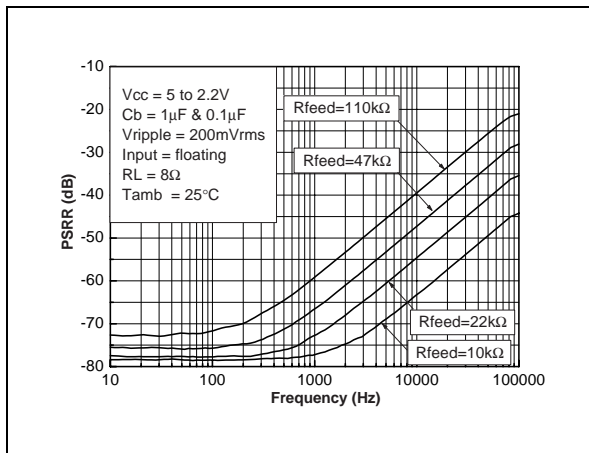


Fig. 18 : Pout @ THD + N = 1% vs Supply Voltage vs RL

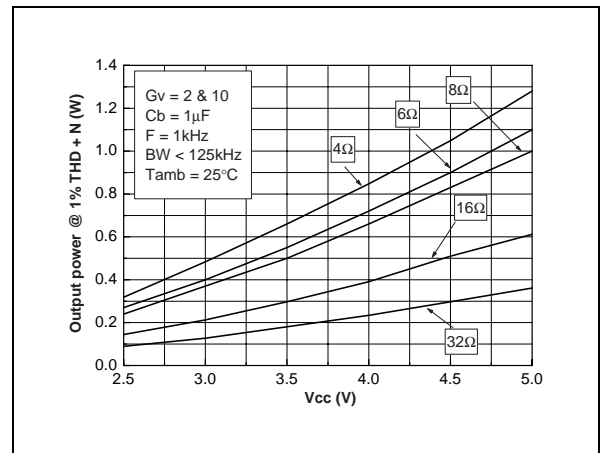


Fig. 19 : Pout @ THD + N = 10% vs Supply Voltage vs RL

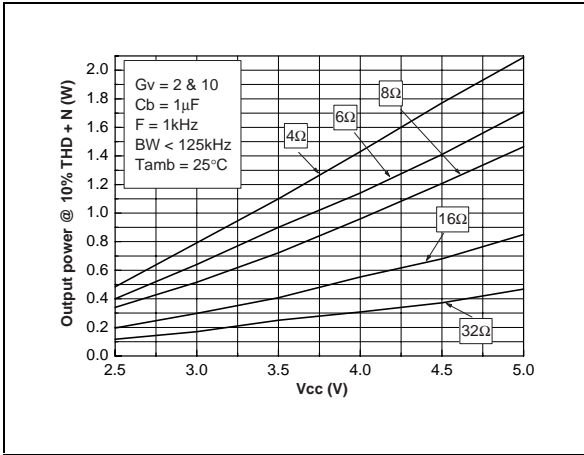


Fig. 20 : Power Dissipation vs Pout

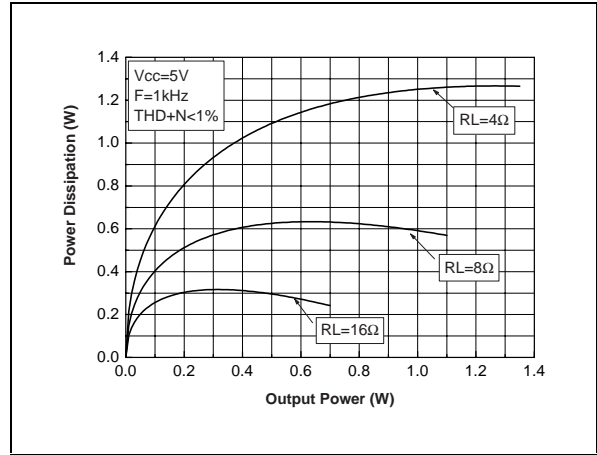


Fig. 21 : Power Dissipation vs Pout

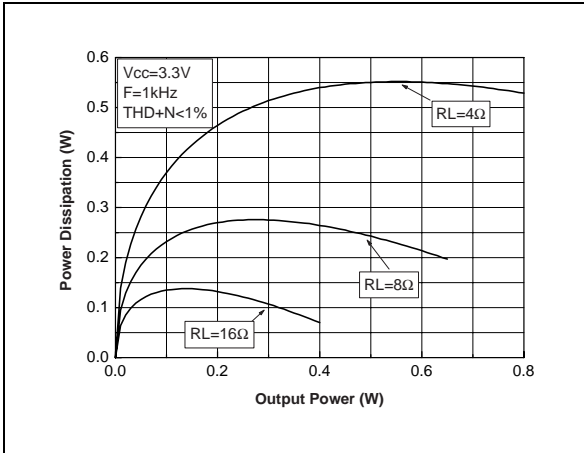


Fig. 22 : Power Dissipation vs Pout

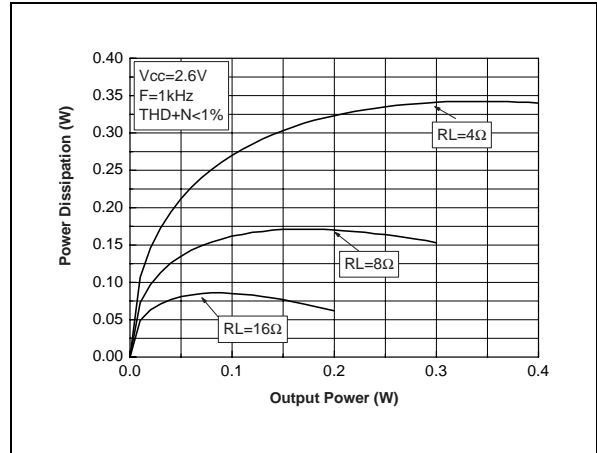


Fig. 23 : Power Dissipation vs Pout

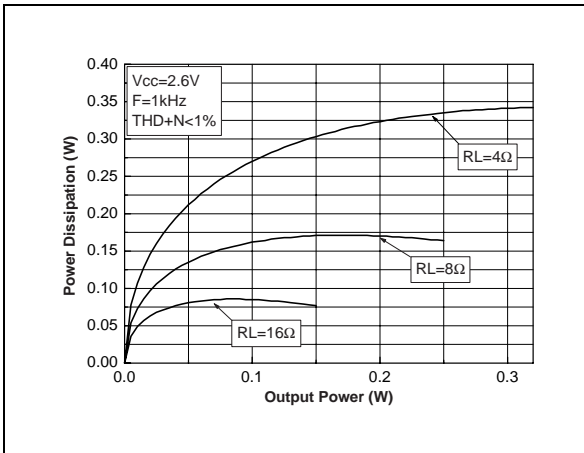


Fig. 24 : Power Derating Curves

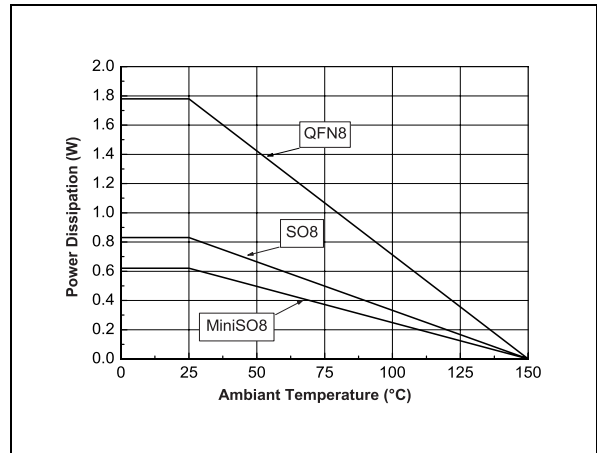


Fig. 25 : THD + N vs Output Power

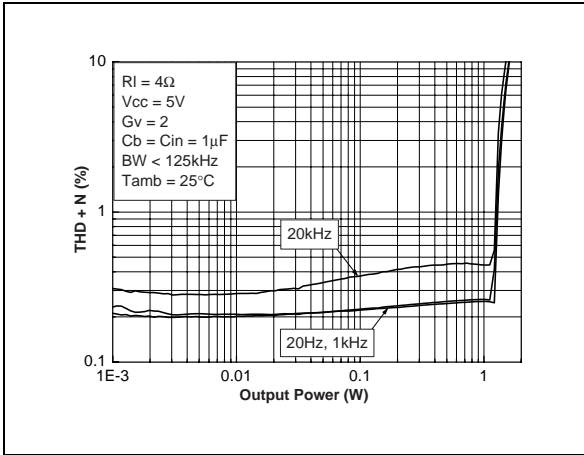


Fig. 26 : THD + N vs Output Power

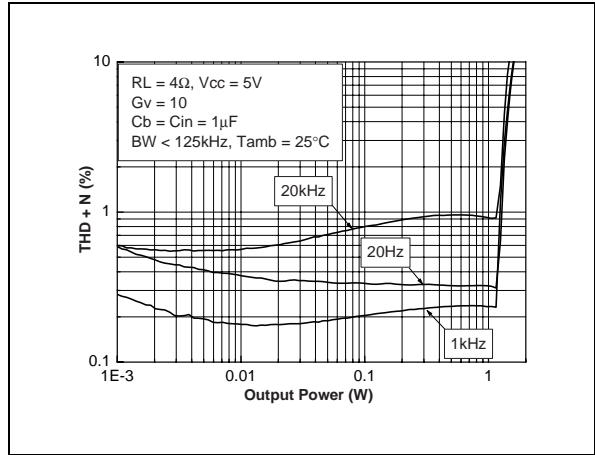


Fig. 27 : THD + N vs Output Power

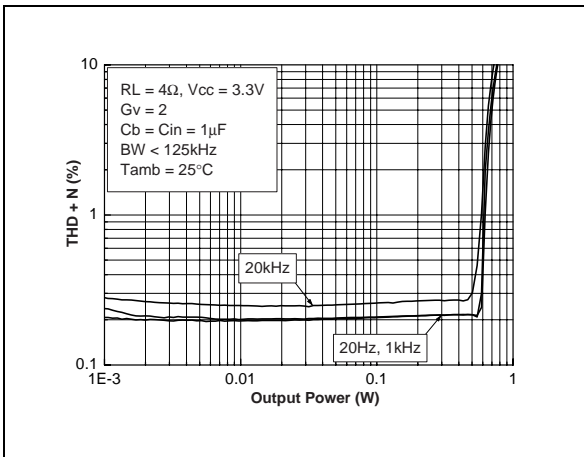


Fig. 28 : THD + N vs Output Power

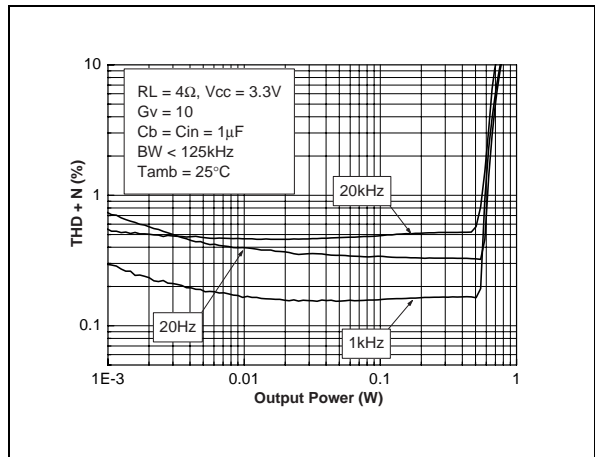


Fig. 29 : THD + N vs Output Power

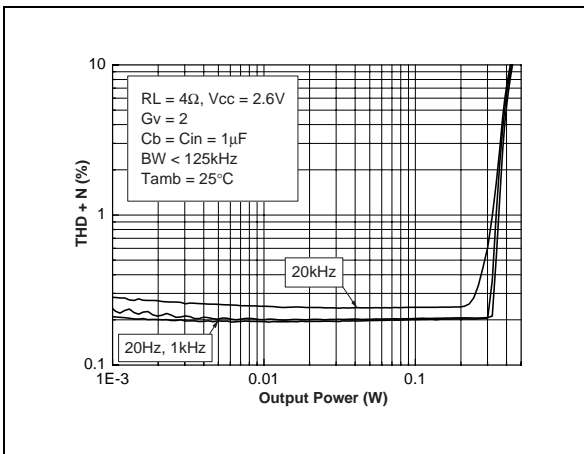


Fig. 30 : THD + N vs Output Power

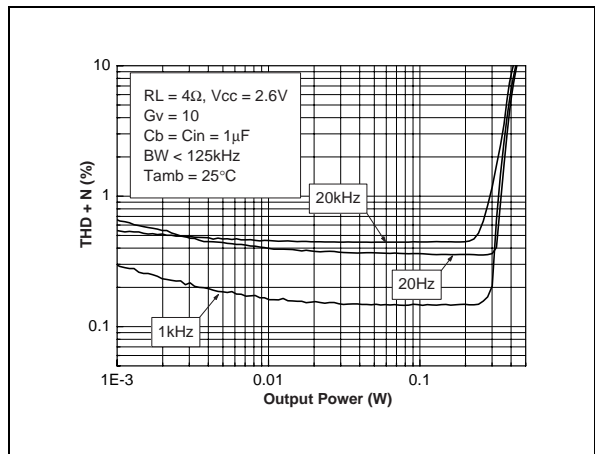


Fig. 31 : THD + N vs Output Power

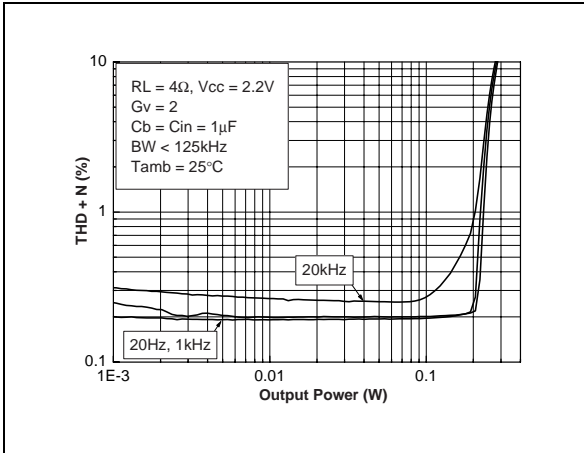


Fig. 32 : THD + N vs Output Power

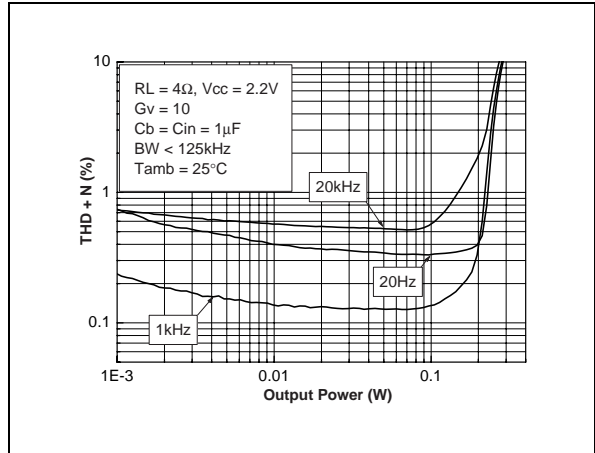


Fig. 33 : THD + N vs Output Power

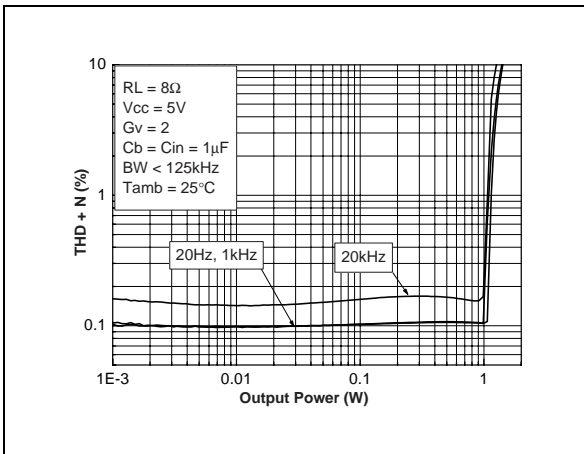


Fig. 34 : THD + N vs Output Power

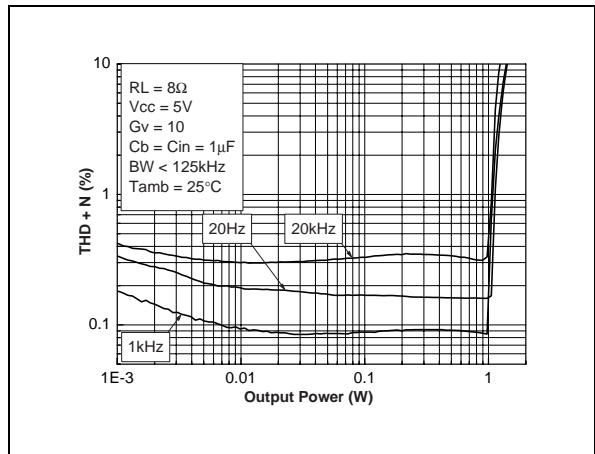


Fig. 35 : THD + N vs Output Power

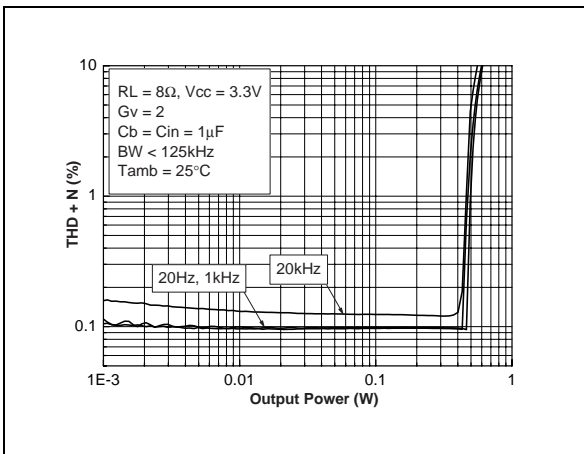


Fig. 36 : THD + N vs Output Power

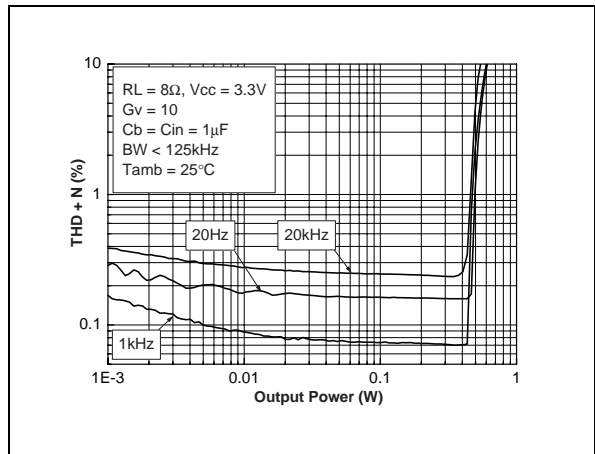


Fig. 37 : THD + N vs Output Power

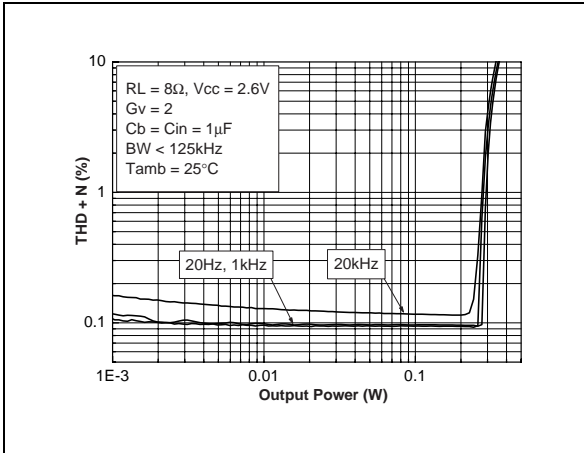


Fig. 38 : THD + N vs Output Power

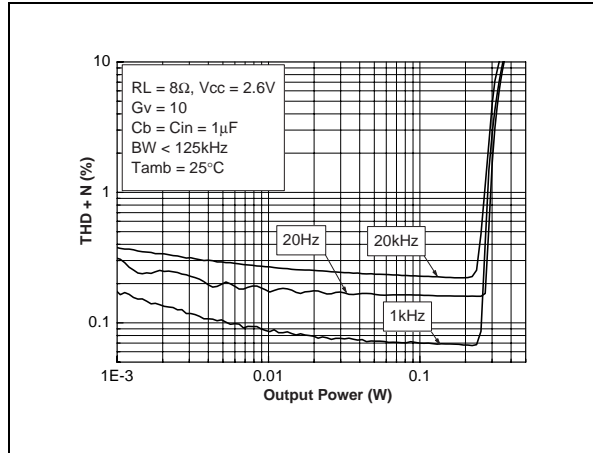


Fig. 39 : THD + N vs Output Power

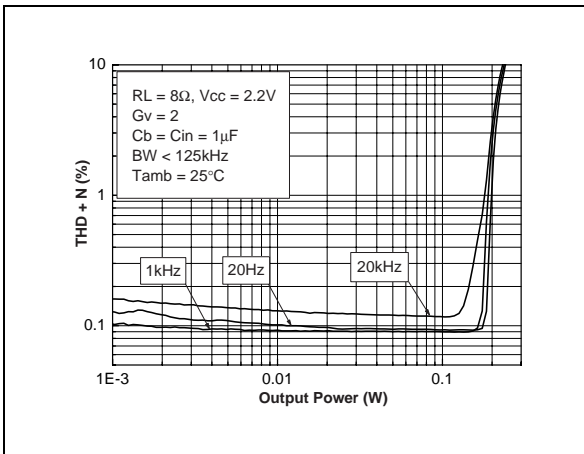


Fig. 40 : THD + N vs Output Power

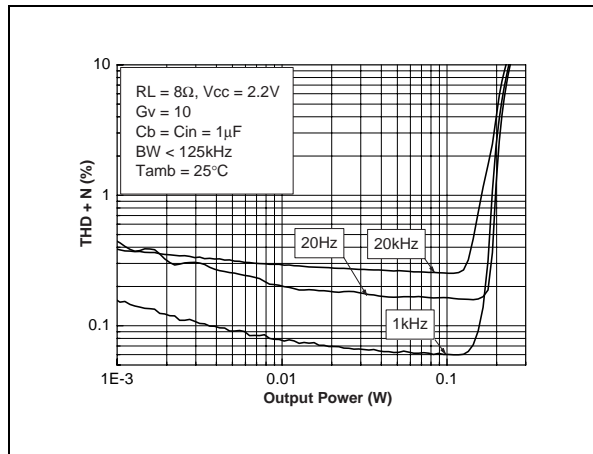


Fig. 41 : THD + N vs Output Power

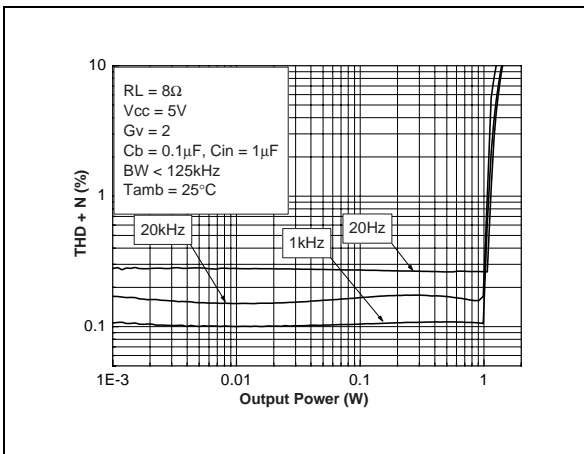


Fig. 42 : THD + N vs Output Power

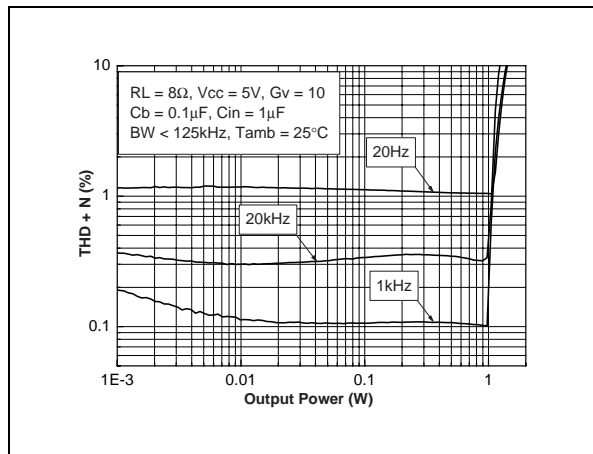


Fig. 43 : THD + N vs Output Power

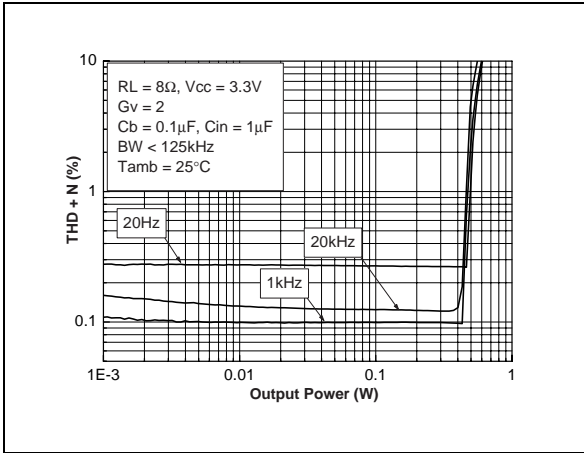


Fig. 44 : THD + N vs Output Power

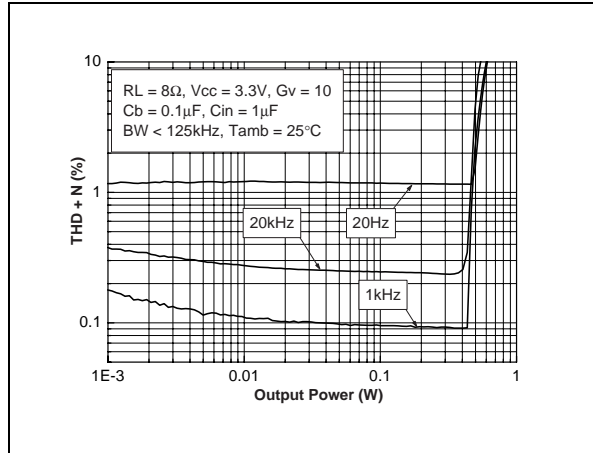


Fig. 45 : THD + N vs Output Power

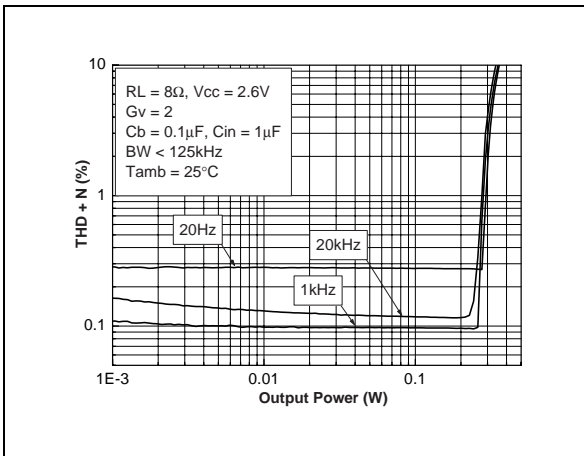


Fig. 46 : THD + N vs Output Power

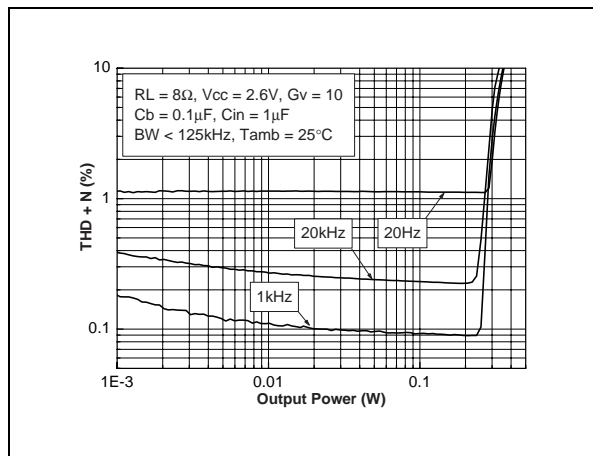


Fig. 47 : THD + N vs Output Power

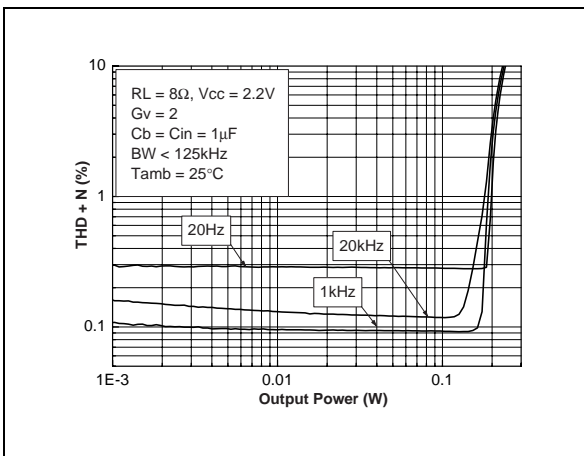


Fig. 48 : THD + N vs Output Power

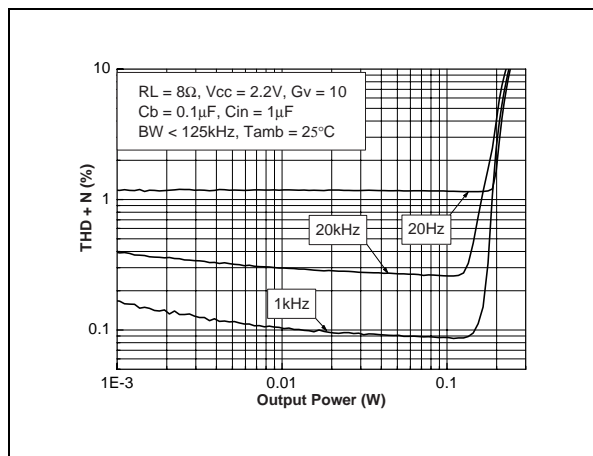


Fig. 49 : THD + N vs Output Power

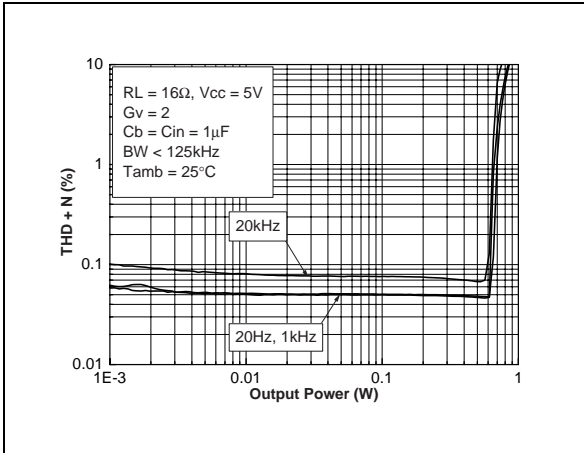


Fig. 50 : THD + N vs Output Power

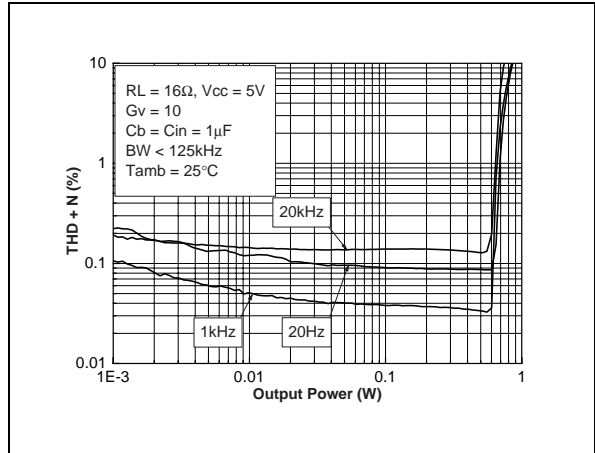


Fig. 51 : THD + N vs Output Power

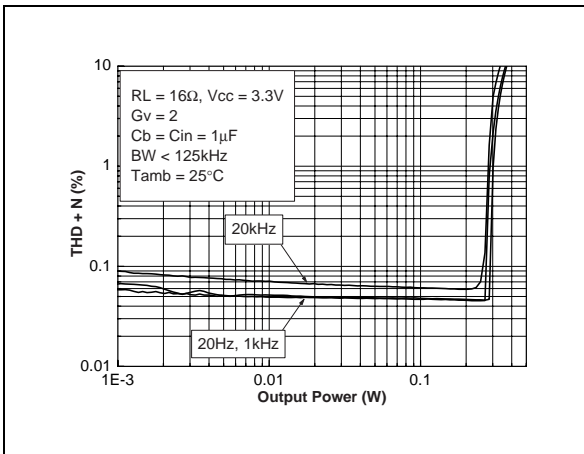


Fig. 52 : THD + N vs Output Power

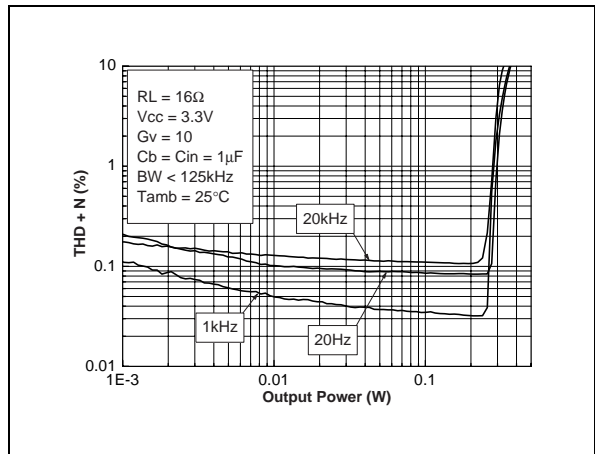


Fig. 53 : THD + N vs Output Power

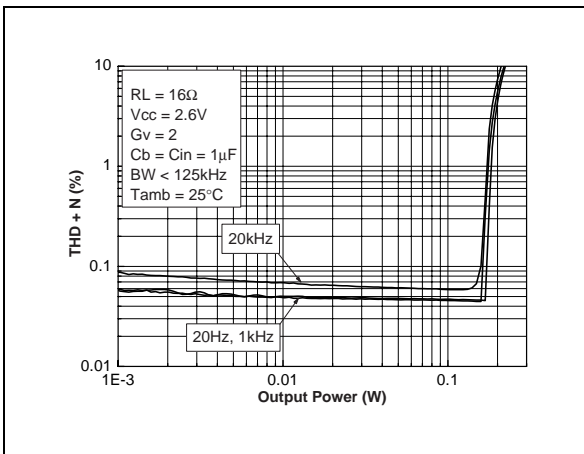


Fig. 54 : THD + N vs Output Power

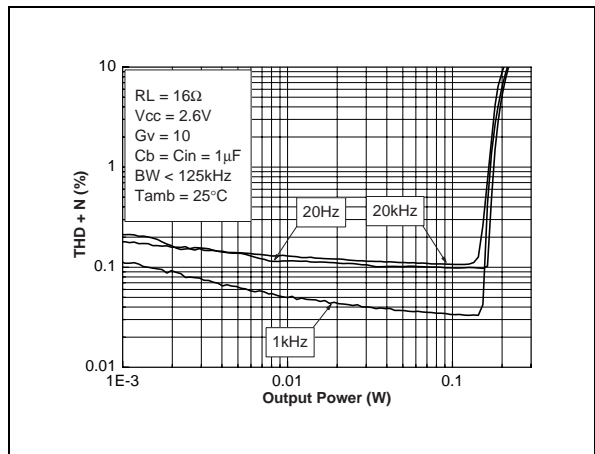


Fig. 55 : THD + N vs Output Power

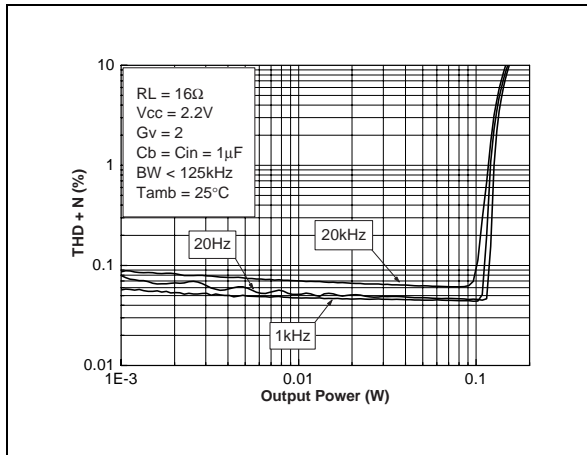


Fig. 56 : THD + N vs Output Power

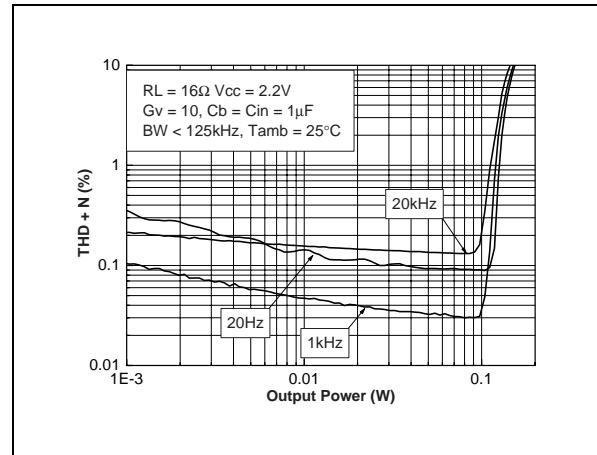


Fig. 57 : THD + N vs Frequency

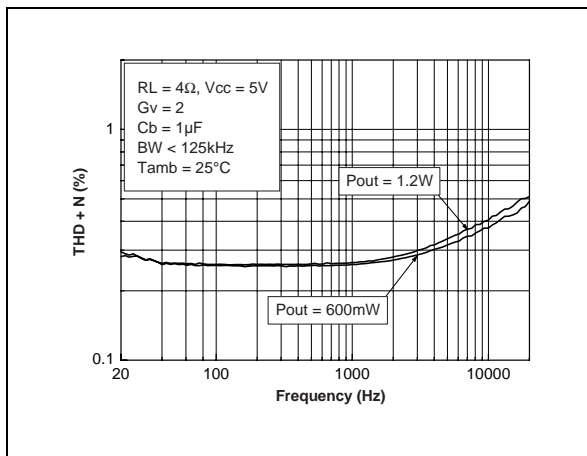


Fig. 58 : THD + N vs Frequency

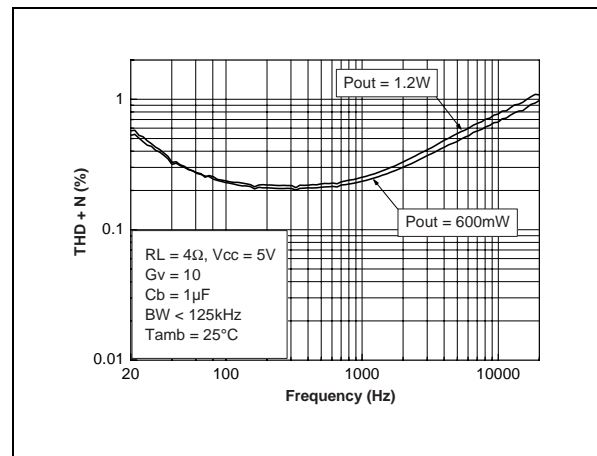


Fig. 59 : THD + N vs Frequency

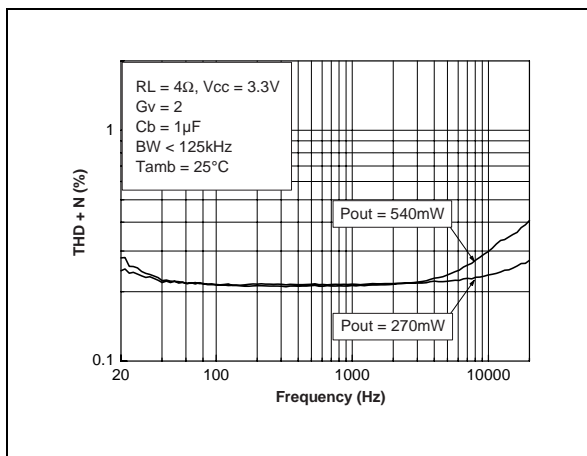


Fig. 60 : THD + N vs Frequency

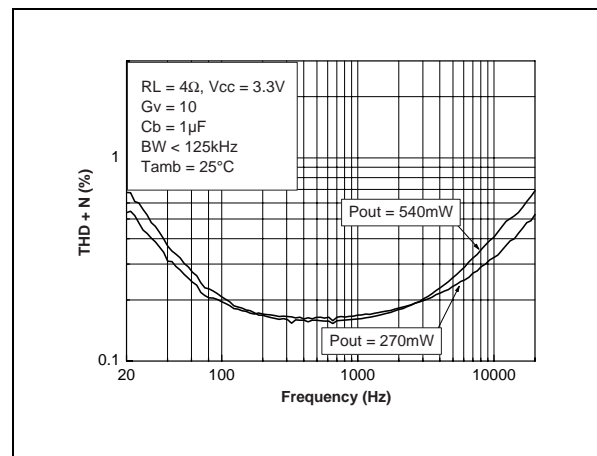


Fig. 61 : THD + N vs Frequency

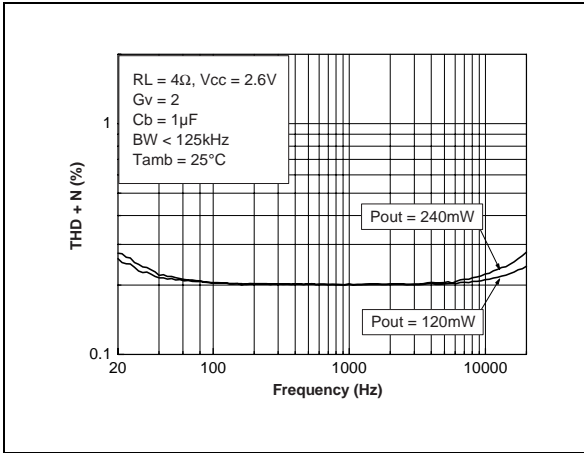


Fig. 62 : THD + N vs Frequency

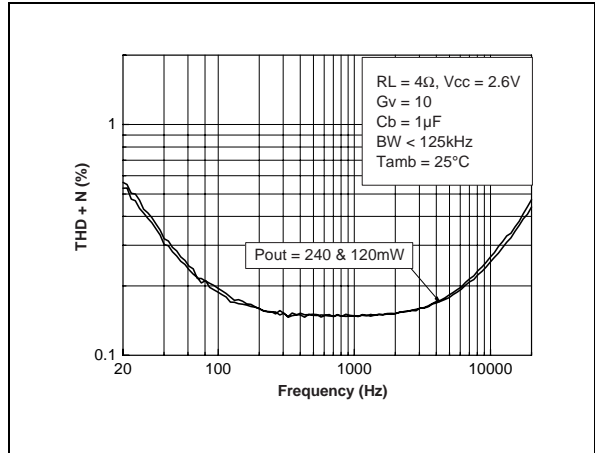


Fig. 63 : THD + N vs Frequency

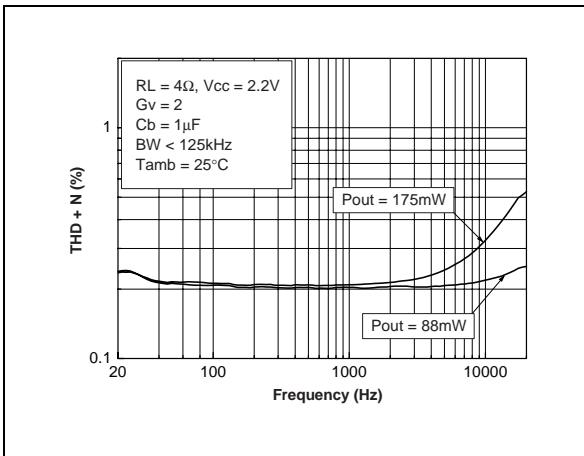


Fig. 64 : THD + N vs Frequency

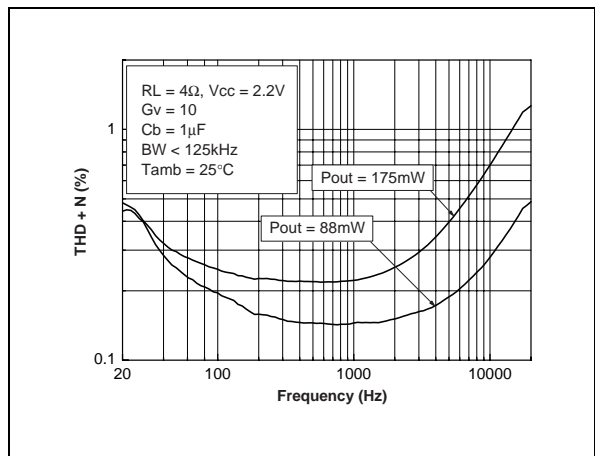


Fig. 65 : THD + N vs Frequency

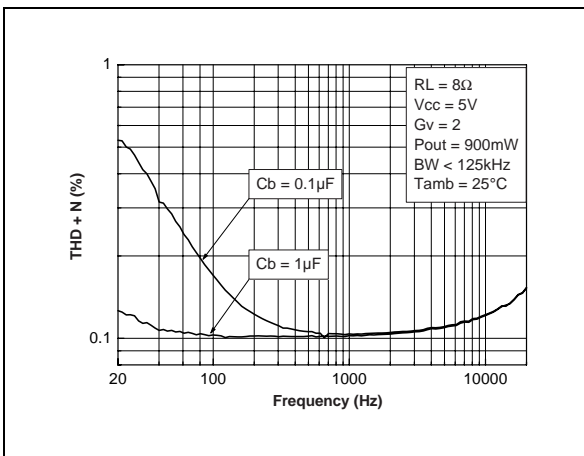


Fig. 66 : THD + N vs Frequency

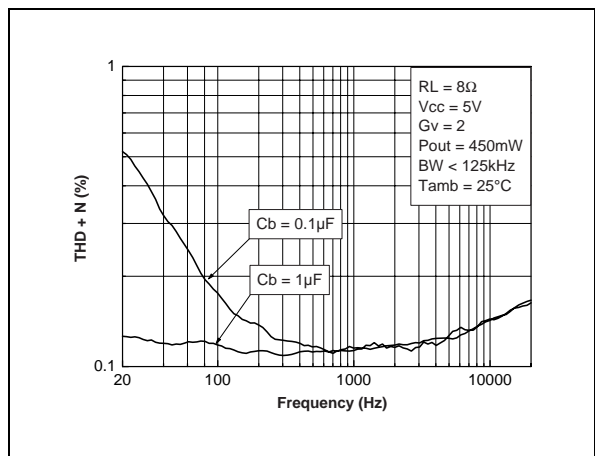


Fig. 67 : THD + N vs Frequency

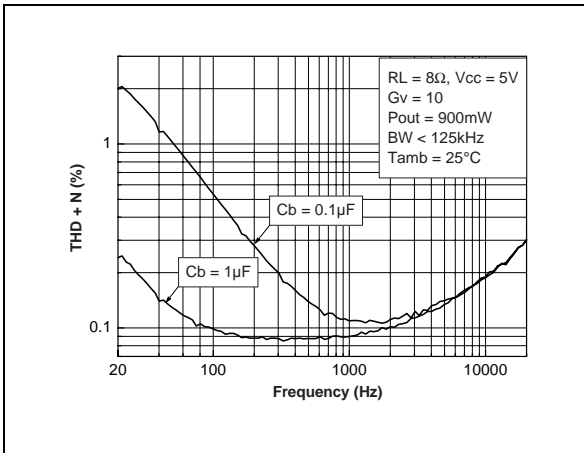


Fig. 68 : THD + N vs Frequency

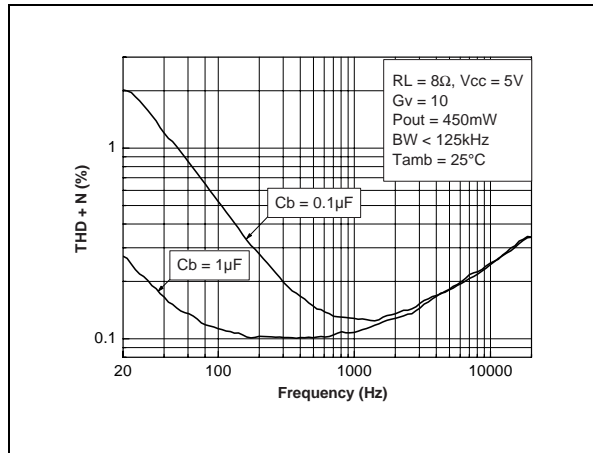


Fig. 69 : THD + N vs Frequency

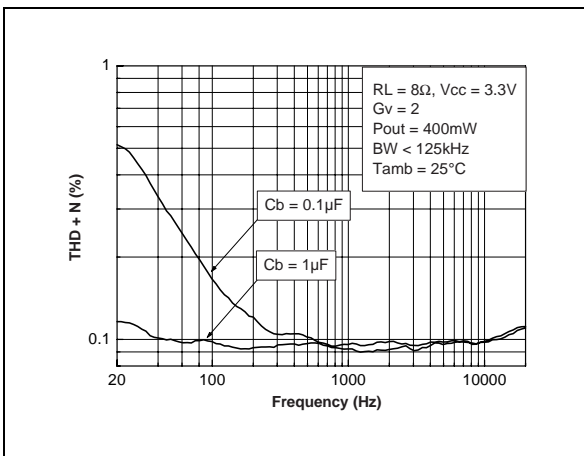


Fig. 70 : THD + N vs Frequency

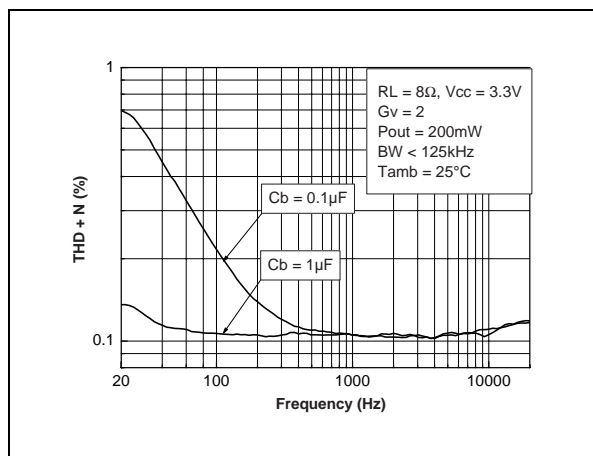


Fig. 71 : THD + N vs Frequency

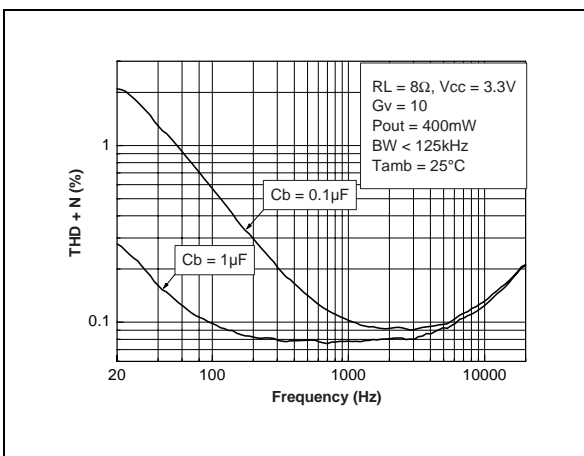


Fig. 72 : THD + N vs Frequency

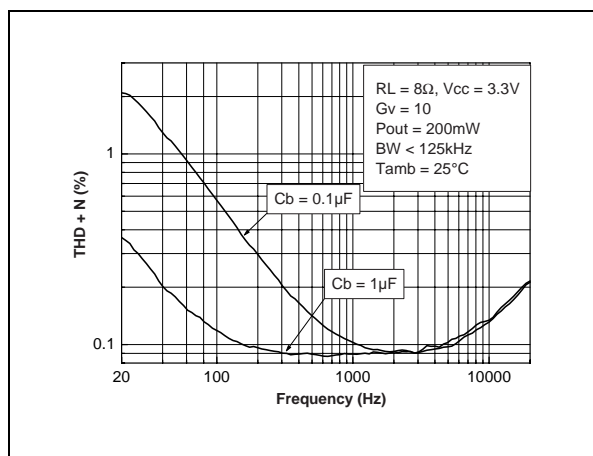


Fig. 73 : THD + N vs Frequency

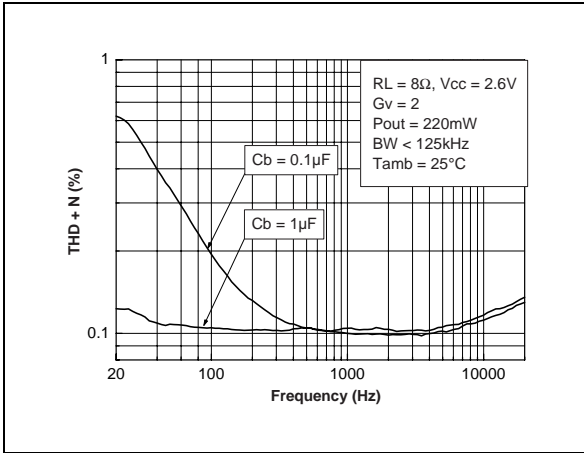


Fig. 74 : THD + N vs Frequency

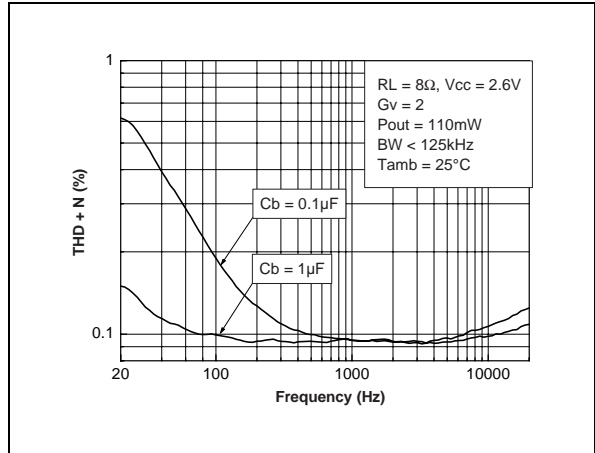


Fig. 75 : THD + N vs Frequency

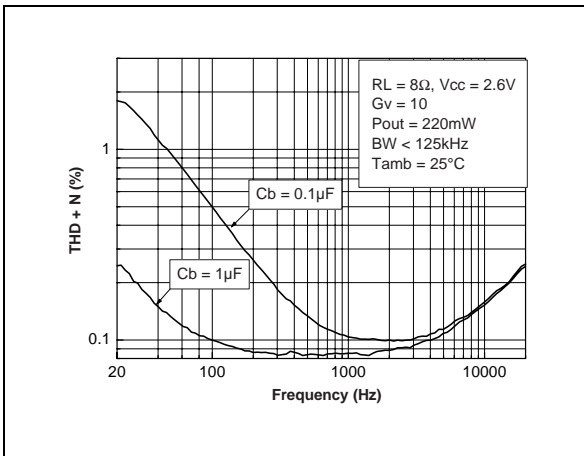


Fig. 76 : THD + N vs Frequency

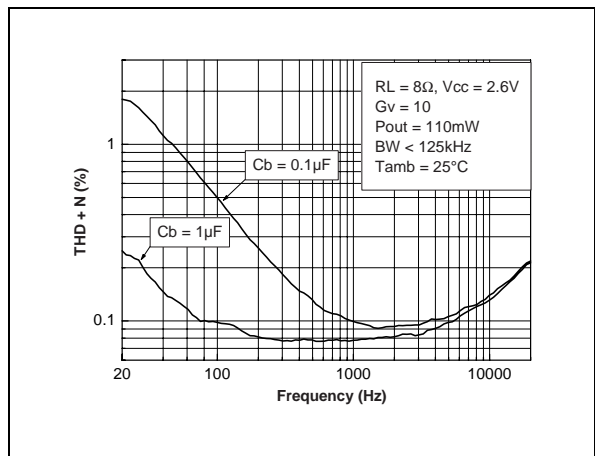


Fig. 77 : THD + N vs Frequency

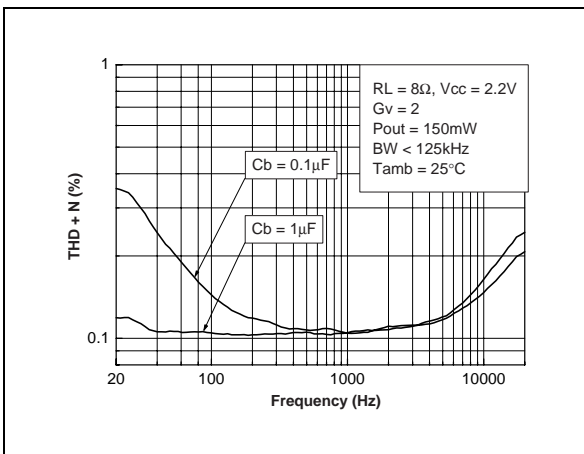


Fig. 78 : THD + N vs Frequency

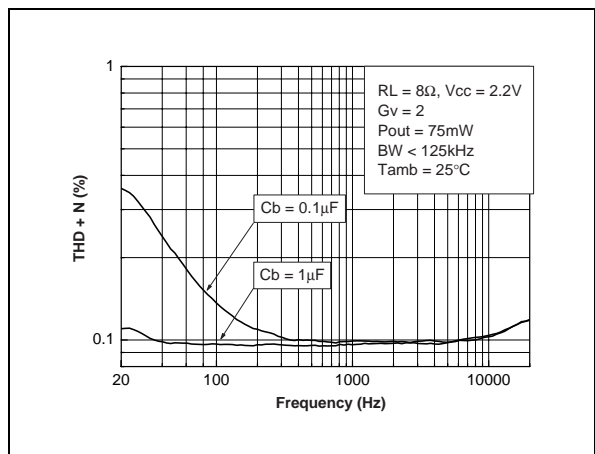


Fig. 79 : THD + N vs Frequency

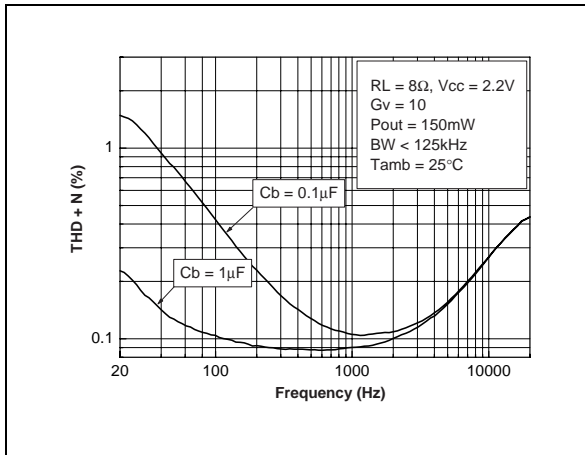


Fig. 80 : THD + N vs Frequency

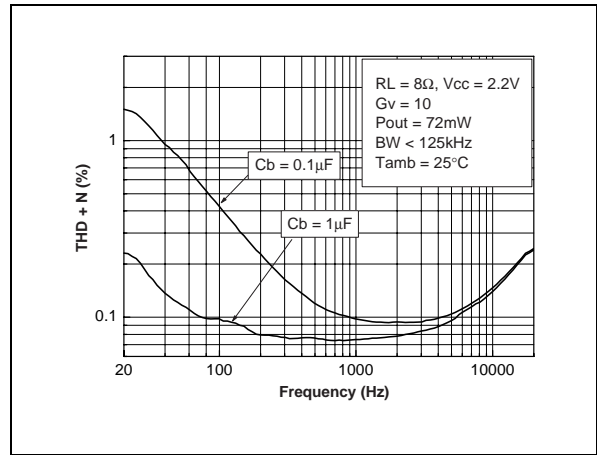


Fig. 81 : THD + N vs Frequency

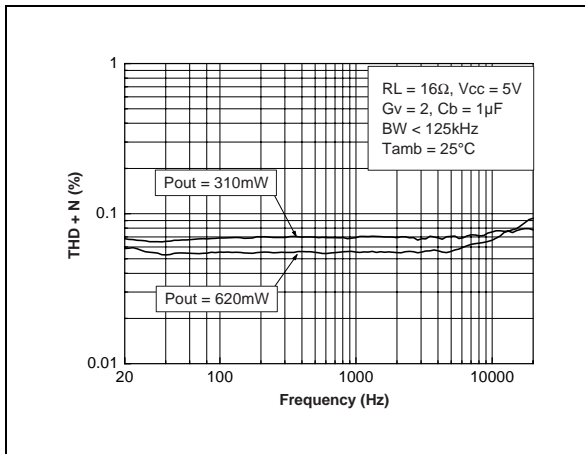


Fig. 82 : THD + N vs Frequency

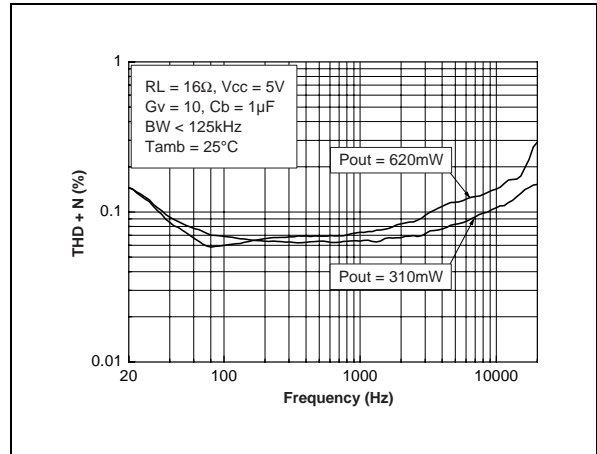


Fig. 83 : THD + N vs Frequency

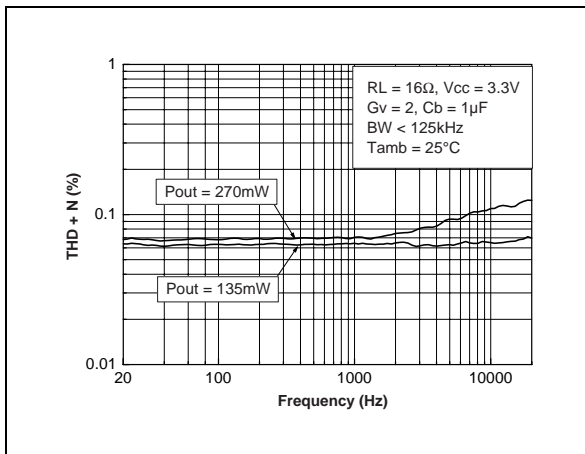


Fig. 84 : THD + N vs Frequency

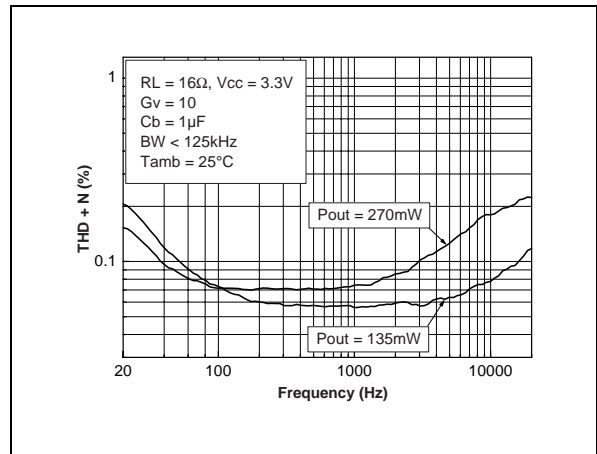


Fig. 85 : THD + N vs Frequency

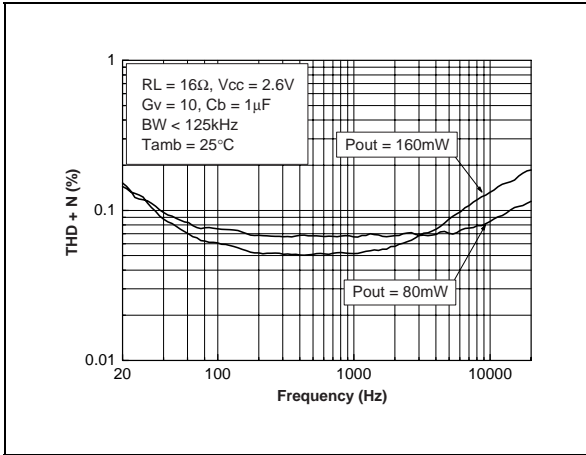


Fig. 86 : THD + N vs Frequency

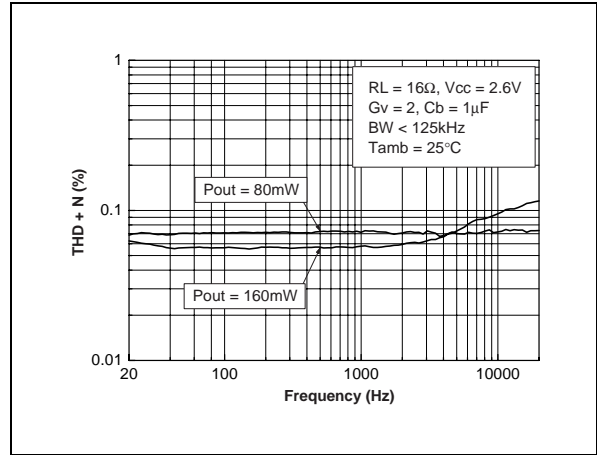


Fig. 87 : THD + N vs Frequency

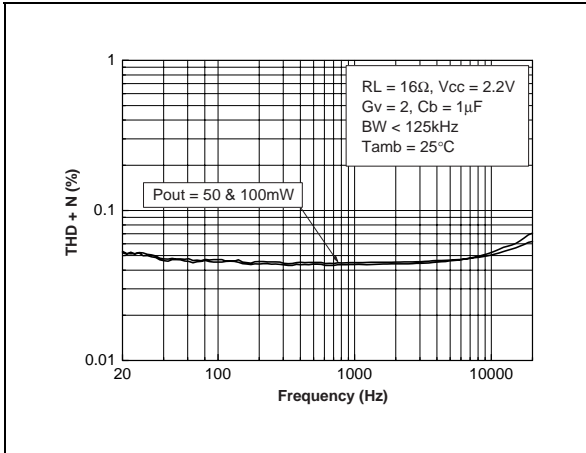


Fig. 88 : THD + N vs Frequency

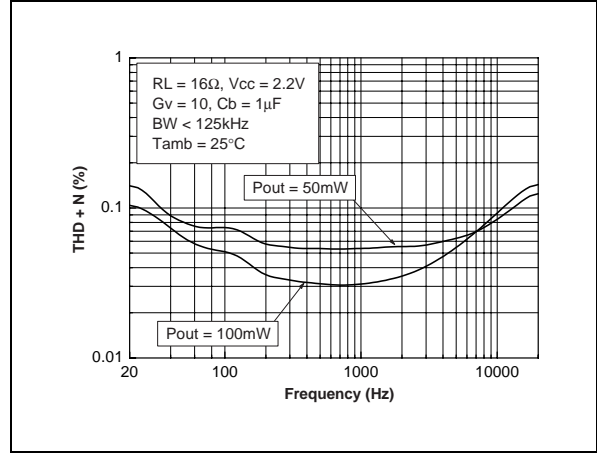


Fig. 89 : Signal to Noise Ratio vs Power Supply with Unweighted Filter (20Hz to 20kHz)

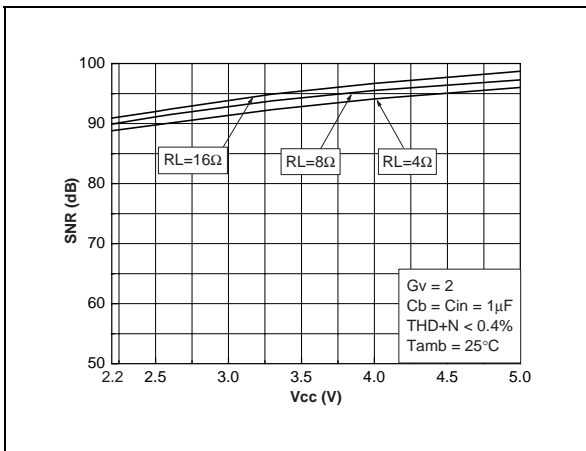


Fig. 90 : Signal to Noise Ratio Vs Power Supply with Unweighted Filter (20Hz to 20kHz)

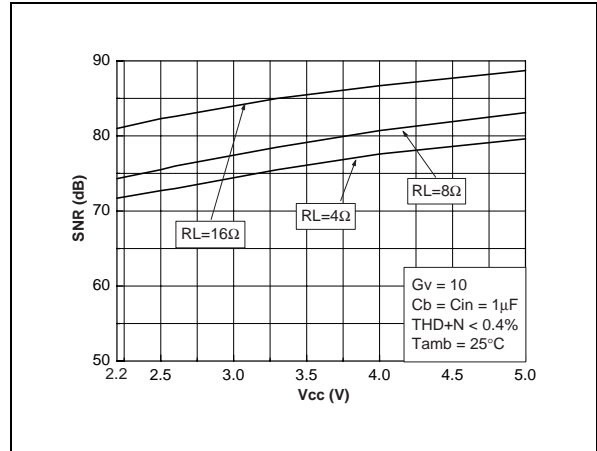


Fig. 91 : Signal to Noise Ratio vs Power Supply with Weighted Filter type A

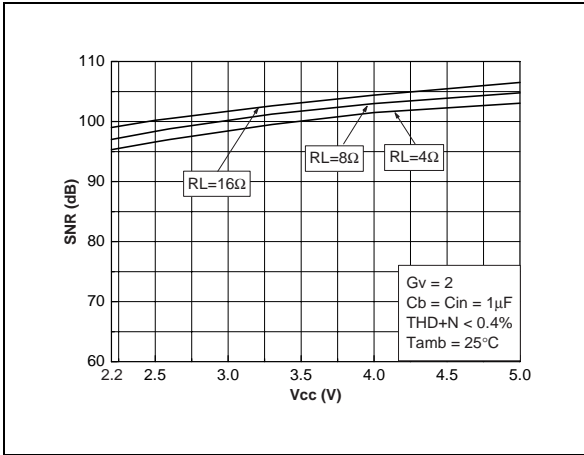


Fig. 92 : Signal to Noise Ratio vs Power Supply with Weighted Filter Type A

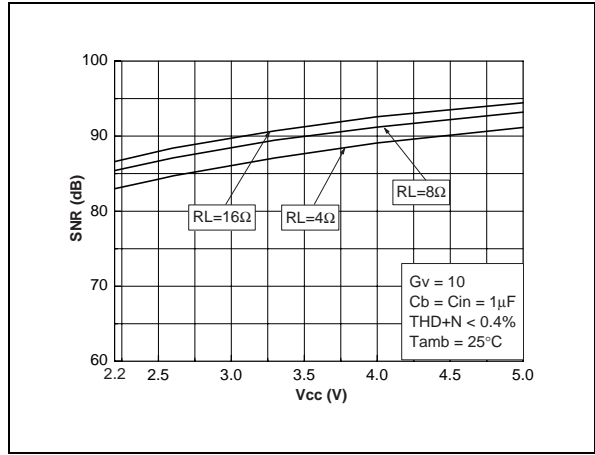


Fig. 93 : Frequency Response Gain vs Cin, & Cfeed

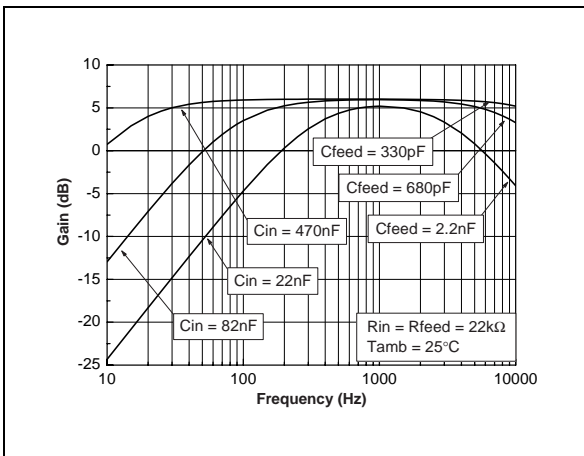


Fig. 94 : Current Consumption vs Power Supply Voltage (no load)

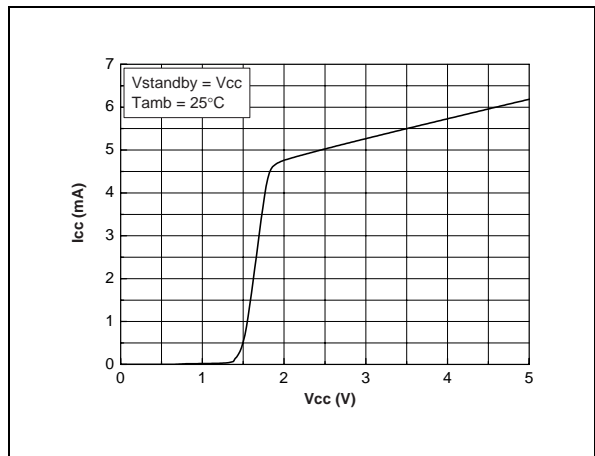


Fig. 95 : Current Consumption vs Standby Voltage @ Vcc = 5V

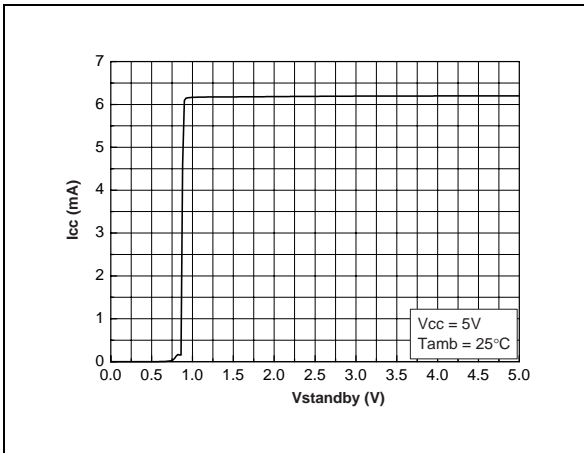


Fig. 96 : Current Consumption vs Standby Voltage @ Vcc = 3.3V

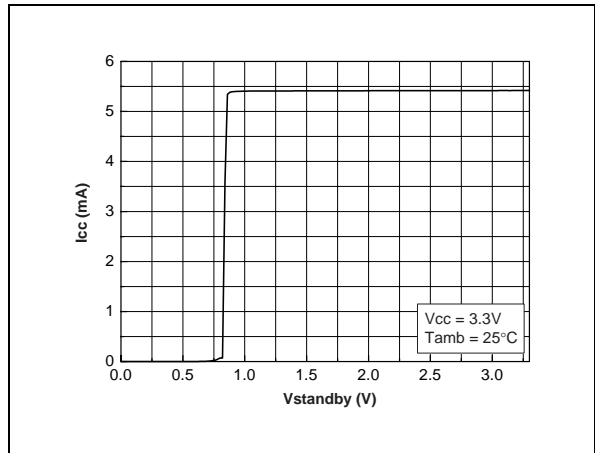


Fig. 97 : Current Consumption vs Standby Voltage @ Vcc = 2.6V

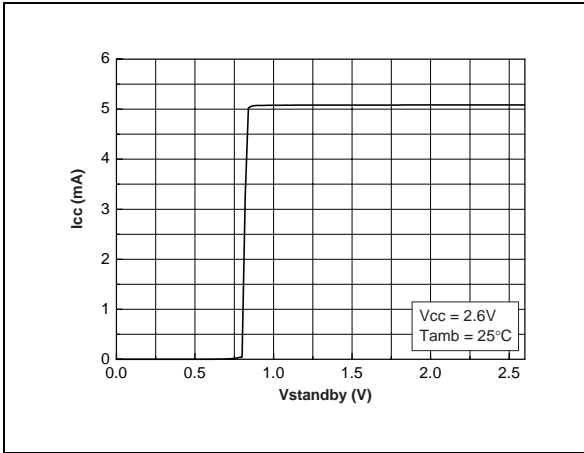


Fig. 98 : Current Consumption vs Standby Voltage @ Vcc = 2.2V

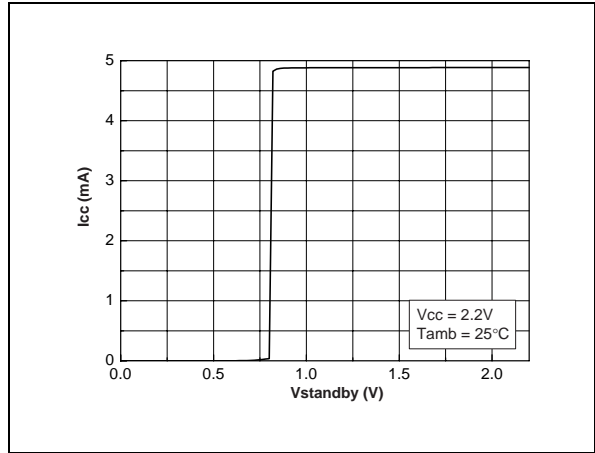


Fig. 99 : Clipping Voltage vs Power Supply Voltage and Load Resistor

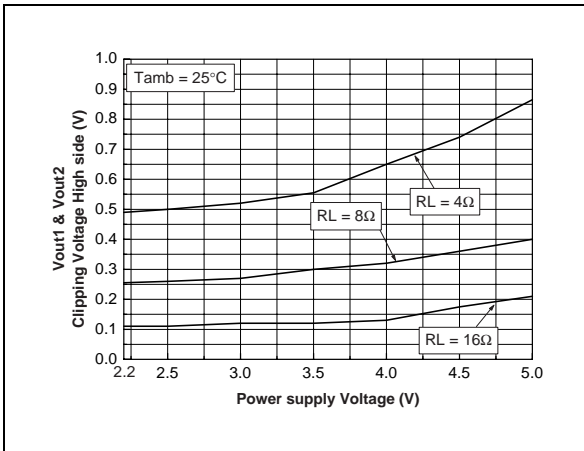
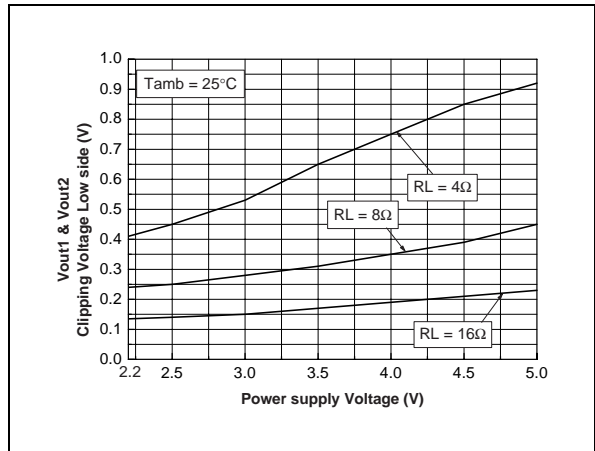


Fig. 100 : Clipping Voltage vs Power Supply Voltage and Load Resistor



APPLICATION INFORMATION

Fig. 101 : Demoboard Schematic

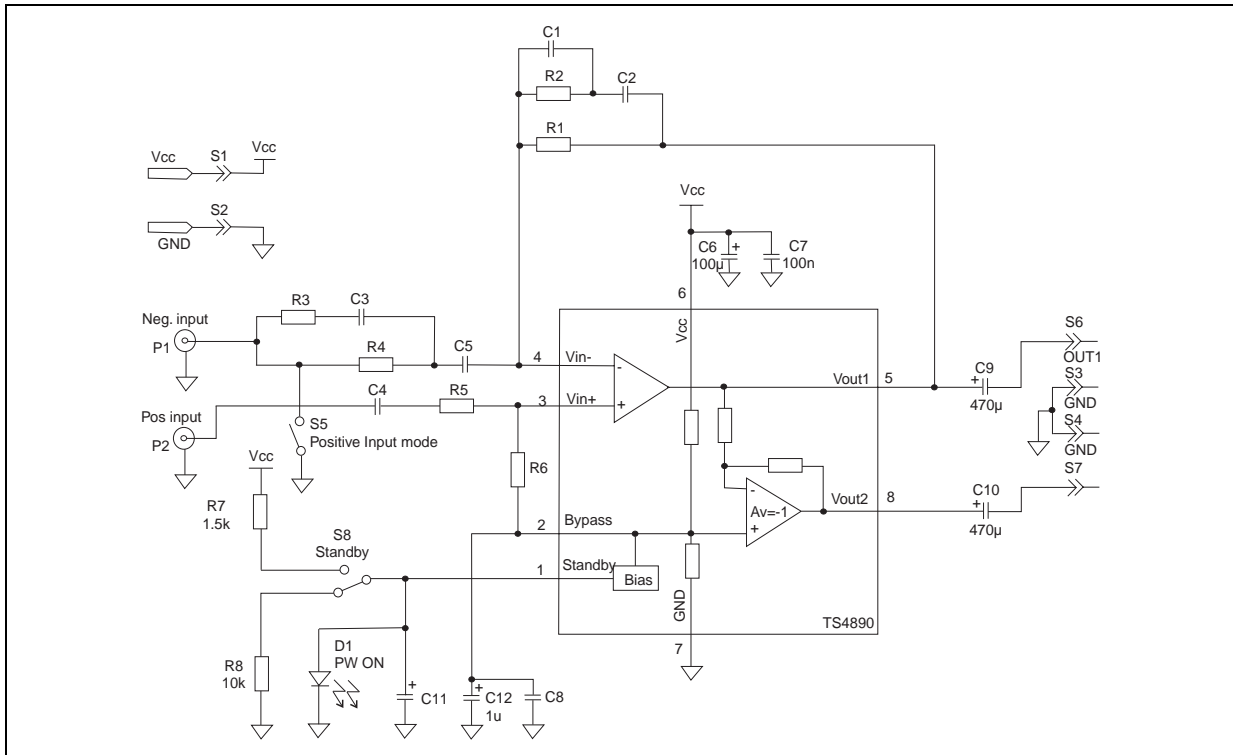


Fig. 102 : SO8 & MiniSO8 Demoboard Components Side

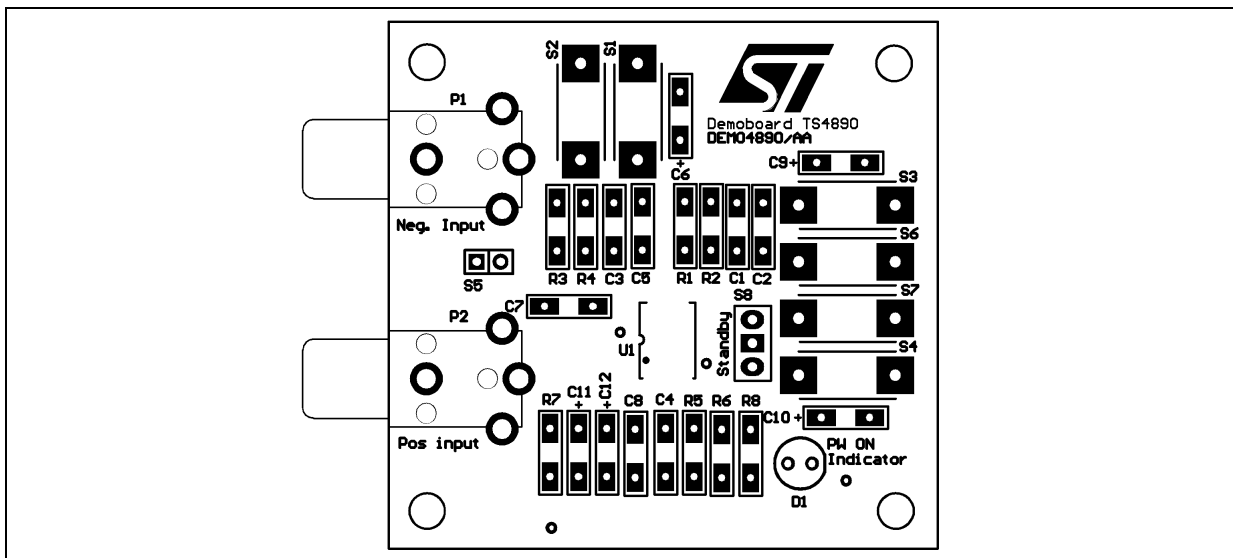


Fig. 103 : SO8 & MiniSO8 Demoboard Top Solder Layer

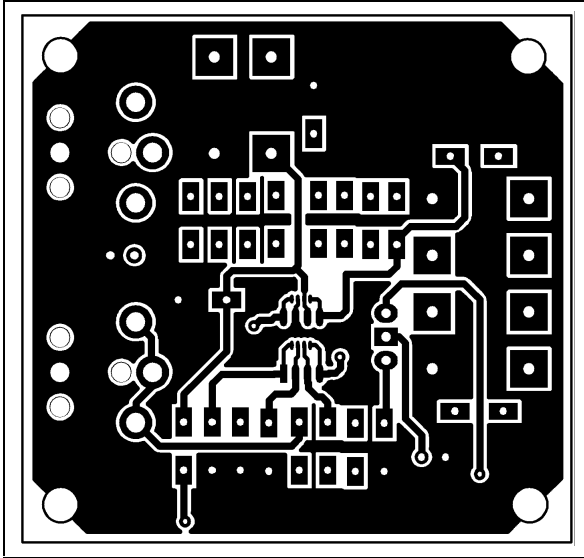
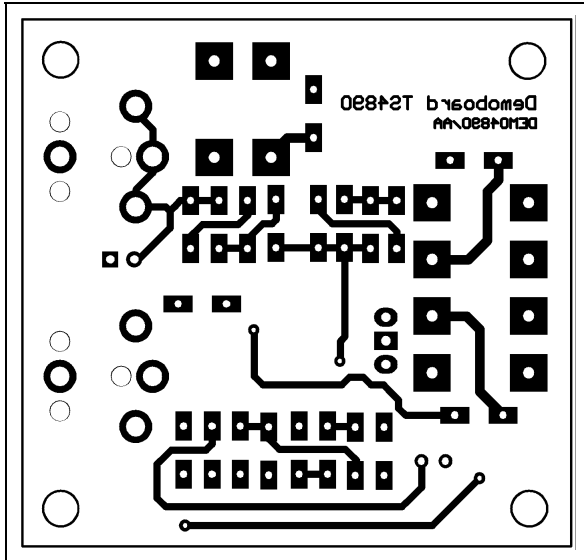


Fig. 104 : SO8 & MiniSO8 Demoboard Bottom Solder Layer



■ BTL Configuration Principle

The TS4890 is a monolithic power amplifier with a BTL output type. BTL (Bridge Tied Load) means that each end of the load are connected to two single ended output amplifiers. Thus, we have :

Single ended output 1 = $V_{out1} = V_{out}$ (V)
 Single ended output 2 = $V_{out2} = -V_{out}$ (V)

And $V_{out1} - V_{out2} = 2V_{out}$ (V)

The output power is :

$$P_{out} = \frac{(2 V_{out_{RMS}})^2}{R_L} \text{ (W)}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

■ Gain In Typical Application Schematic (cf. page 1)

In flat region (no effect of C_{in}), the output voltage of the first stage is :

$$V_{out1} = -V_{in} \frac{R_{feed}}{R_{in}} \text{ (V)}$$

For the second stage : $V_{out2} = -V_{out1}$ (V)

The differential output voltage is

$$V_{out2} - V_{out1} = 2V_{in} \frac{R_{feed}}{R_{in}} \text{ (V)}$$

The differential gain named gain (G_v) for more convenient usage is :

$$G_v = \frac{V_{out2} - V_{out1}}{V_{in}} = 2 \frac{R_{feed}}{R_{in}}$$

Remark : V_{out2} is in phase with V_{in} and V_{out1} is 180 phased with V_{in} . It means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1} .

■ Low and high frequency response

In low frequency region, the effect of C_{in} starts. C_{in} with R_{in} forms a high pass filter with a -3dB cut off frequency .

$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}} \text{ (Hz)}$$

In high frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel on R_{feed} . Its form a low pass filter with a -3dB cut off frequency .

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}} \text{ (Hz)}$$

■ **Power dissipation and efficiency**

Hypothesis :

- Voltage and current in the load are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{cc})

Regarding the load we have :

$$V_{OUT} = V_{PEAK} \sin \omega t \text{ (V)}$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} \text{ (A)}$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} \text{ (W)}$$

Then, the average current delivered by the supply voltage is

$$I_{CCAVG} = 2 \frac{V_{PEAK}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is
P_{supply} = V_{cc} I_{ccAVG} (W)

Then, the **power dissipated by the amplifier** is
P_{diss} = P_{supply} - P_{out} (W)

$$P_{diss} = \frac{2\sqrt{2} V_{cc}}{\pi\sqrt{R_L}} \sqrt{P_{OUT}} - P_{OUT} \text{ (W)}$$

and the maximum value is obtained when

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is

$$P_{dissmax} = \frac{2V_{cc}^2}{\pi^2 R_L} \text{ (W)}$$

Remark : This maximum value is only depending on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4 V_{cc}}$$

The maximum theoretical value is reached when V_{peak} = V_{cc}, so

$$\frac{\pi}{4} = 78.5\%$$

■ **Decoupling of the circuit**

Two capacitors are needed to bypass properly the TS4890. A power supply bypass capacitor C_s and a bias voltage bypass capacitor C_b.

C_s has especially an influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances. With 100µF, you can expect similar THD+N performances like shown in the datasheet.

If C_s is lower than 100µF, in high frequency increase THD+N and disturbances on the power supply rail are less filtered. To the contrary, if C_s is higher than 100µF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N in lower frequency, but its function is critical on the final result of PSRR with input grounded in lower frequency.

If C_b is lower than 1µF, THD+N increase in lower frequency (see THD+N vs frequency curves) and the PSRR worsens up. If C_b is higher than 1µF, the benefit on THD+N in lower frequency is small but the benefit on PSRR is substantial (see PSRR vs. C_b curves).

Note that C_{in} has a non-negligible effect on PSRR in lower frequency. Lower is its value, higher is the PSRR (see fig. 13).

■ **Pop and Click performance**

In order to have the best performances with the pop and click circuitry, the formula below must be follow :

$$\tau_{in} \leq \tau_b$$

With

$$\tau_{in} = (R_{in} + R_{feed}) \times C_{in} \text{ (s)}$$

and

$$\tau_b = 50k\Omega \times C_b \text{ (s)}$$

■ Power amplifier design examples

Given :

- Load impedance : 8Ω
- Output power @ 1% THD+N : 0.5W
- Input impedance : 10kΩ min.
- Input voltage peak to peak : 1Vpp
- Bandwidth frequency : 20Hz to 20kHz (0, -3dB)
- THD+N in 20Hz to 20kHz < 0.5% @Pout=0.45W
- Ambient temperature max = 50°C
- SO8 package

First of all, we must calculate the minimum power supply voltage to obtain 0.5W into 8Ω. See curves in fig. 15, we can read 3.5V. Thus, the power supply voltage value min. will be 3.5V.

Following the maximum power dissipation equation :

$$P_{dissmax} = \frac{2V_{cc}^2}{\pi^2 R_L} \text{ (W)}$$

with 3.5V we have P_{dissmax}=0.31W.

Refer to power derating curves (fig. 24), with 0.31W the maximum ambient temperature will be 100°C. This last value could be higher if you follow the example layout shows on the demoboard (better dissipation).

The gain of the amplifier in flat region will be :

$$G_V = \frac{V_{OUTPP}}{V_{INPP}} = \frac{2\sqrt{2R_L P_{OUT}}}{V_{INPP}} = 5.65$$

We have Rin > 10kΩ. Let's take Rin = 10kΩ, then R_{feed} = 28.25kΩ. We could use for R_{feed} = 30kΩ in normalized value and the gain will be G_v = 6.

In lower frequency we want 20 Hz (-3dB cut off frequency). Then

$$C_{IN} = \frac{1}{2\pi R_{in} F_{CL}} = 795nF$$

So, we could use for C_{in} a 1μF capacitor value that gives 16Hz.

In Higher frequency we want 20kHz (-3dB cut off frequency). The Gain Bandwidth Product of the TS4890 is 2MHz typical and doesn't change when the amplifier delivers power into the load.

The first amplifier has a gain of

$$\frac{R_{feed}}{R_{in}} = 3$$

and the theoretical value of the -3dB cut of higher frequency is 2MHz/3 = 660kHz.

We can keep this value or limiting the bandwidth by adding a capacitor C_{feed}, in parallel on R_{feed}. Then

$$C_{FEED} = \frac{1}{2\pi R_{FEED} F_{CH}} = 265pF$$

So, we could use for C_{feed} a 220pF capacitor value that gives 24kHz.

Now, we can choose the value of C_b with the constraint THD+N in 20Hz to 20kHz < 0.5% @ Pout=0.45W. If you refer to the closest THD+N vs frequency measurement : fig. 71 (V_{cc}=3.3V, G_v=10), with C_b = 1μF, the THD+N vs frequency is always below 0.4%. As the behaviour is the same with V_{cc} = 5V (fig. 67), V_{cc} = 2.6V (fig. 67). As the gain for these measurements is higher (worst case), we can consider with C_b = 1μF, V_{cc} = 3.5V and G_v = 6, that the THD+N in 20Hz to 20kHz range with Pout = 0.45W will be lower than 0.4%.

In the following tables, you could find three another examples with values required for the demoboard.

Remark : components with (*) marking are optional.

Application n°1 : 20Hz to 20kHz bandwidth and 6dB gain BTL power amplifier.

Components :

| Designator | Part Type |
|------------|---|
| R1 | 22k / 0.125W |
| R4 | 22k / 0.125W |
| R6 | Short Circuit |
| R7* | (V _{cc} -V _{f_led})/I _{f_led} |
| R8 | 10k / 0.125W |
| C5 | 470nF |
| C6 | 100μF |

| Designator | Part Type |
|----------------|-------------------------------------|
| C7 | 100nF |
| C9 | Short Circuit |
| C10 | Short Circuit |
| C12 | 1µF |
| S1, S2, S6, S7 | 2mm insulated Plug 10.16mm pitch |
| S8 | 3 pts connector 2.54mm pitch |
| P1 | PCB Phono Jack |
| D1* | Led 3mm |
| U1 | TS4890ID or TS4890IS |

Application n°2 : 20Hz to 20kHz bandwidth and 20dB gain BTL power amplifier.

Components :

| Designator | Part Type |
|----------------|-------------------------------------|
| R1 | 110k / 0.125W |
| R4 | 22k / 0.125W |
| R6 | Short Circuit |
| R7* | (Vcc-Vf_led)/If_led |
| R8 | 10k / 0.125W |
| C5 | 470nF |
| C6 | 100µF |
| C7 | 100nF |
| C9 | Short Circuit |
| C10 | Short Circuit |
| C12 | 1µF |
| S1, S2, S6, S7 | 2mm insulated Plug 10.16mm pitch |
| S8 | 3 pts connector 2.54mm pitch |
| P1 | PCB Phono Jack |
| D1* | Led 3mm |
| U1 | TS4890ID or TS4890IS |

Application n°3 : 50Hz to 10kHz bandwidth and 10dB gain BTL power amplifier.

Components :

| Designator | Part Type |
|----------------|-------------------------------------|
| R1 | 33k / 0.125W |
| R2 | Short Circuit |
| R4 | 22k / 0.125W |
| R6 | Short Circuit |
| R7* | (Vcc-Vf_led)/If_led |
| R8 | 10k / 0.125W |
| C2 | 470pF |
| C5 | 150nF |
| C6 | 100µF |
| C7 | 100nF |
| C9 | Short Circuit |
| C10 | Short Circuit |
| C12 | 1µF |
| S1, S2, S6, S7 | 2mm insulated Plug 10.16mm pitch |
| S8 | 3 pts connector 2.54mm pitch |
| P1 | PCB Phono Jack |
| D1* | Led 3mm |
| U1 | TS4890ID or TS4890IS |

Application n°4 : Differential inputs BTL power amplifier.

In this configuration, we need to place these components : R1, R4, R5, R6, R7, C4, C5, C12.

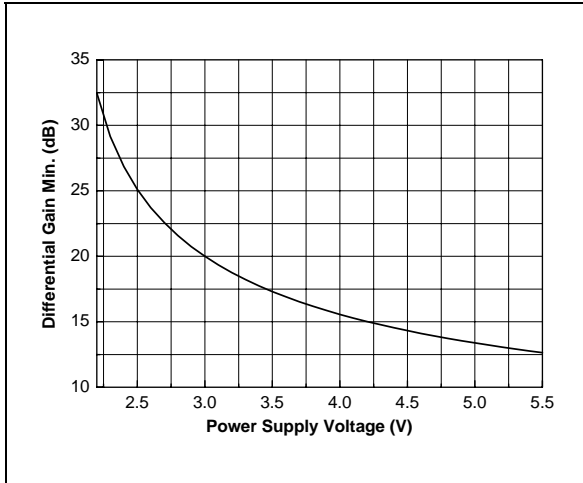
We have also : R4 = R5, R1 = R6, C4 = C5.

The gain of the amplifier is:

$$G_{VDIFF} = 2 \frac{R1}{R4}$$

Note : Due to the VICM range (see Operating Condition), GVDIFF must have a minimum value shown in figure 105.

Fig. 105 : Minimum Differential Gain vs Power Supply Voltage



For Vcc=5V, a 20Hz to 20kHz bandwidth and 20dB gain BTL power amplifier you could follow the bill of material below.

| Designator | Part Type |
|----------------|-------------------------------------|
| C5 | 470nF |
| C6 | 100µF |
| C7 | 100nF |
| C9 | Short Circuit |
| C10 | Short Circuit |
| C12 | 1µF |
| D1* | Led 3mm |
| S1, S2, S6, S7 | 2mm insulated Plug 10.16mm pitch |
| S8 | 3 pts connector 2.54mm pitch |
| P1, P2 | PCB Phono Jack |
| U1 | TS4890ID or TS4890IS |

Components :

| Designator | Part Type |
|------------|----------------------------------|
| R1 | 110k / 0.125W |
| R4 | 22k / 0.125W |
| R5 | 22k / 0.125W |
| R6 | 110k / 0.125W |
| R7* | $(V_{cc}-V_{f_led})/I_{f_led}$ |
| R8 | 10k / 0.125W |
| C4 | 470nF |

■ Note on how to use the PSRR curves (page 8)

We have finished a design and we have chosen for the components :

- Rin=Rfeed=22kΩ
- Cin=100nF
- Cb=1μF

Now, on fig. 16, we can see the PSRR (input grounded) vs frequency curves. At 217Hz, we have a PSRR value of -36dB.

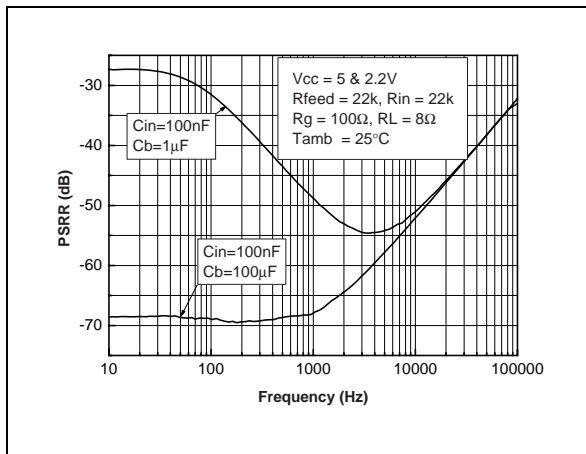
In reality we want a value about -70dB. So, we need a gain of 34dB !

Now, on fig. 15 we can see the effect of Cb on the PSRR (input grounded) vs. frequency. With Cb=100μF, we can reach the -70dB value.

The process to obtain the final curve (Cb=100μF, Cin=100nF, Rin=Rfeed=22kΩ) is a simple transfer point by point on each frequency of the curve on fig. 16 to the curve on fig. 15.

The measurement result is shown on the next figure.

Fig. 106 : PSRR changes with Cb



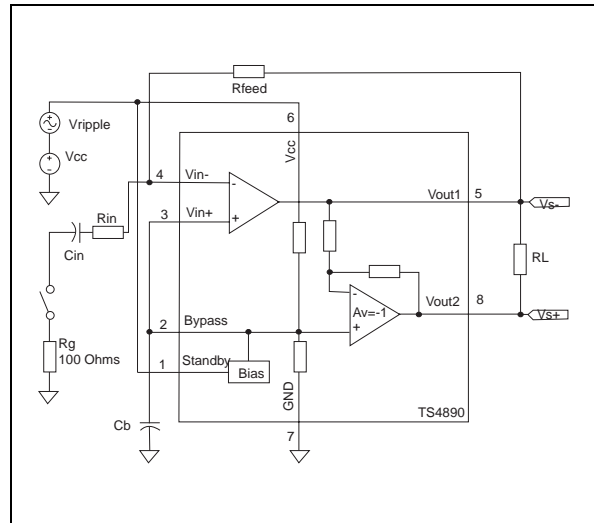
■ Note on PSRR measurement

What is the PSRR ?

The PSRR is the Power Supply Rejection Ratio. It's a kind of SVR in a determined frequency range. The PSRR of a device, is the ratio between a power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

How do we measure the PSRR ?

Fig. 107 : PSRR measurement schematic



■ Principle of operation

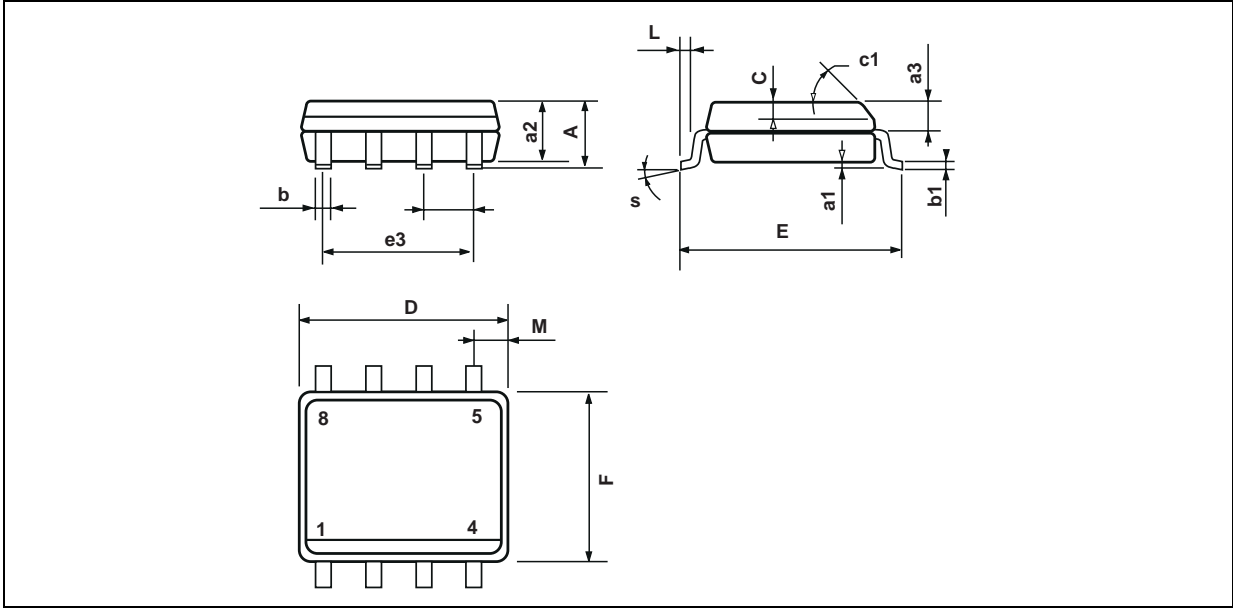
- We fixed the DC voltage supply (Vcc)
- We fixed the AC sinusoidal ripple voltage (Vripple)
- No bypass capacitor Cs is used

The PSRR value for each frequency is :

$$PSRR(dB) = 20 \times \text{Log}_{10} \left[\frac{Rms(V_{ripple})}{Rms(V_{s+} - V_{s-})} \right]$$

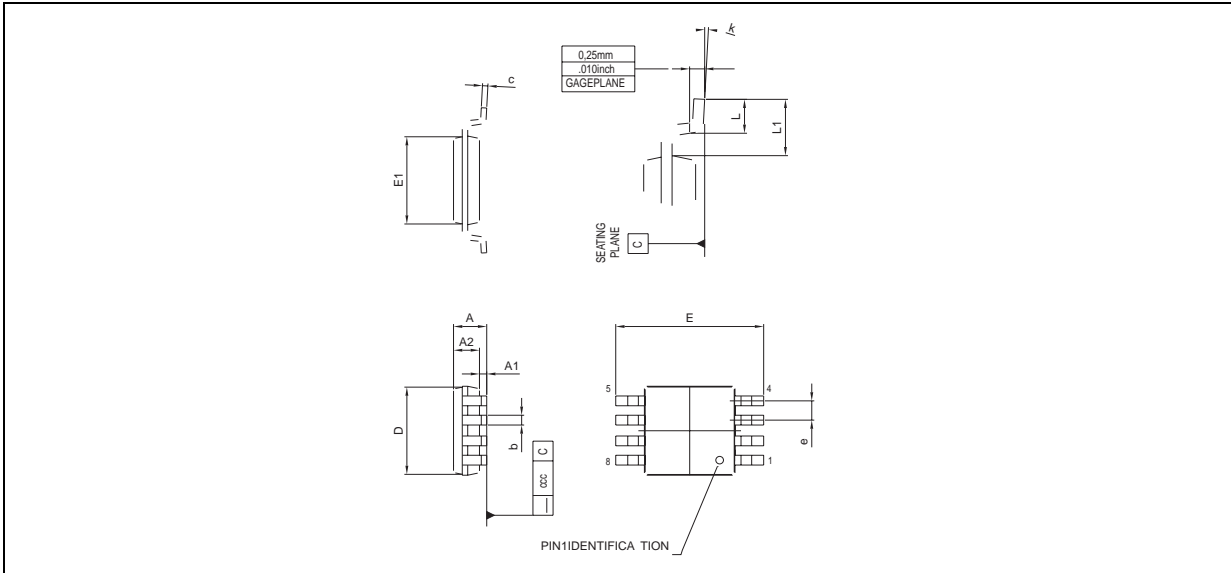
Remark : The measure of the Rms voltage is not a Rms selective measure but a full range (2 Hz to 125 kHz) Rms measure. It means that we measure the effective Rms signal + the noise.

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



| Dim. | Millimeters | | | Inches | | |
|------|-------------|------|------|--------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.65 | | | 0.065 |
| a3 | 0.65 | | 0.85 | 0.026 | | 0.033 |
| b | 0.35 | | 0.48 | 0.014 | | 0.019 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | 0.25 | | 0.5 | 0.010 | | 0.020 |
| c1 | 45° (typ.) | | | | | |
| D | 4.8 | | 5.0 | 0.189 | | 0.197 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F | 3.8 | | 4.0 | 0.150 | | 0.157 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| M | | | 0.6 | | | 0.024 |
| S | 8° (max.) | | | | | |

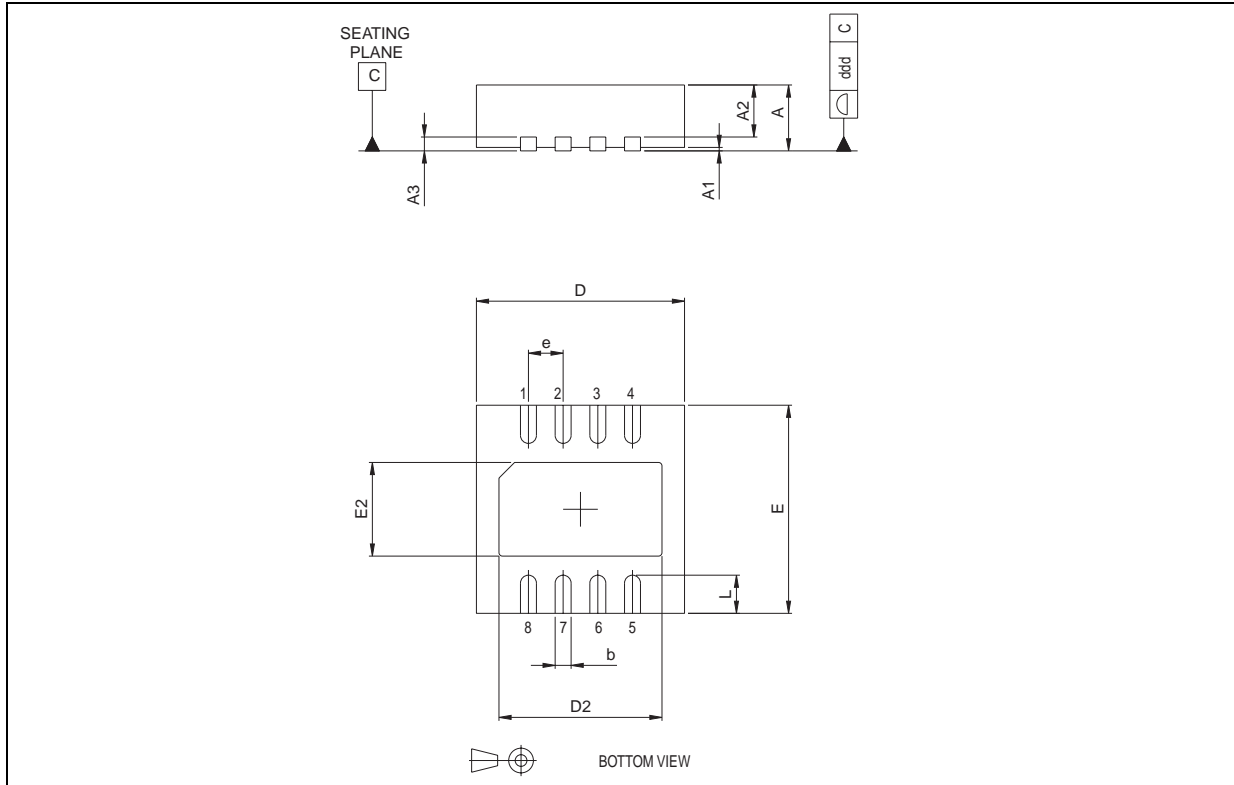
PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (miniSO8)



| Dim. | Millimeters | | | Inches | | |
|------|-------------|-------|-------|--------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.100 | | | 0.043 |
| A1 | 0.050 | 0.100 | 0.150 | 0.002 | 0.004 | 0.006 |
| A2 | 0.780 | 0.860 | 0.940 | 0.031 | 0.034 | 0.037 |
| b | 0.250 | 0.330 | 0.400 | 0.010 | 0.013 | 0.016 |
| c | 0.130 | 0.180 | 0.230 | 0.005 | 0.007 | 0.009 |
| D | 2.900 | 3.000 | 3.100 | 0.114 | 0.118 | 0.122 |
| E | 4.750 | 4.900 | 5.050 | 0.187 | 0.193 | 0.199 |
| E1 | 2.900 | 3.000 | 3.100 | 0.114 | 0.118 | 0.122 |
| e | | 0.650 | | | 0.026 | |
| L | 0.400 | 0.550 | 0.700 | 0.016 | 0.022 | 0.028 |
| L1 | | 0.950 | | | 0.037 | |
| k | 0d | 3d | 6d | 0d | 3d | 6d |
| aaa | | | 0.100 | | | 0.004 |

PACKAGE MECHANICAL DATA

8 CONNECTIONS - Dual Micro Leadframe Package (QFN8)



| Dimensions | Millimeters | | |
|------------|-------------|------|------|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | | 0.02 | 0.05 |
| A2 | | 0.70 | |
| A3 | | 0.20 | |
| b | 0.18 | 0.23 | 0.30 |
| D | | 3.00 | |
| D2 | 2.20 | 2.35 | 2.45 |
| E | | 3.00 | |
| E2 | 1.20 | 1.35 | 1.45 |
| e | | 0.50 | |
| L | 0.45 | 0.55 | 0.65 |
| ddd | | | 0.08 |

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