



TS4902

300mW at 3.3V SUPPLY AUDIO POWER AMPLIFIER WITH STANDBY MODE ACTIVE LOW

- OPERATING FROM $V_{CC} = 2.2V$ to $5.5V$
- **0.7W** OUTPUT POWER @ $V_{CC}=5V$, THD=1%,
 $f=1kHz$, with an 8Ω load
- **0.3W** OUTPUT POWER @ $V_{CC}=3.3V$,
THD=1%, $f=1kHz$, with an 8Ω load
- ULTRA LOW CONSUMPTION IN STANDBY
MODE (**10nA**)
- **77dB** PSRR @ 217Hz from 5V to 2.2V
- ULTRA LOW POP & CLICK
- ULTRA LOW DISTORTION (**0.1%**)
- UNITY GAIN STABLE
- AVAILABLE IN **MiniSO8 & SO8**

DESCRIPTION

The TS4902 is an audio power amplifier designed to provide the best price to power ratio while preserving high audio quality.

Available in MiniSO8 & SO8 package, it is capable of delivering up to 0.7W of continuous RMS output power into an 8Ω load @ 5V.

TS4902 is also exhibiting an outstanding 0.1% distortion level (THD) from a 5V supply for a P_{out} of 200mW RMS.

An externally controlled standby mode reduces the supply current to less than 10nA. It also includes an internal thermal shutdown protection.

The unity-gain stable amplifier can be configured by external gain setting resistors.

APPLICATIONS

- Mobile Phones (Cellular / Cordless)
- PDAs
- Portable Audio Devices

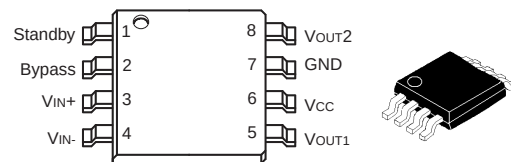
ORDER CODE

Part Number	Temperature Range	Package	
		ST	D
TS4902IST	-40, +85°C	•	
TS4902ID			•

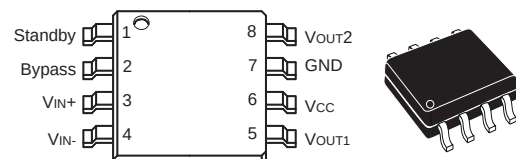
S = MiniSO Package (MiniSO) is only available in Tape & Reel (ST)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)

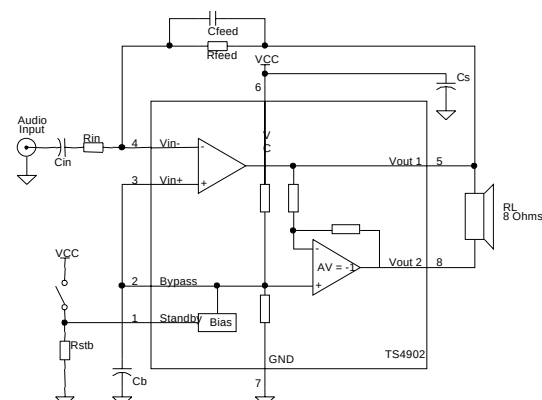
TS4902IS-TS4902IST - MiniSO8



TS4902ID-TS4902IDT - SO8



TYPICAL APPLICATION SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ¹⁾	6	V
V_i	Input Voltage ²⁾	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient ³⁾ SO8 MiniSO8	175 215	°C/W
P_d	Power Dissipation ⁴⁾	See the power derating curves Fig 20.	
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
Latch-up	Latch-up Immunity	Class A	
	Lead Temperature (soldering, 10sec)	250	°C

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed $V_{CC} + 0.3V$ / $G_{ND} - 0.3V$
3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4. Exceeding the power derating curves during a long period, will cause abnormal operation.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.2 to 5.5	V
V_{ICM}	Common Mode Input Voltage Range	G_{ND} to $V_{CC} - 1.5V$	V
V_{STB}	Standby Voltage Input : Device ON Device OFF	$1.5 \leq V_{STB} \leq V_{CC}$ $G_{ND} \leq V_{STB} \leq 0.5$	V
R_L	Load Resistor	4 - 32	Ω
R_{thja}	Thermal Resistance Junction to Ambient ¹⁾ SO8 MiniSO8	150 190	°C/W

1. This thermal resistance can be reduced with a suitable PCB layout (see Power Derating Curves)

ELECTRICAL CHARACTERISTICS

$V_{CC} = +5V$, GND = 0V, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current ¹⁾ No input signal, Vstdby = GND, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
P_O	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$		0.7		W
THD + N	Total Harmonic Distortion + Noise $P_O = 250mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$		0.15		%
PSRR	Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, Vripple = 200mV rms		77		dB
Φ_M	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when Vstdby is tied to GND

2. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is the surimposed sinus signal to V_{CC} @ $f = 217Hz$

$V_{CC} = +3.3V$, GND = 0V, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)³⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current ¹⁾ No input signal, Vstdby = GND, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
P_O	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$		300		mW
THD + N	Total Harmonic Distortion + Noise $P_O = 250mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$		0.15		%
PSRR	Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, Vripple = 200mV rms		77		dB
Φ_M	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when Vstdby is tied to GND

2. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is the surimposed sinus signal to V_{CC} @ $f = 217Hz$

3. All electrical values are made by correlation between 2.6V and 5V measurements

ELECTRICAL CHARACTERISTICS

$V_{CC} = 2.6V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current ¹⁾ No input signal, $V_{stdby} = GND$, $R_L = 8\Omega$		10	1000	nA
V_{OO}	Output Offset Voltage No input signal, $R_L = 8\Omega$		5	20	mV
P_o	Output Power THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$		180		mW
THD + N	Total Harmonic Distortion + Noise $P_o = 200mW$ rms, $G_v = 2$, $20Hz < f < 20kHz$, $R_L = 8\Omega$		0.15		%
PSRR	Power Supply Rejection Ratio ²⁾ $f = 217Hz$, $R_L = 8\Omega$, $R_{Feed} = 22K\Omega$, $V_{ripple} = 200mV$ rms		77		dB
Φ_M	Phase Margin at Unity Gain $R_L = 8\Omega$, $C_L = 500pF$		70		Degrees
GM	Gain Margin $R_L = 8\Omega$, $C_L = 500pF$		20		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz

1. Standby mode is activated when V_{stdby} is tied to GND

2. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. Vripple is the surimposed sinus signal to V_{CC} @ $f = 217Hz$

Components	Functional Description
R_{in}	Inverting input resistor which sets the closed loop gain in conjunction with R_{feed} . This resistor also forms a high pass filter with C_{in} ($f_c = 1 / (2 \times \pi \times R_{in} \times C_{in})$)
C_{in}	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
R_{feed}	Feed back resistor which sets the closed loop gain in conjunction with R_{in}
C_s	Supply Bypass capacitor which provides power supply filtering
C_b	Bypass pin capacitor which provides half supply filtering
C_{feed}	Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency $1 / (2 \times \pi \times R_{feed} \times C_{feed})$)
R_{stb}	Pull-up resistor which fixes the right supply level on the standby pin
G_v	Closed loop gain in BTL configuration = $2 \times (R_{feed} / R_{in})$

REMARKS

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor $C_s = 100\mu F$.
2. The standby response time is about $1\mu s$.

Fig. 1 : Open Loop Frequency Response

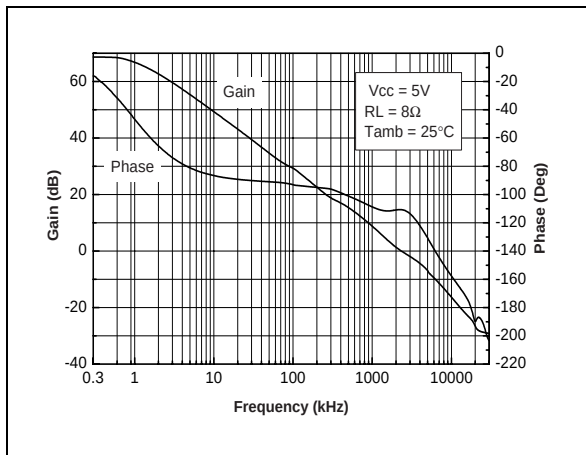


Fig. 2 : Open Loop Frequency Response

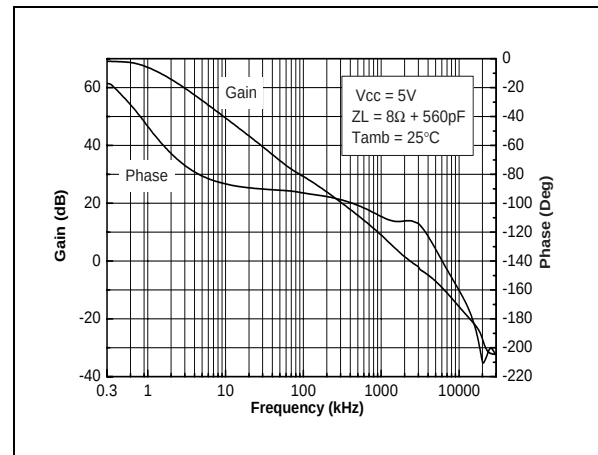


Fig. 3 : Open Loop Frequency Response

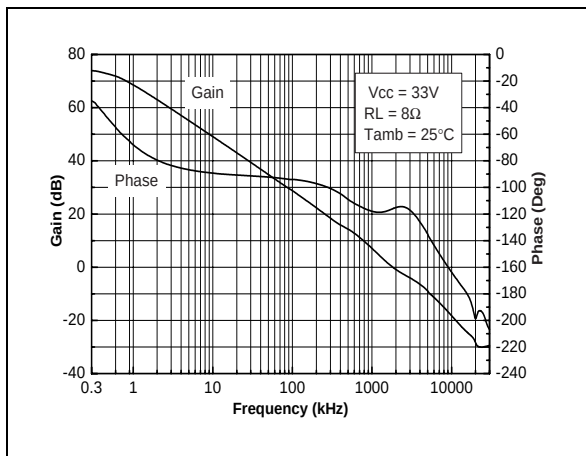


Fig. 4 : Open Loop Frequency Response

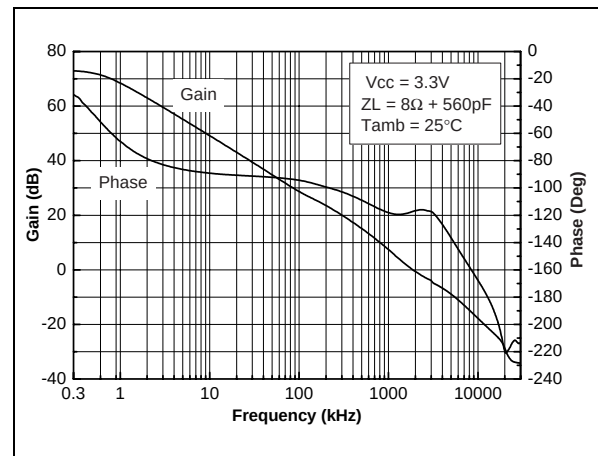


Fig. 5 : Open Loop Frequency Response

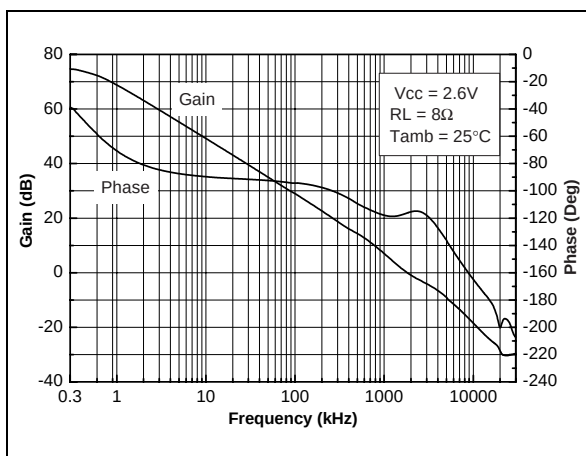


Fig. 6 : Open Loop Frequency Response

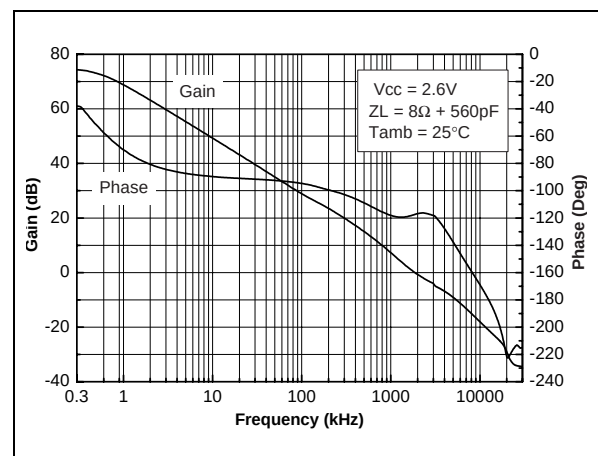


Fig. 7 : Open Loop Frequency Response

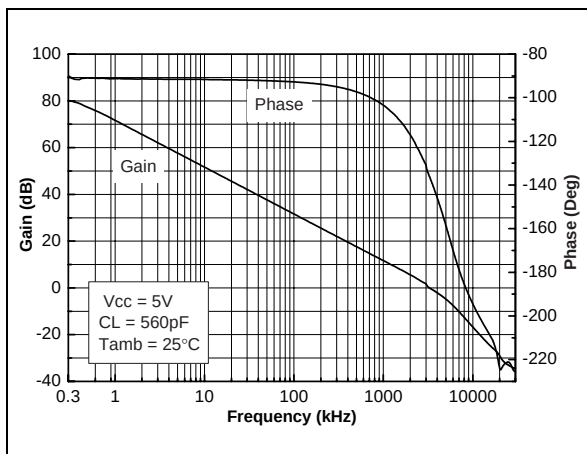


Fig. 8 : Open Loop Frequency Response

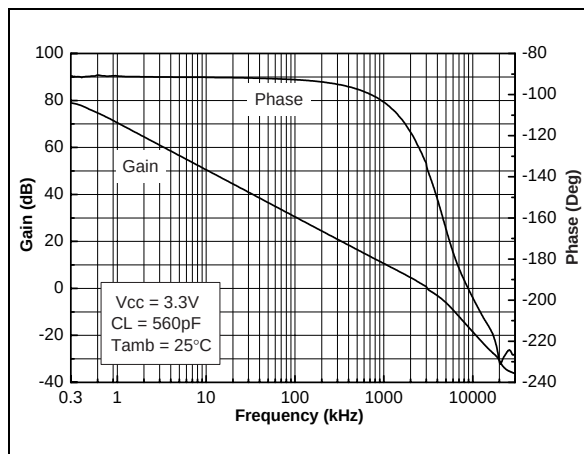


Fig. 9 : Open Loop Frequency Response

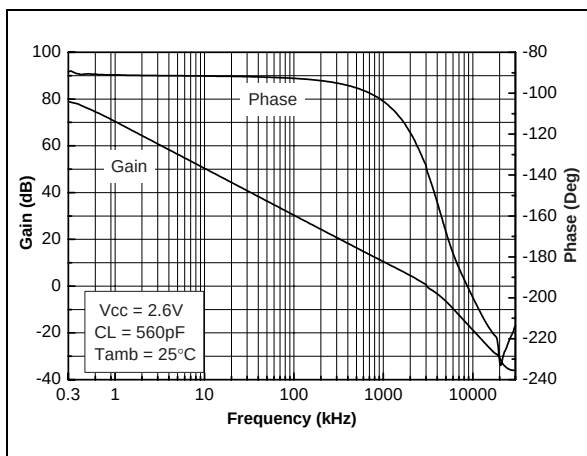


Fig. 10 : Power Supply Rejection Ratio (PSRR) vs Power supply

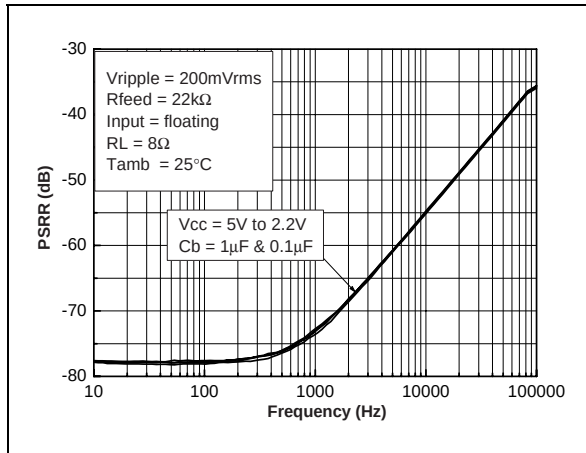


Fig. 11 : Power Supply Rejection Ratio (PSRR) vs Feedback Capacitor

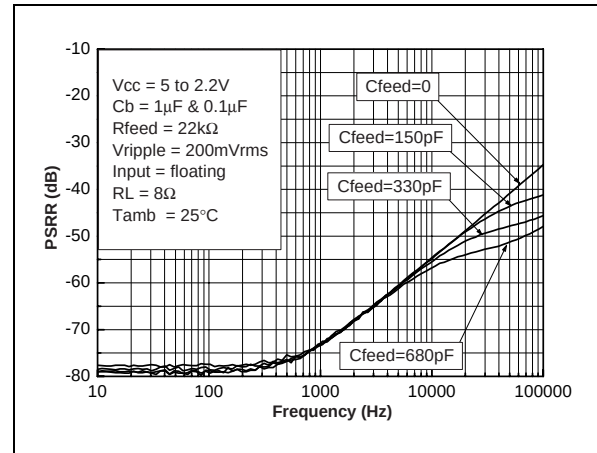


Fig. 12 : Power Supply Rejection Ratio (PSRR) vs Bypass Capacitor

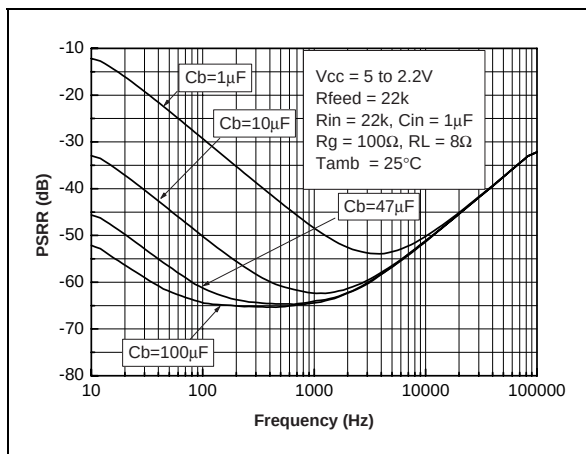


Fig. 13 : Power Supply Rejection Ratio (PSRR) vs Input Capacitor

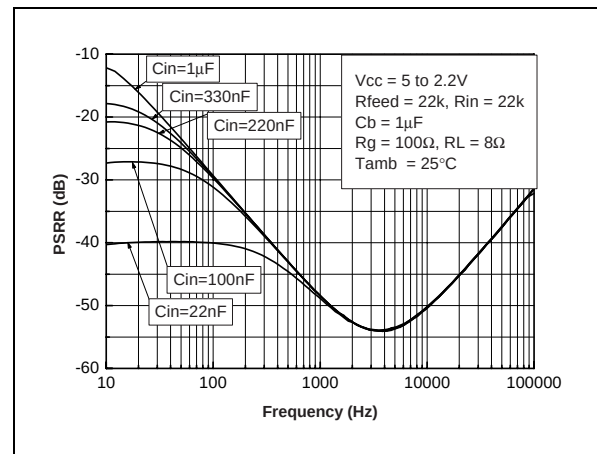


Fig. 14 : Power Supply Rejection Ratio (PSRR) vs Feedback Resistor

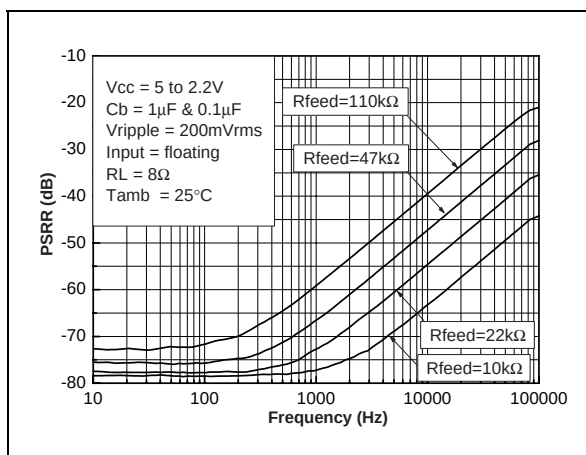


Fig. 15 : Pout @ THD + N = 1% vs Supply Voltage vs RL

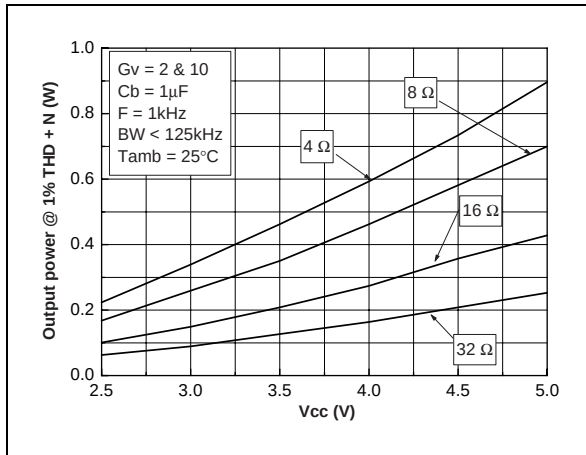


Fig. 16 : Pout @ THD + N = 10% vs Supply Voltage vs RL

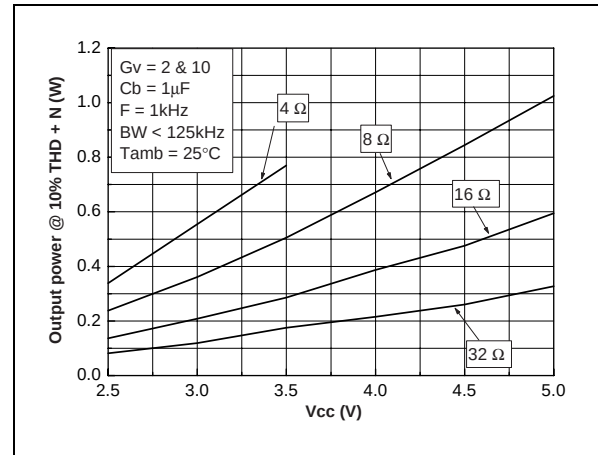


Fig. 17 : Power Dissipation vs Pout

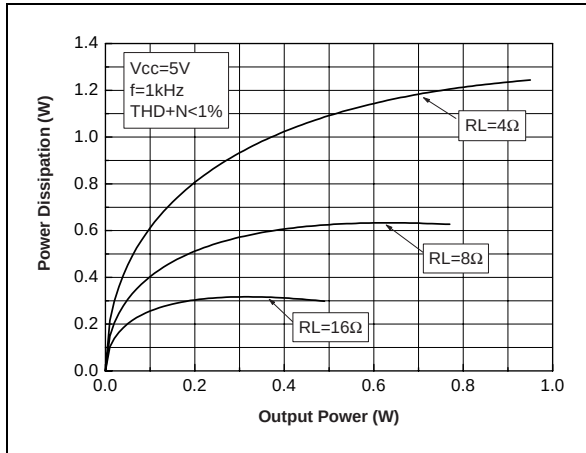


Fig. 18 : Power Dissipation vs Pout

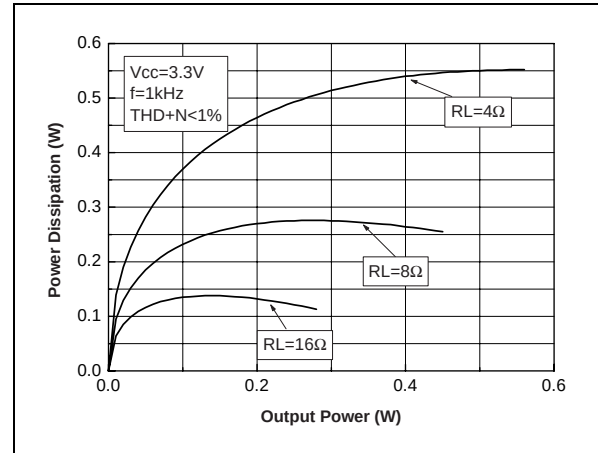


Fig. 19 : Power Dissipation vs Pout

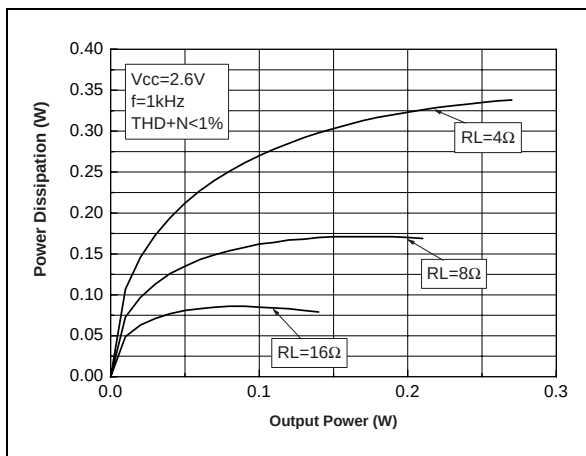


Fig. 20 : Power Derating Curves

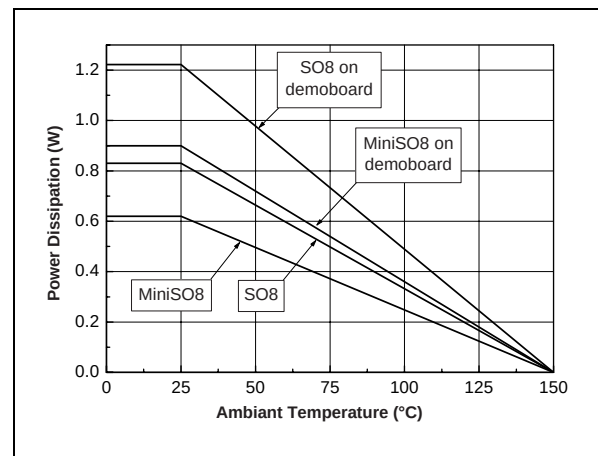


Fig. 21 : Output Power vs Load Resistance

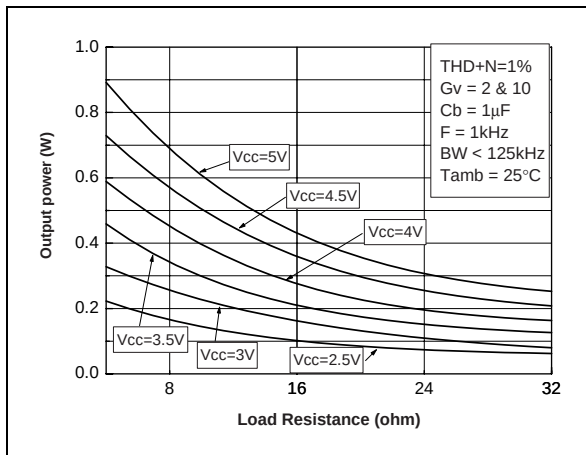


Fig. 22 : Output Power vs Load Resistance

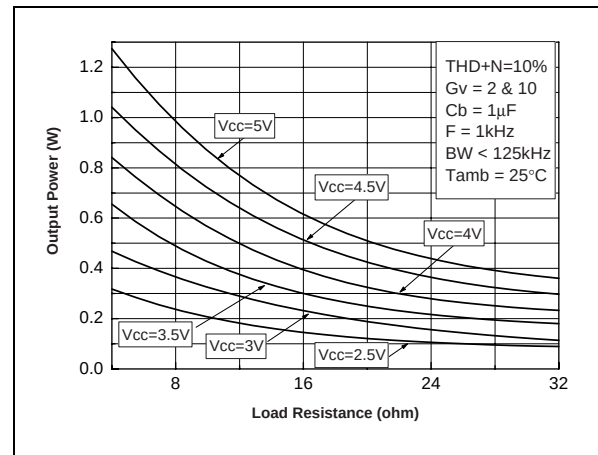


Fig. 23 : Clipping Voltage vs Supply Voltage

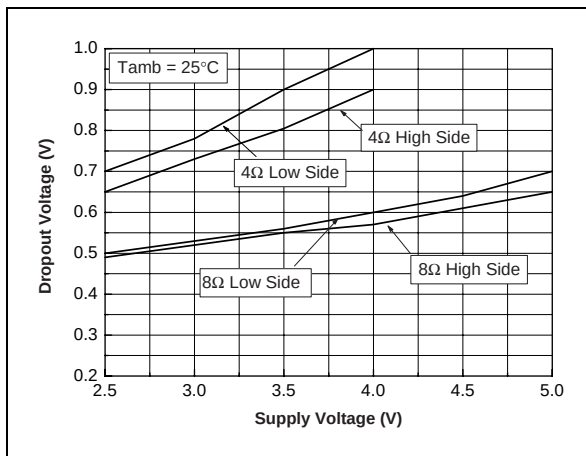
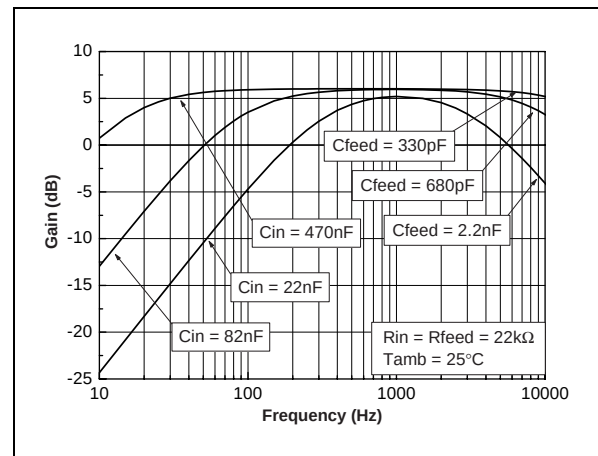
Fig. 24 : Frequency response vs C_{in} & C_{feed} 

Fig. 25 : Noise Floor

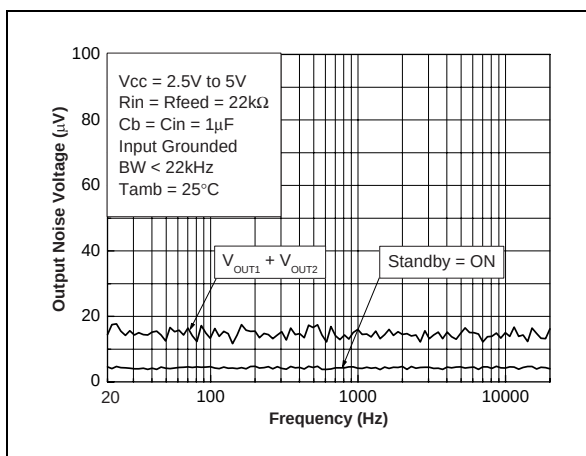


Fig. 26 : THD + N vs Output Power

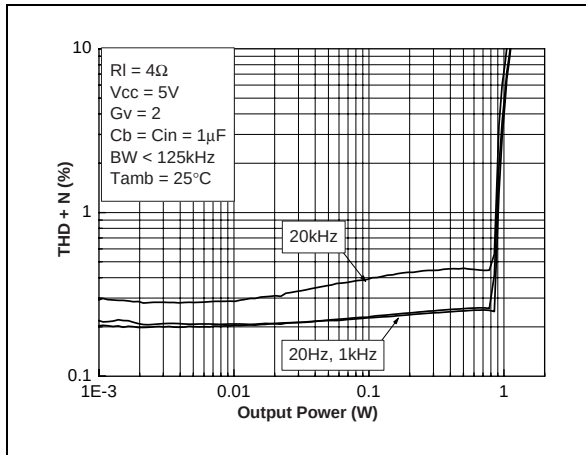


Fig. 27 : THD + N vs Output Power

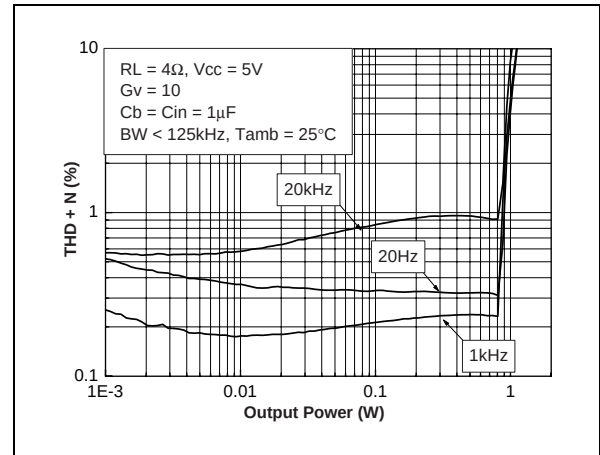


Fig. 28 : THD + N vs Output Power

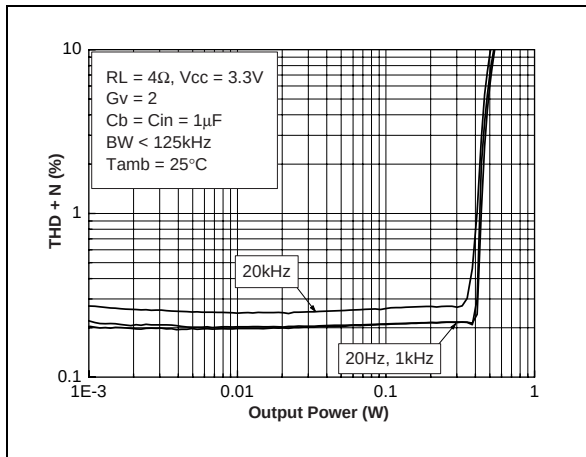


Fig. 29 : THD + N vs Output Power

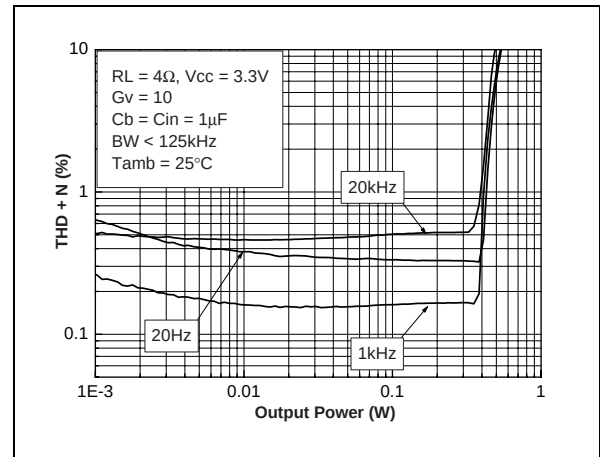


Fig. 30 : THD + N vs Output Power

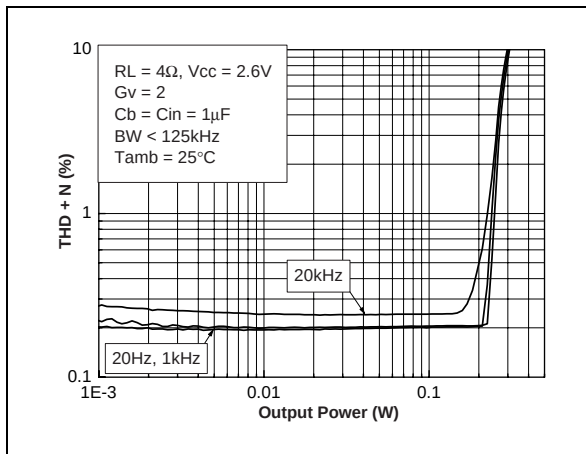


Fig. 31 : THD + N vs Output Power

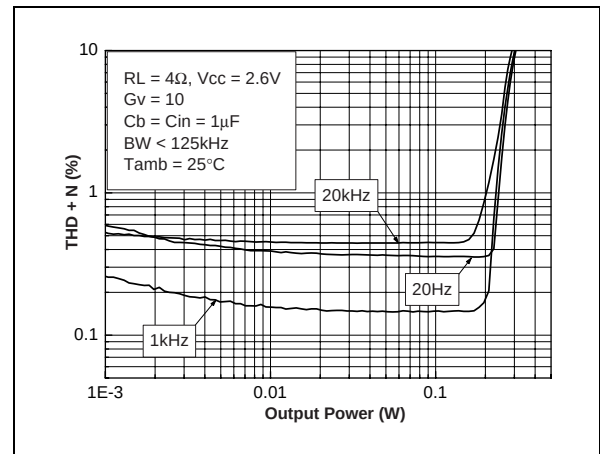


Fig. 32 : THD + N vs Output Power

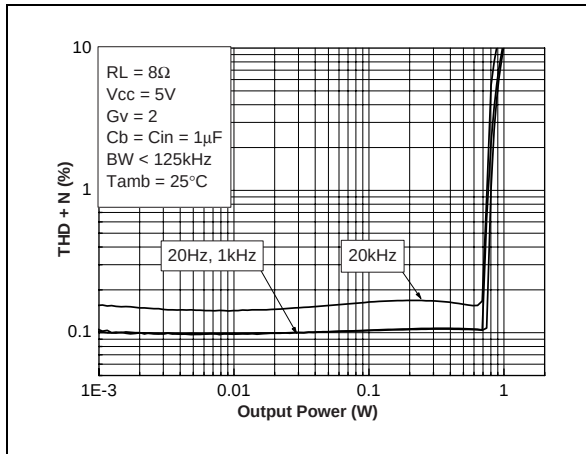


Fig. 33 : THD + N vs Output Power

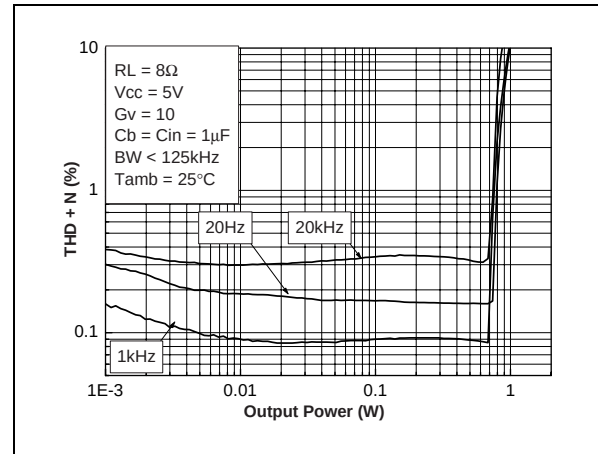


Fig. 34 : THD + N vs Output Power

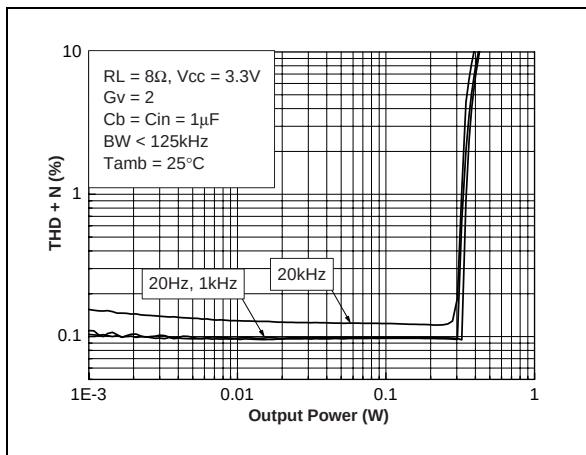


Fig. 35 : THD + N vs Output Power

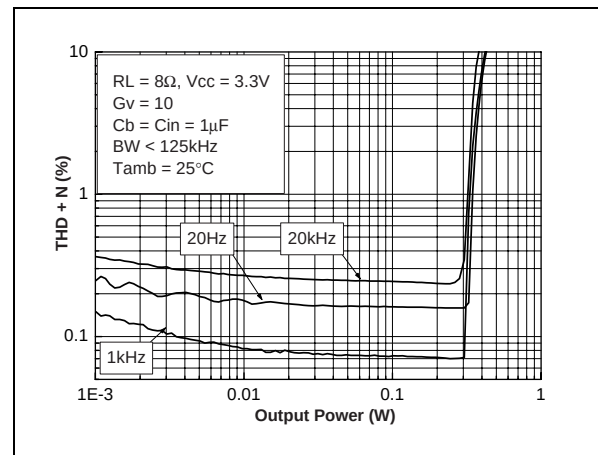


Fig. 36 : THD + N vs Output Power

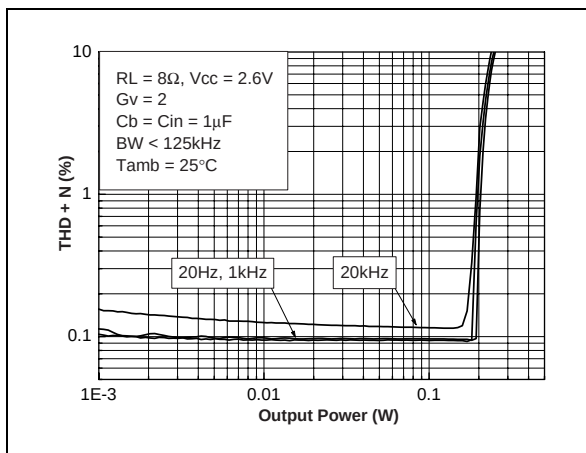


Fig. 37 : THD + N vs Output Power

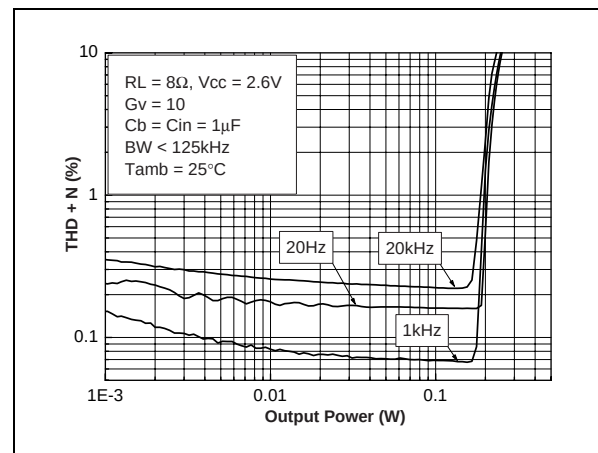


Fig. 38 : THD + N vs Output Power

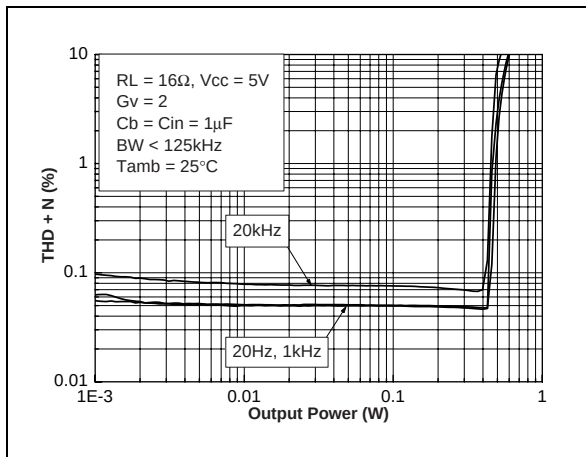


Fig. 39 : THD + N vs Output Power

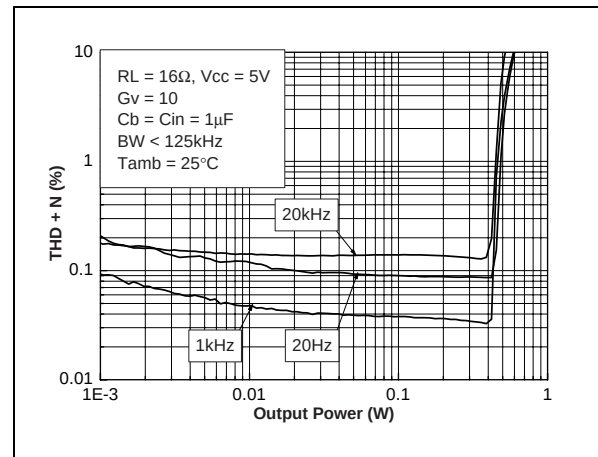


Fig. 40 : THD + N vs Output Power

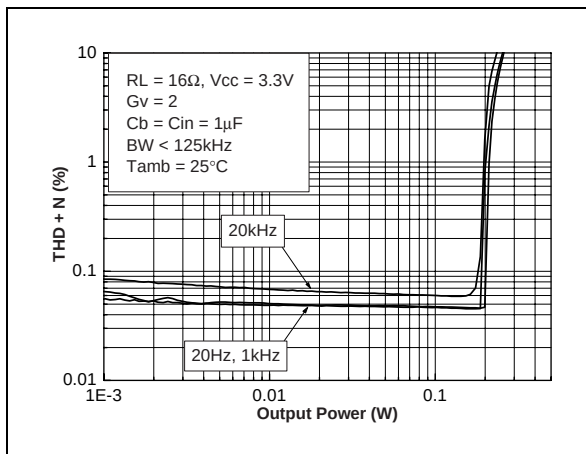


Fig. 41 : THD + N vs Output Power

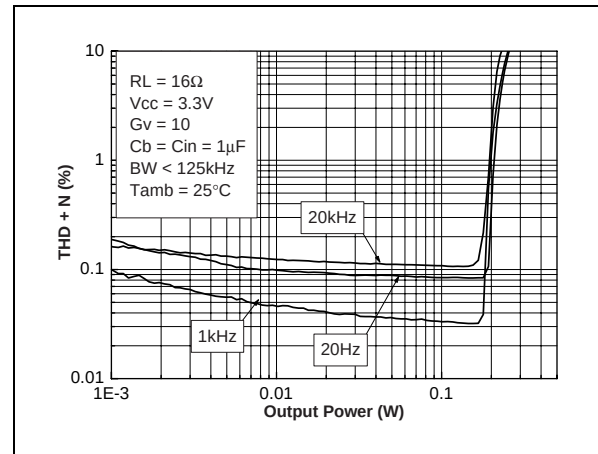


Fig. 42 : THD + N vs Output Power

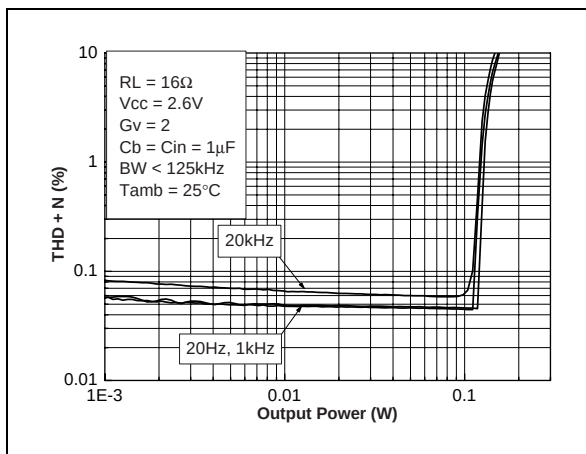


Fig. 43 : THD + N vs Output Power

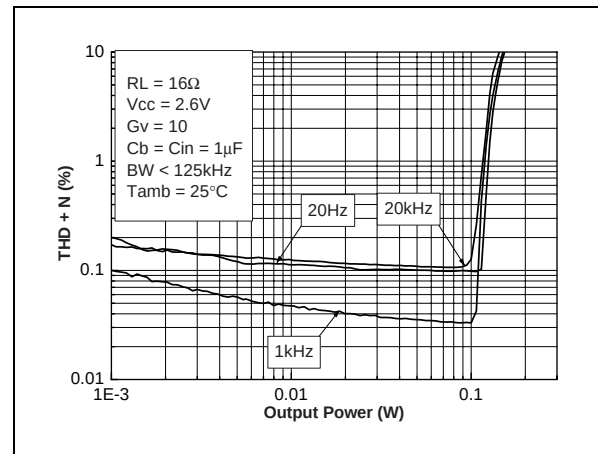


Fig. 44 : Signal to Noise Ratio vs Power Supply with Unweighted Filter (20Hz to 20kHz)

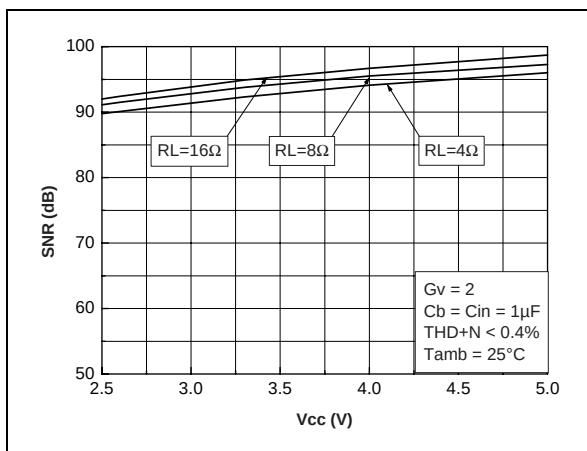


Fig. 45 : Signal to Noise Ratio Vs Power Supply with Unweighted Filter (20Hz to 20kHz)

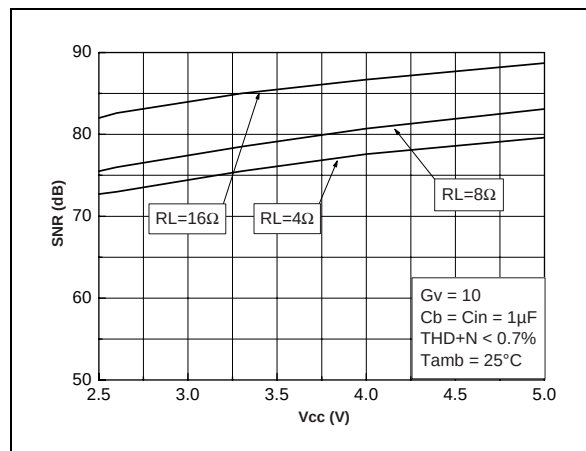


Fig. 46 : Signal to Noise Ratio vs Power Supply with Weighted Filter type A

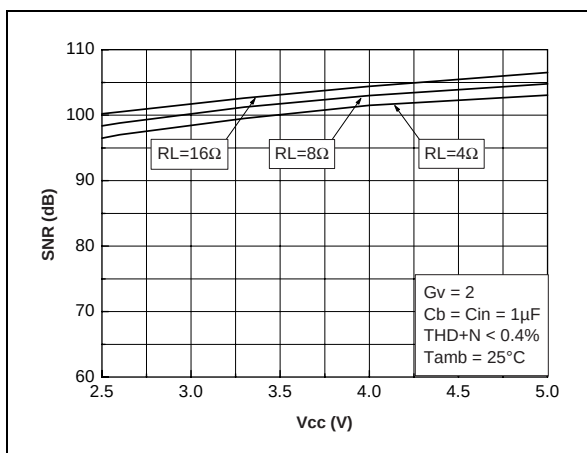


Fig. 47 : Signal to Noise Ratio vs Power Supply with Weighted Filter Type A

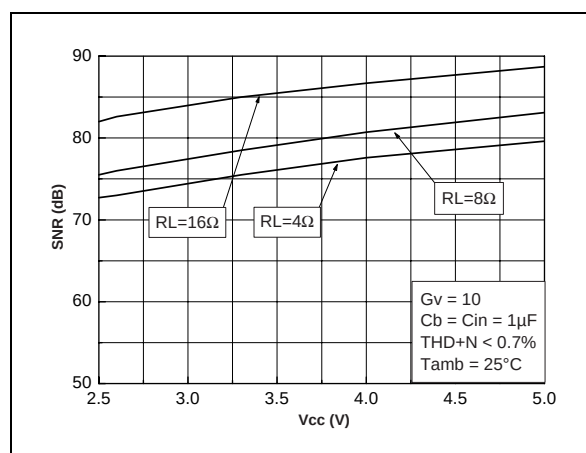


Fig. 48 : Current Consumption vs Power Supply Voltage

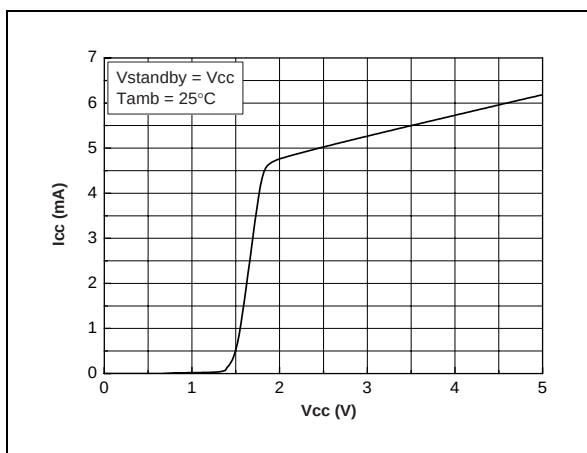


Fig. 49 : Current Consumption vs Standby Voltage @ $V_{CC} = 5V$

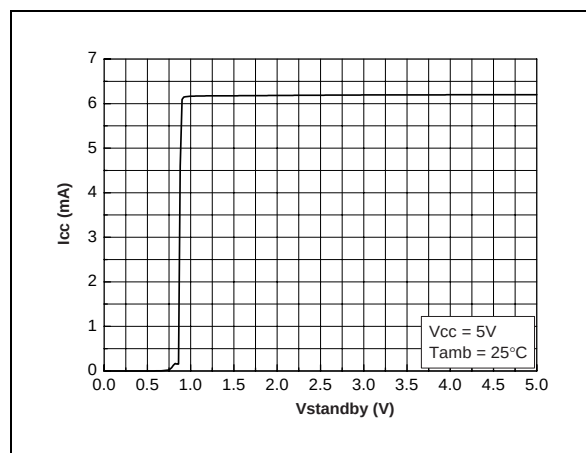


Fig. 50 : Current Consumption vs Standby Voltage @ Vcc = 3.3V

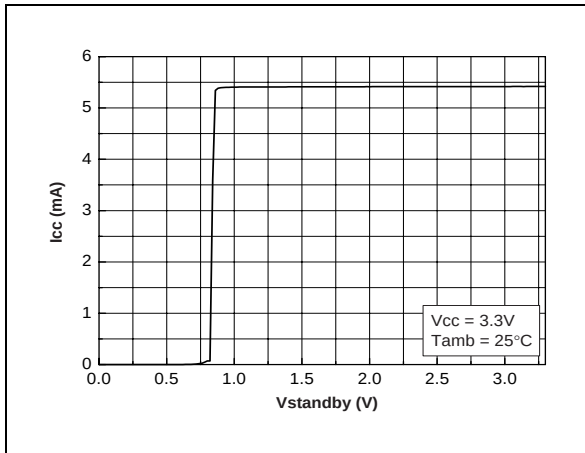
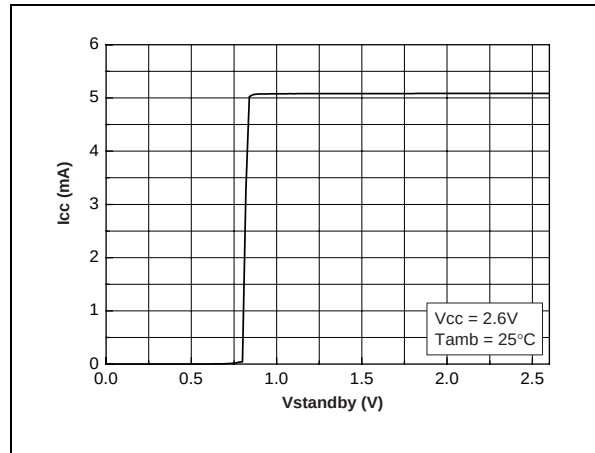


Fig. 51 : Current Consumption vs Standby Voltage @ Vcc = 2.6V



■ BTL Configuration Principle

The TS4902 is a monolithic power amplifier with a BTL (Bridge Tied Load) output configuration. BTL means that each end of the load is connected to two single ended output amplifiers. Thus, we have:

Single ended output 1 = $V_{out1} = V_{out}$ (V)

Single ended output 2 = $V_{out2} = -V_{out}$ (V)

And $V_{out1} - V_{out2} = 2V_{out}$ (V)

The output power is :

$$P_{out} = \frac{(2 V_{out_{RMS}})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

■ Gain In Typical Application Schematic (cf. page 1)

In flat region (no effect of C_{in}), the output voltage of the first stage is :

$$V_{out1} = -V_{in} \frac{R_{feed}}{R_{in}} (V)$$

For the second stage : $V_{out2} = -V_{out1}$ (V)

The differential output voltage is

$$V_{out2} - V_{out1} = 2V_{in} \frac{R_{feed}}{R_{in}} (V)$$

The differential gain named gain (G_v) for more convenient usage is :

$$G_v = \frac{V_{out2} - V_{out1}}{V_{in}} = 2 \frac{R_{feed}}{R_{in}}$$

Remark : V_{out2} is in phase with V_{in} and V_{out1} is 180 phased with V_{in} . It means that the positive terminal of the loudspeaker should be connected to V_{out2} and the negative to V_{out1} .

■ Low and high frequency response

In low frequency region, the effect of C_{in} starts. C_{in} with R_{in} forms a high pass filter with a -3dB cut off frequency

$$F_{CL} = \frac{1}{2\pi R_{in} C_{in}} (Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel with R_{feed} . Its form a low pass filter with a -3dB cut off frequency

$$F_{CH} = \frac{1}{2\pi R_{feed} C_{feed}} (Hz)$$

■ Power dissipation and efficiency

Hypothesis :

- Voltage and current in the load are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{cc})

Regarding the load we have :

$$V_{OUT} = V_{PEAK} \sin \omega t (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A)$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} (W)$$

Then, the average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = 2 \frac{V_{PEAK}}{\pi R_L} (A)$$

The power delivered by the supply voltage is
 $P_{supply} = V_{cc} I_{CC_{AVG}} (W)$

Then, the **power dissipated by the amplifier** is
 $P_{diss} = P_{supply} - P_{out} (W)$

$$P_{diss} = \frac{2\sqrt{2}V_{cc}}{\pi\sqrt{R_L}} \sqrt{P_{OUT}} - P_{OUT} (W)$$

and the maximum value is obtained when

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{dissmax} = \frac{2V_{cc}^2}{\pi^2 R_L} (W)$$

Remark : This maximum value is only depending on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}$, so

$$\frac{\pi}{4} = 78.5\%$$

■ Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4902, a power supply bypass capacitor C_s and a bias voltage bypass capacitor C_b .

C_s has especially an influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances.

With 100μF, you can expect similar THD+N performances like shown in the datasheet.

If C_s is lower than 100μF, in high frequency increases, THD+N and disturbances on the power supply rail are less filtered.

To the contrary, if C_s is higher than 100μF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N in lower frequency, but its function is critical on the final result of PSRR with input grounded in lower frequency.

If C_b is lower than 1μF, THD+N increase in lower frequency (see THD+N vs frequency curves) and the PSRR worsens up

If C_b is higher than 1μF, the benefit on THD+N in lower frequency is small but the benefit on PSRR is substantial (see PSRR vs. C_b curve : fig.12).

Note that C_{in} has a non-negligible effect on PSRR in lower frequency. Lower is its value, higher is the PSRR (see fig. 13).

■ Pop and Click performance

Pop and Click performance is intimately linked with the size of the input capacitor C_{in} and the bias voltage bypass capacitor C_b .

Size of C_{in} is due to the lower cut-off frequency and PSRR value requested. Size of C_b is due to THD+N and PSRR requested always in lower frequency.

Moreover, C_b determines the speed that the amplifier turns ON. The slower the speed is, the softer the turn ON noise is.

The charge time of C_b is directly proportional to the internal generator resistance 50kΩ.

Then, the charge time constant for C_b is

$$\tau_b = 50k\Omega \times C_b \text{ (s)}$$

As C_b is directly connected to the non-inverting input (pin 2 & 3) and if we want to minimize, in amplitude and duration, the output spike on V_{out1} (pin 5), C_{in} must be charged faster than C_b . The charge time constant of C_{in} is

$$\tau_{in} = (R_{in} + R_{feed}) \times C_{in} \text{ (s)}$$

Thus we have the relation

$$\tau_{in} \ll \tau_b \text{ (s)}$$

The respect of this relation permits to minimize the pop and click noise.

Remark : Minimize C_{in} and C_b has a benefit on pop and click phenomena but also on cost and size of the application.

Example : your target for the -3dB cut off frequency is 100 Hz. With $R_{in}=R_{feed}=22 \text{ k}\Omega$, $C_{in}=72\text{nF}$ (in fact 82nF or 100nF).

With $C_b=1\mu\text{F}$, if you choose the one of the latest two values of C_{in} , the pop and click phenomena at power supply ON or standby function ON/OFF will be very small

$$50 \text{ k}\Omega \times 1\mu\text{F} \gg 44\text{k}\Omega \times 100\text{nF} \text{ (50ms} \gg 4.4\text{ms)}.$$

Increasing C_{in} value increases the pop and click phenomena to an unpleasant sound at power supply ON and standby function ON/OFF.

Why C_s is not important in pop and click consideration ?

Hypothesis :

- $C_s = 100\mu\text{F}$
- Supply voltage = 5V
- Supply voltage internal resistor = 0.1Ω
- Supply current of the amplifier $I_{cc} = 6\text{mA}$

At power ON of the supply, the supply capacitor is charged through the internal power supply resistor. So, to reach 5V you need about five to ten times the charging time constant of C_s ($\tau_s = 0.1 \times C_s \text{ (s)}$).

Then, this time equal 50μs to 100μs $\ll \tau_b$ in the majority of application.

At power OFF of the supply, Cs is discharged by a constant current I_{CC} . The discharge time from 5V to 0V of Cs is

$$t_{DischCs} = \frac{5C_s}{I_{CC}} = 83 \text{ ms}$$

Now, we must consider the discharge time of Cb. At power OFF or standby ON, Cb is discharged by a 100kΩ resistor. So the discharge time is about $\tau_{bDisch} \approx 3 \times C_b \times 100k\Omega$ (s). In the majority of application, $C_b = 1\mu F$, then $\tau_{bDisch} \approx 300ms \gg t_{dischCs}$.

■ How to use the PSRR curves (page 7)

We have finished a design and we have chosen the components values :

- $R_{in} = R_{feed} = 22k\Omega$, $C_{in} = 100nF$, $C_b = 1\mu F$

Now, on fig. 13, we can see the PSRR (input grounded) vs frequency curves. At 217Hz we have a PSRR value of -36dB.

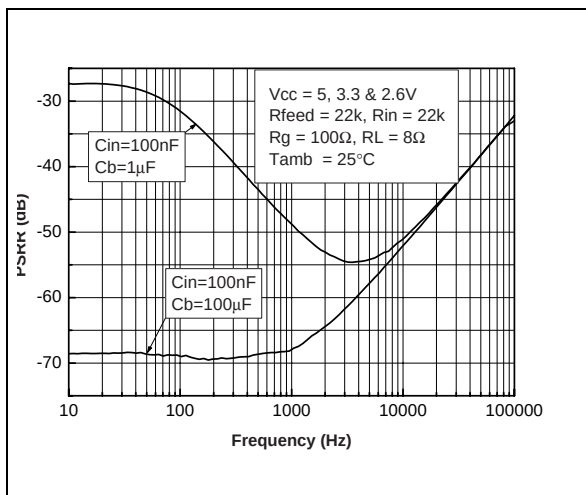
In fact, we want a value of about -70dB. So, we need a gain of +34dB !

Now, on fig. 12 we can see the effect of Cb on the PSRR (input grounded) vs. frequency. With $C_b = 100\mu F$, we can reach the -70dB value.

The process to obtain the final curve ($C_b = 100\mu F$, $C_{in} = 100nF$, $R_{in} = R_{feed} = 22k\Omega$) is a simple transfer point by point on each frequency of the curve on fig. 13 to the curve on fig. 12.

The measurement result is shown on figure A.

Fig. A : PSRR changes with Cb



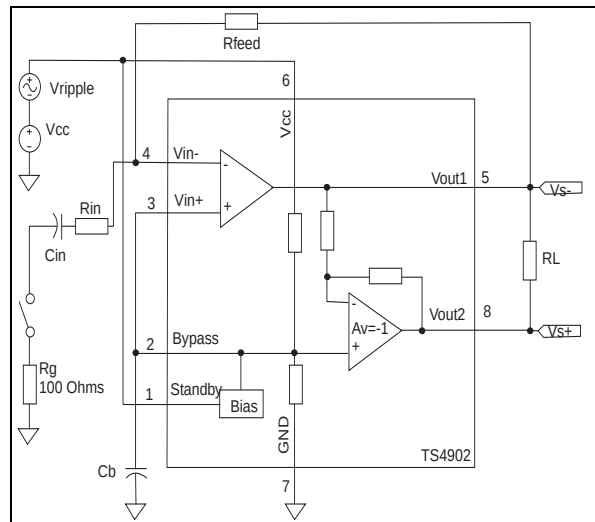
■ Remark on PSRR measurement conditions

What is the PSRR ?

The PSRR is the Power Supply Rejection Ratio. It's a kind of SVR in a determined frequency range. The PSRR of a device is the ratio between the power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

How do we measure the PSRR ?

Fig. B : PSRR measurement schematic



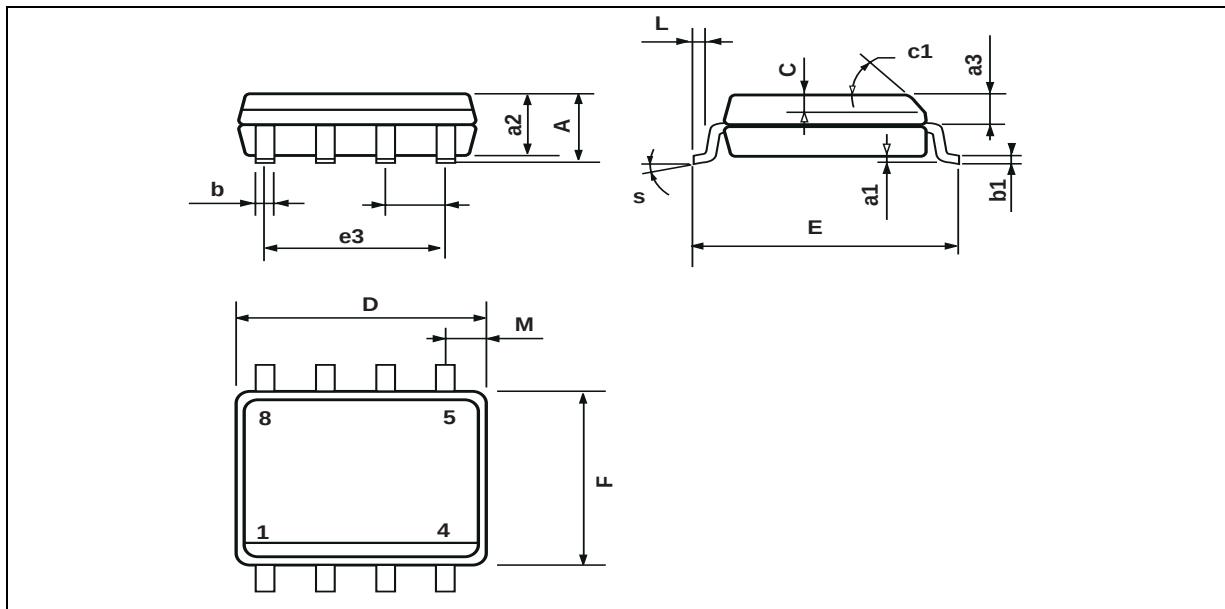
■ Measurement process:

- Fix the DC voltage supply (V_{cc})
- Fix the AC sinusoidal ripple voltage (V_{ripple})
- No bypass capacitor Cs is used

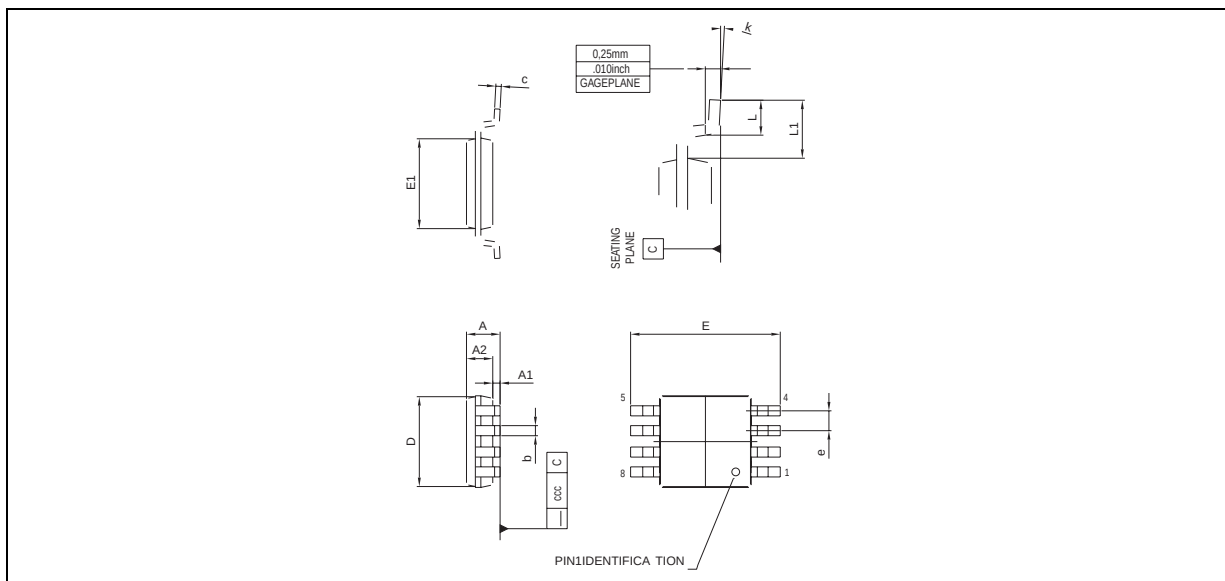
The PSRR value for each frequency is :

$$PSRR(dB) = 20 \times \log_{10} \left[\frac{Rms(V_{ripple})}{Rms(V_{s+} - V_{s-})} \right]$$

Remark : The measurement of the RMS voltage is not a selective RMS measurement but a full range (2 Hz to 125 kHz) RMS measurement. This means we have: the effective RMS signal + the noise.

PACKAGE MECHANICAL DATA**8 PINS - PLASTIC MICROPACKAGE (SO)**

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

PACKAGE MECHANICAL DATA**8 PINS - PLASTIC MICROPACKAGE (miniSO)**

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.100			0.043
A1	0.050	0.100	0.150	0.002	0.004	0.006
A2	0.780	0.860	0.940	0.031	0.034	0.037
b	0.250	0.330	0.400	0.010	0.013	0.016
c	0.130	0.180	0.230	0.005	0.007	0.009
D	2.900	3.000	3.100	0.114	0.118	0.122
E	4.750	4.900	5.050	0.187	0.193	0.199
E1	2.900	3.000	3.100	0.114	0.118	0.122
e		0.650			0.026	
L	0.400	0.550	0.700	0.016	0.022	0.028
L1		0.950			0.037	
k	0d	3d	6d	0d	3d	6d
ccc			0.100			0.004

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