USBDFxxW5

A.S.D.™

EMI FILTER AND LINE TERMINATION FOR USB DOWNSTREAM PORTS

APPLICATIONS

EMI Filter and line termination for USB downstream ports on:
- Desktop computer
- Notebooks
- Workstations
- USB Hubs

FEATURES

- Monolithic device with recommended line termination for USB downstream ports
- Integrated Rt series termination and Ct bypassing capacitors.
- Integrated ESD protection
- Small package size

DESCRIPTION

The USB specification requires USB downstream ports to be terminated with pull-down resistors from the D+ and D- lines to ground. On the implementation of USB systems, the radiated and conducted EMI should be kept within the required levels as stated by the FCC regulations. In addition to the requirements of termination and EMC compatibility, the computing devices are required to be tested for ESD susceptibility.

The USBDFxxW5 provides the recommended line termination while implementing a low pass filter to limit EMI levels and providing ESD protection which exceeds IEC 61000-4-2 level 4 standard. The device is packaged in a SOT323-5L which is the smallest available lead frame package (50% smaller than the standard SOT23).

BENEFITS

- EMI / RFI noise suppression
- Required line termination for USB downstream ports
- ESD protection exceeding IEC61000-4-2 level 4
- High flexibility in the design of high density boards
- Tailored to meet USB 1.1 standard

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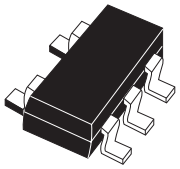
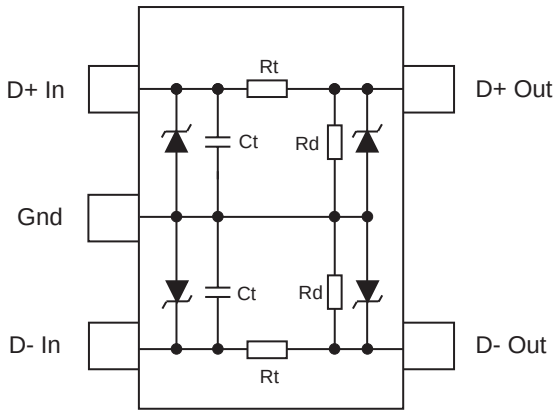


SOT323-5L

FUNCTIONAL DIAGRAM



	Rt	Rd	Ct
Code 01	33Ω	15kΩ	47pF
Code 02	15Ω	15kΩ	47pF
Tolerance	±10%	±10%	±20%

COMPLIES WITH THE FOLLOWING ESD STANDARDS:

IEC-61000-4-2, level 4
±15 kV (air discharge)
±8 kV (contact discharge)

MIL STD 883C, Method 3015-6
Class 3 C = 100 pF R = 1500 Ω
3 positive strikes and 3 negative strikes (F = 1 Hz)

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

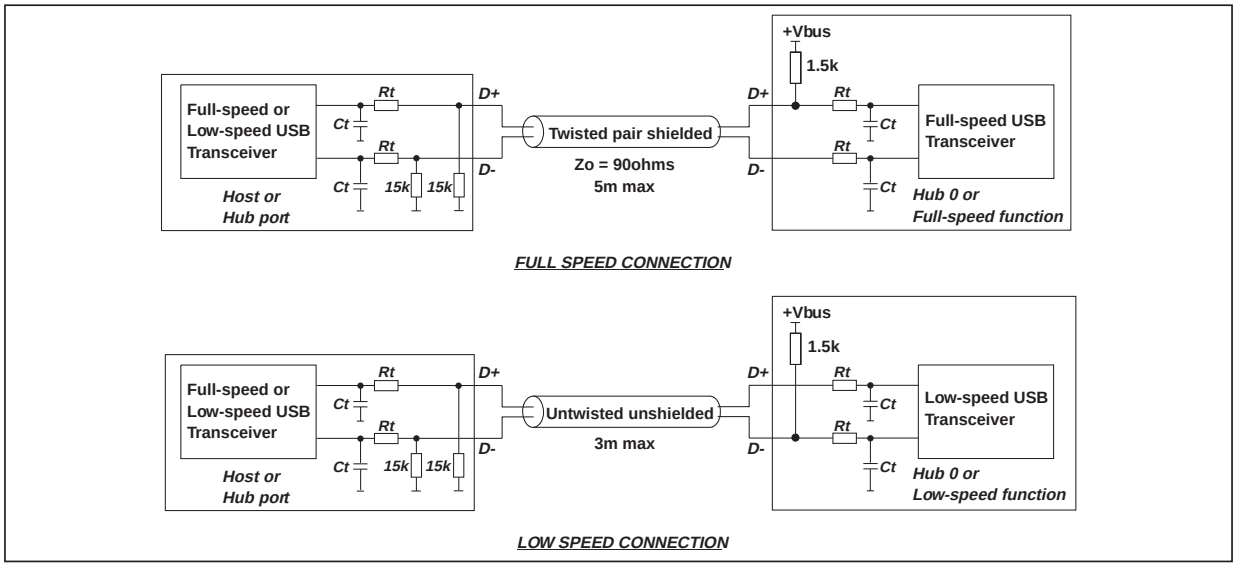
Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, contact discharge ESD discharge - MIL STD 883 - Method 3015-6	±15 ±25	kV kV
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature range	- 55 to +150	°C
T_L	Lead solder temperature (10 second duration)	260	°C
T_{op}	Operating temperature Range	0 to 70	°C
P_r	Power rating per resistor	100	mW

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

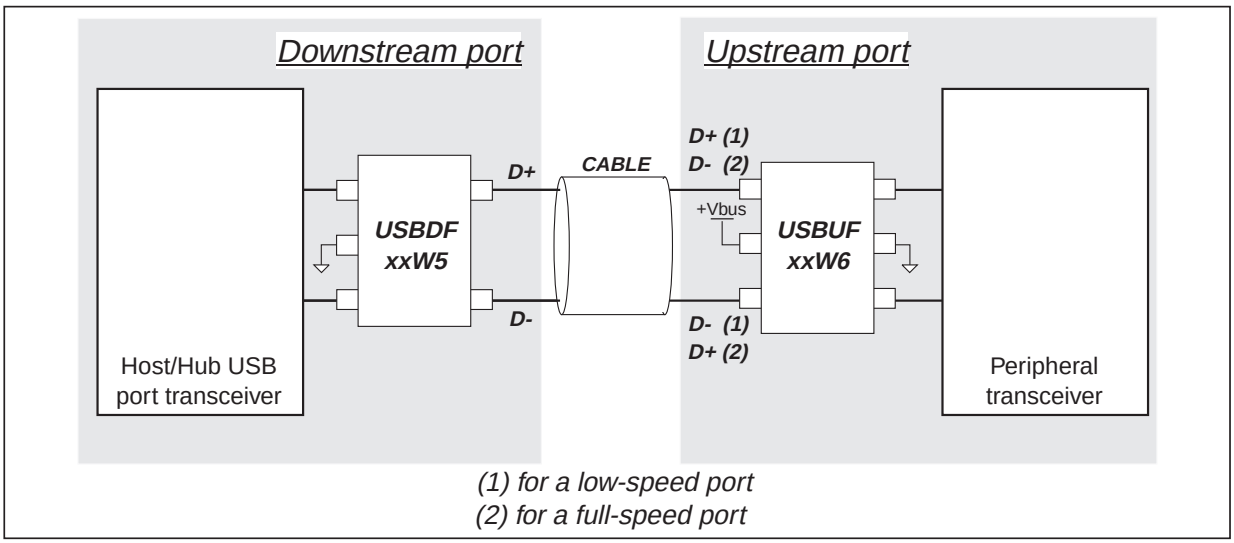
Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
V_{BR}	Diode breakdown voltage	I_R = 1mA	6			V
V_F	Diode forward voltage drop	I_F = 50mA		0.9		V

APPLICATION INFORMATION

Fig. A1: USB Standard requirements



APPLICATION EXAMPLE



EMI FILTERING

Current FCC regulations requires that class B computing devices meet specified maximum levels for both ratiated and conducted EMI.

- Radiated EMI covers the frequency range from 30MHz to 1GHz.
- Conducted EMI covers the 450kHz to 30MHz range.

For the types of devices utilizing the USB the most difficult test to pass is usually the radiated EMI test. For this reason the USBDF device is aiming to minimize radiated EMI.
The differential signal (D+ and D-) of the USB does not contribute significantly to radiated or conducted EMI because the magnetic field of the two conductors exactly cancels each other.
The inside of the PC environment is very noisy and designers must minimise noise coupling from the different sources. D+ and D- must not be routed near high speed lines (clocks...).
Induced common mode noise can be minimised by running pairs of USB signals parallel to each other and running grounded guard trace on each side of the signal pair from the USB controller to the USBDF device.
If possible, locate the USBDF device physically near the USB connectors. Distance between the USB controller and the USB connector must be minimized.
The 47pF (Ct) capacitors are used to bypass high frequency energy to ground and for edge control, and must be placed between the USB Controller and the series termination resistors (Rt). Both Ct and Rt should be placed as close to the USB Controller as practicable.

The USBDFxxW5 ensure a filtering protection against ElectroMagnetic and RadioFrequency Interferences thanks to its low-pass filter structure. This filter is characterized by the following parameters :

- cut-off frequency
- Insertion loss
- high frequency rejection

Fig. A3 shows the attenuation curve for frequencies up to 3GHz.

Fig. A2: Measurement configuration

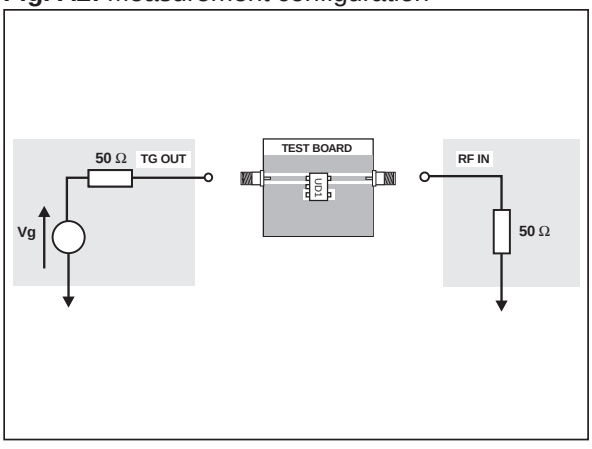
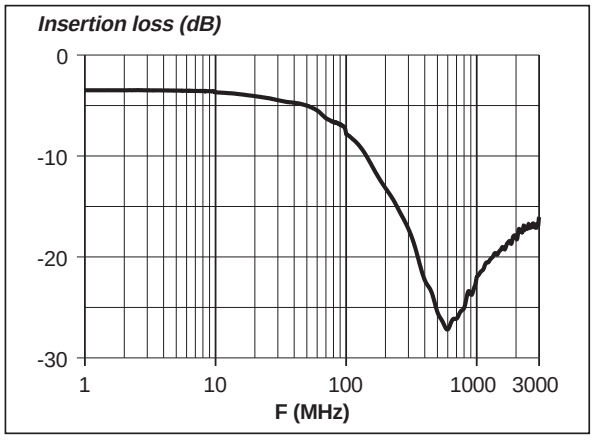


Fig. A3: USBDFxxW5 attenuation curve.



ESD PROTECTION

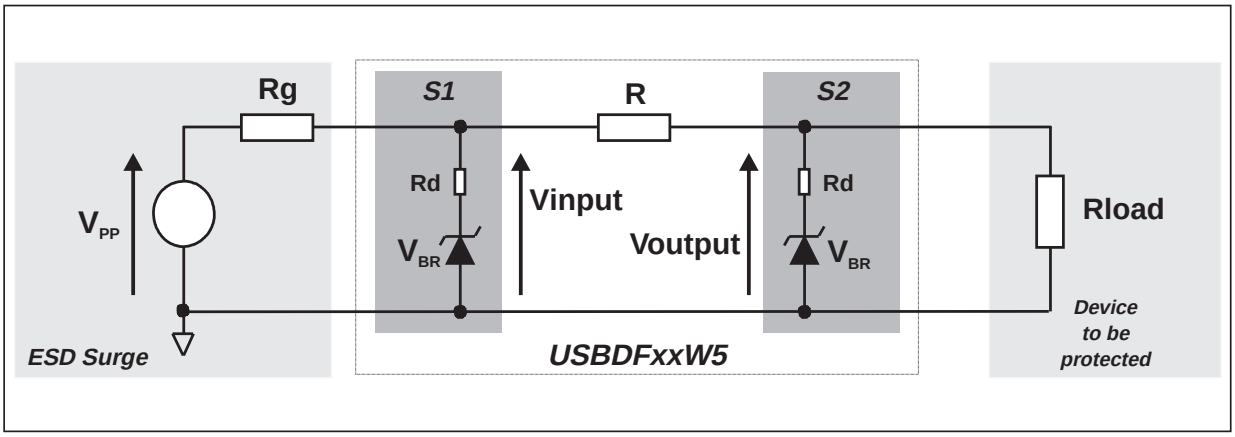
In addition to the requirements of termination and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test is described in the IEC 61000-4-2 and is already in place in Europe. This test requires that a device tolerates ESD events and remain operational without user intervention.

The USBDFxxW5 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at :

$$Vinput = V_{BR} + R_d.I_{PP}$$

This protection function is splitted in 2 stages. As shown in figure A4, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage very low at the Vout level.

Fig. A4: USBDFxxW5 ESD clamping behavior



To have a good approximation of the remaining voltages at both Vin and Vout stages, we give the typical dynamical resistance value Rd. By taking into account these following hypothesis : Rt>Rd, Rg>Rd and Rload>Rd, it gives these formulas:

$$Vinput = \frac{R_g.V_{BR} + R_d.V_g}{R_g}$$

$$Voutput = \frac{R_t.V_{BR} + R_d.Vinput}{R_t}$$

The results of the calculation done for V_{PP}=8kV, Rg=330Ω (IEC61000-4-2 standard), V_{BR}=7V (typ.) and Rd = 1Ω (typ.) give:

Vinput = 31.2 V

Voutput = 7.95 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the Vin side. This parasitic effect is not present at the Vout side due the low current involved after the resistance R.

The measurements done here after show very clearly (Fig. A6) the high efficiency of the ESD protection :

- no influence of the parasitic inductances on Vout stage
- output clamping voltage very close to V_{BR} (positive strike) and $-V_F$ (negative strike)

Fig. A5: Measurement board

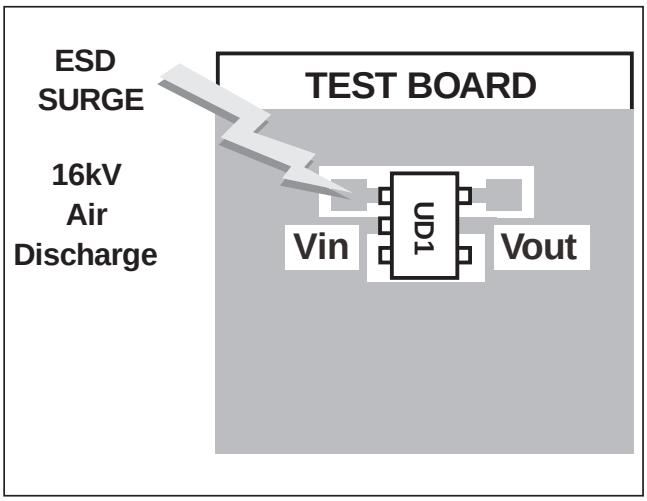
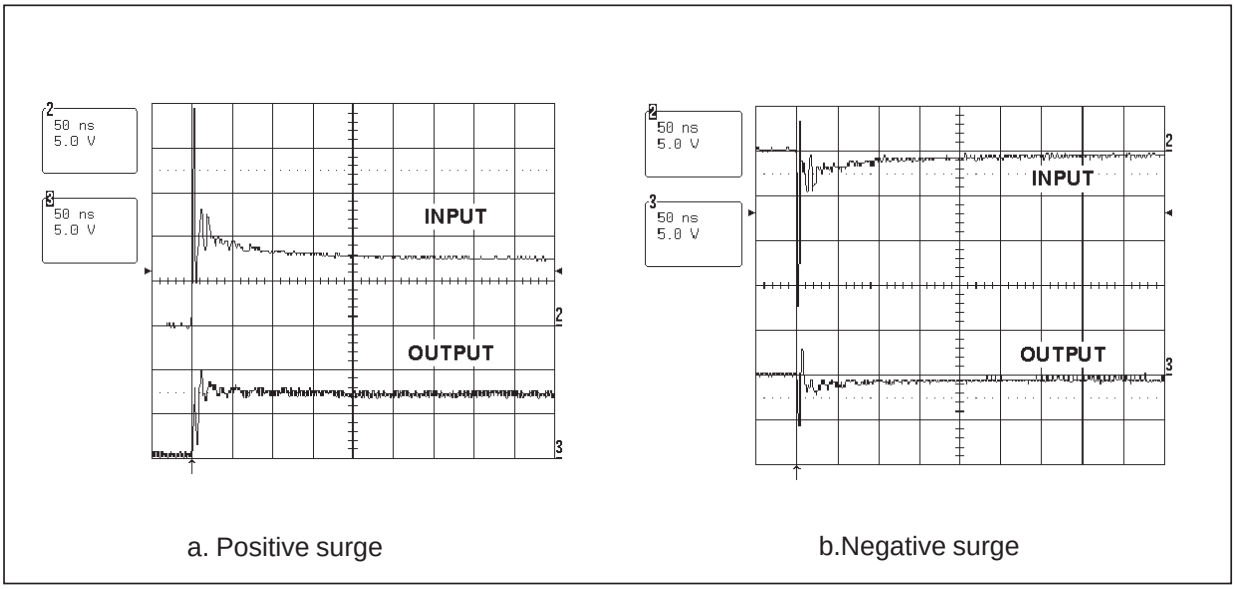


Fig. A6: Remaining voltage at both stages S1 (Vinput) and S2 (Voutput) during ESD surge.



a. Positive surge

b.Negative surge

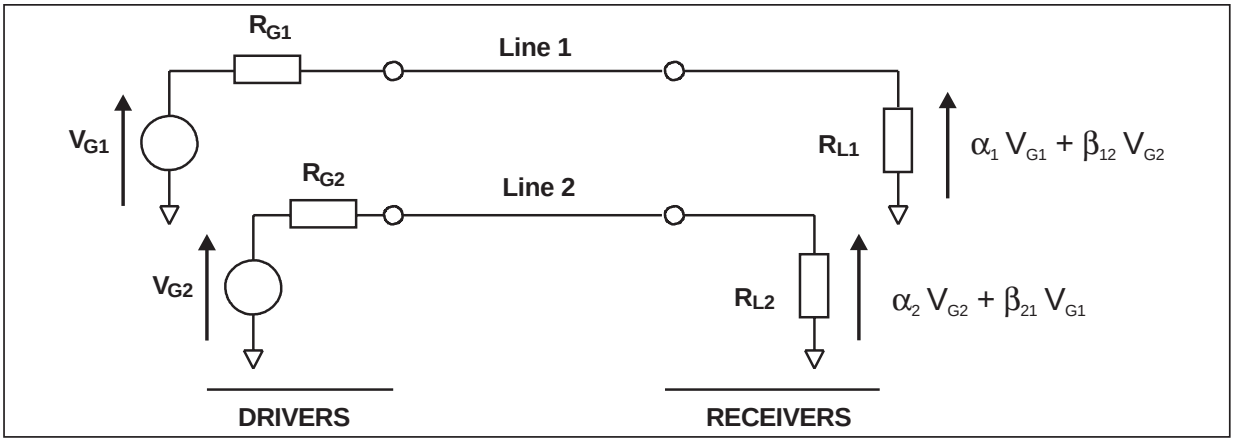
Please note that the USBDFxxW5 is not only acting for positive ESD surges but also for negative ones. For these kinds of disturbances it clamps close to ground voltage as shown in Fig. A6b.

LATCH-UP PHENOMENA

The early ageing and destruction of IC's is often due to latch-up phenomena which is mainly induced by dV/dt. Thanks to its structure, the USBDFxxW5 provides a high immunity to latch-up phenomena by smoothing very fast edges.

CROSSTALK BEHAVIOR

Fig. A7: Crosstalk phenomena



The crosstalk phenomena is due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, this is the reason why we provide crosstalk measurements for monolithic device to guarantee negligeable crosstalk between the lines. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Fig. A8: Analog Crosstalk measurements

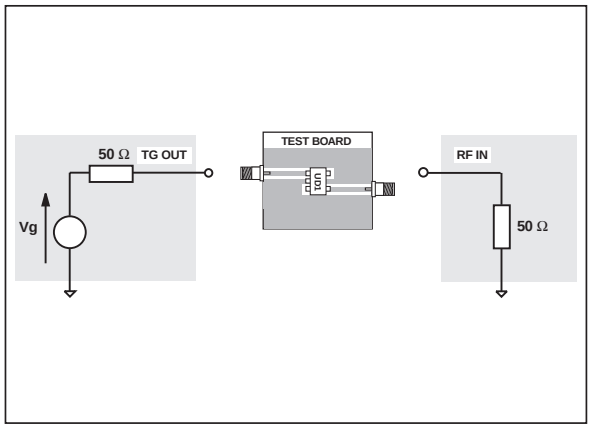


Fig. A9: Typical Analog Crosstalk results

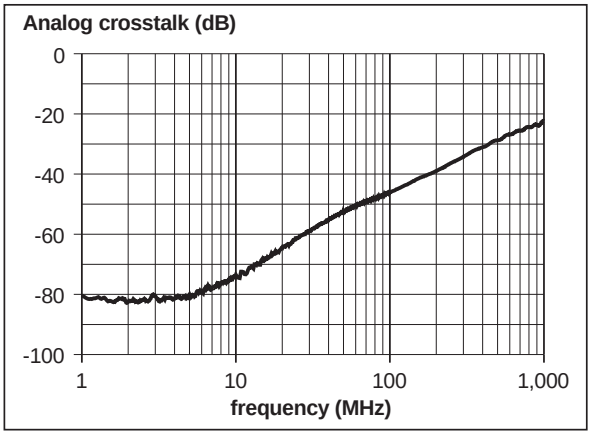


Figure A8 gives the measurement circuit for the analog crosstalk application. In figure A9, the curve shows the effect of the D+ cell on the D- cell. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -46dB.

Fig. A10: Digital crosstalk measurements configuration

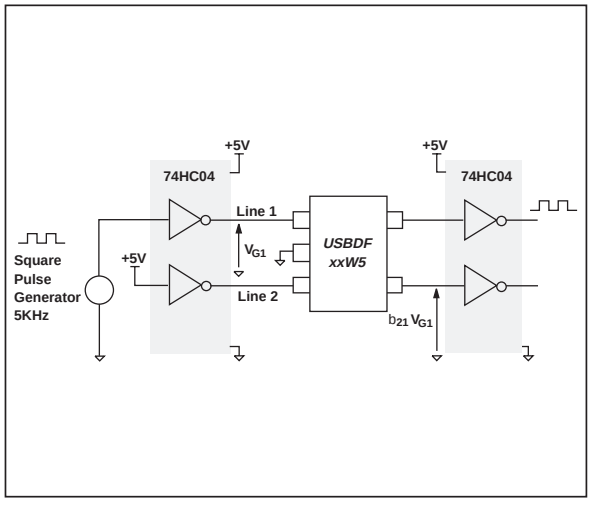


Fig. A11: Digital crosstalk results

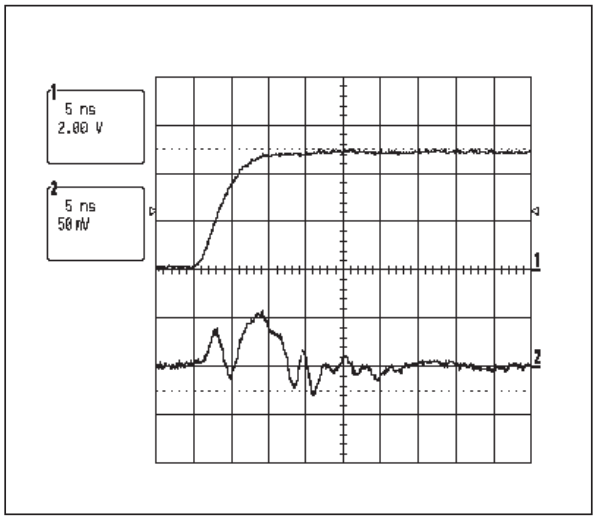


Figure A10 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A11 shows that in such a condition signal from 0 to 5V and rise time of few ns, the impact on the other line is less than 100mV peak to peak (Below the logic high voltage threshold).The measurements performed with falling edges give the same results.

TRANSITION TIMES

This low pass filter has been designed in order to meet the USB 1.1 standard requirements that implies the signal edges are maintained within the 4ns-20ns stipulated USB specification limits.

Fig. A12: Typical rise and fall times: measurements configuration

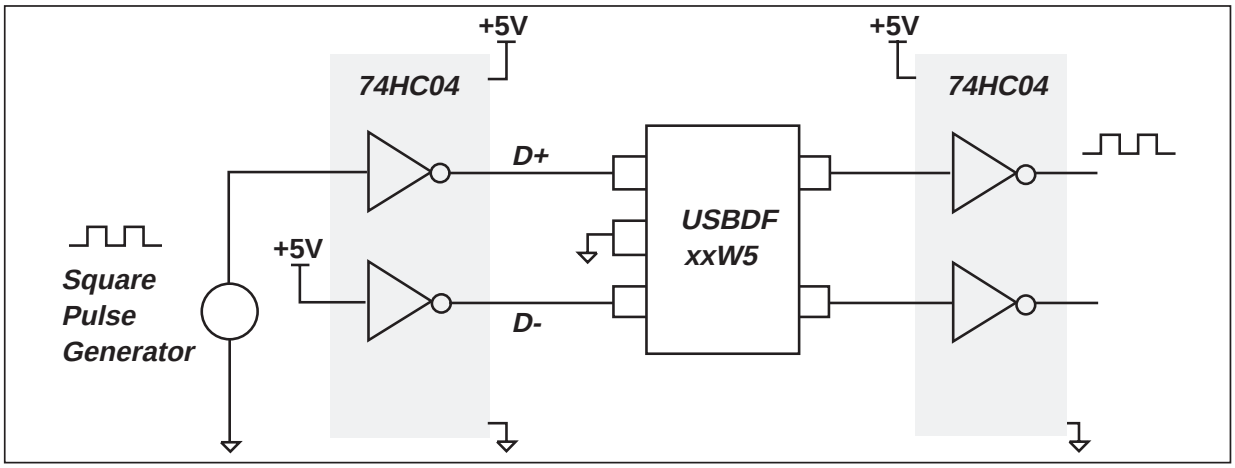
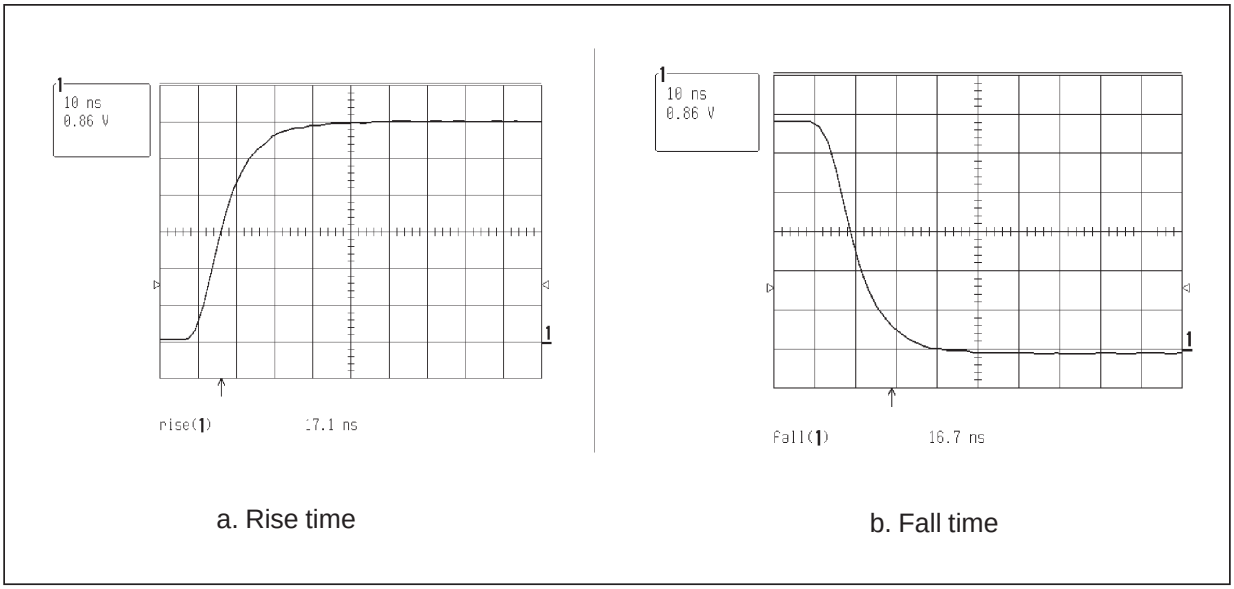


Fig. A13: Typical rise and fall times

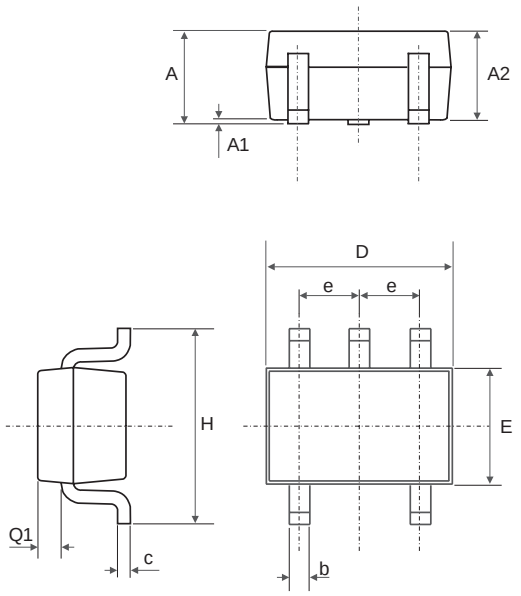


a. Rise time

b. Fall time

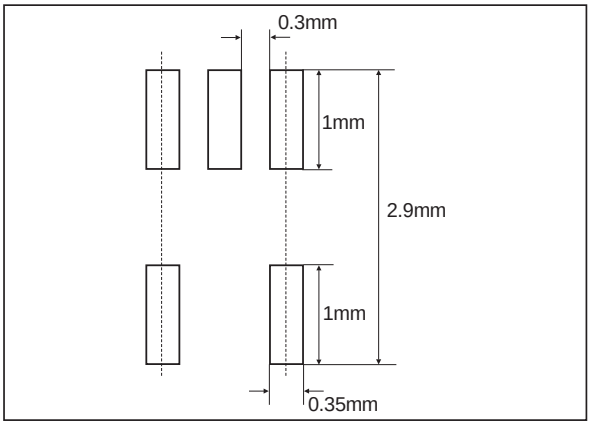
PACKAGE MECHANICAL DATA.

SOT323-5L



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.8	1.1	0.031	0.043
A1	0	0.1	0	0.004
A2	0.8	1	0.031	0.039
b	0.15	0.3	0.006	0.012
c	0.1	0.18	0.004	0.007
D	1.8	2.2	0.071	0.086
E	1.15	1.35	0.045	0.053
e	0.65 Typ.		0.025 Typ.	
H	1.8	2.4	0.071	0.094
Q1	0.1	0.4	0.004	0.016

RECOMMENDED FOOTPRINT (mm)



MECHANICAL SPECIFICATIONS

Lead plating	Tin-lead
Lead plating thickness	5µm min 25µm max
Lead material	Sn / Pb (70% to 90%Sn)
Lead coplanarity	10µm max
Body material	Molded epoxy
Flammability	UL94V-0

MARKING

Type	Order Code	Weight	Marking	Package	Base Qty
USBDF01W5	USBDF01W5	5.4mg	UD1	SOT323-5L	3000
USBDF02W5	USBDF02W5		UD2		

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