



# VN750 / VN750S VN750PT / VN750-B5

## HIGH SIDE DRIVER


TYPE	R <sub>DS(on)</sub>	I <sub>OUT</sub>	V <sub>CC</sub>
VN750 VN750S VN750PT VN750-B5	60 mΩ	6 A	36 V

- CMOS COMPATIBLE INPUT
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (\*)


### DESCRIPTION

The VN750, VN750S, VN750PT, VN750-B5 are a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

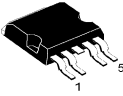
Active V<sub>CC</sub> pin voltage clamp protects the device against low energy spikes (see ISO7637 transient



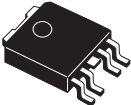
**SO-8**



**PENTAWATT**



**P<sup>2</sup>PAK**



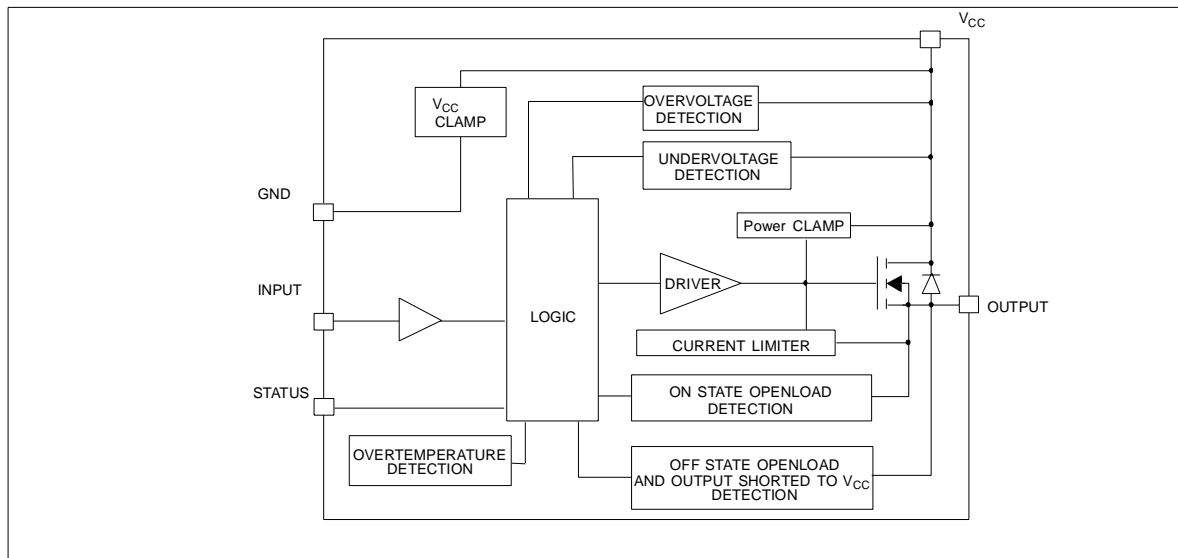
**PPAK**

ORDER CODES		
PACKAGE	TUBE	T&R
PENTAWATT	VN750	-
SO-8	VN750S	VN750S13TR
P <sup>2</sup> PAK	VN750-B5	VN750-B513TR
PPAK	VN750PT	VN750PT13TR

compatibility table). Active current limitation combined with thermal shutdown and automatic restart protect the device against overload.

The device detects open load condition both is on and off state. Output shorted to V<sub>CC</sub> is detected in the off state. Device automatically turns off in case of ground pin disconnection.

### BLOCK DIAGRAM



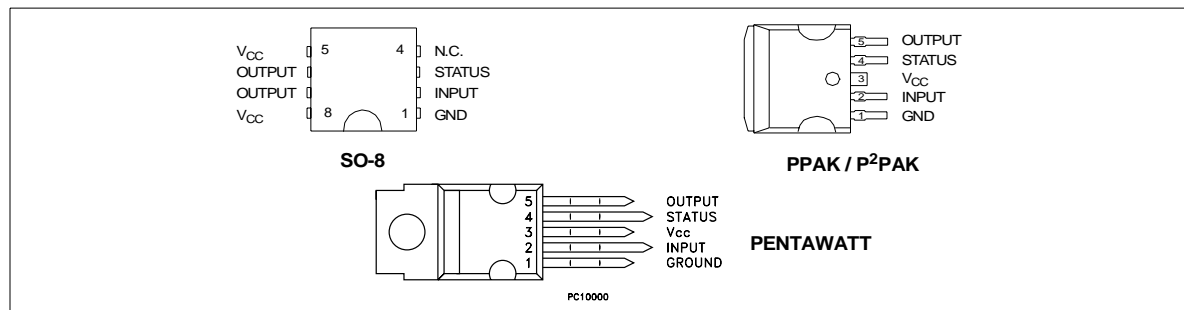
(\*) See application schematic at page 8

## VN750 / VN750S / VN750PT / VN750-B5

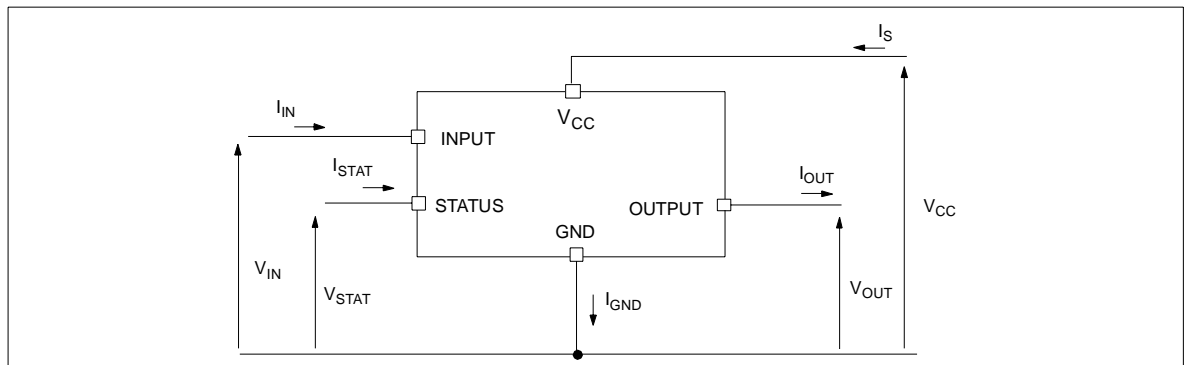
### ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value				Unit
		SO-8	PENTAWATT	P <sup>2</sup> PAK	PPAK	
$V_{CC}$	DC Supply Voltage	41				V
$-V_{CC}$	Reverse DC Supply Voltage	- 0.3				V
$-I_{gnd}$	DC Reverse Ground Pin Current	- 200				mA
$I_{OUT}$	DC Output Current	Internally Limited				A
$-I_{OUT}$	Reverse DC Output Current	- 6				A
$I_{IN}$	DC Input Current	+/- 10				mA
$I_{STAT}$	DC Status Current	+/- 10				mA
$V_{ESD}$	Electrostatic Discharge (Human Body Model: R=1.5K $\Omega$ ; C=100pF)					
	- INPUT	4000				V
	- STATUS	4000				V
	- OUTPUT	5000				V
	- $V_{CC}$	5000				V
$E_{MAX}$	Maximum Switching Energy (L=1.8mH; R <sub>L</sub> =0 $\Omega$ ; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150 $^{\circ}$ C; I <sub>L</sub> =9A)	100				mJ
$E_{MAX}$	Maximum Switching Energy (L=2.46mH; R <sub>L</sub> =0 $\Omega$ ; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150 $^{\circ}$ C; I <sub>L</sub> =9A)			138	138	mJ
$P_{tot}$	Power Dissipation T <sub>C</sub> =25 $^{\circ}$ C	4.2	60	60	60	W
$T_j$	Junction Operating Temperature	Internally Limited				$^{\circ}$ C
$T_c$	Case Operating Temperature	- 40 to 150				$^{\circ}$ C
$T_{stg}$	Storage Temperature	- 55 to 150				$^{\circ}$ C

### CONNECTION DIAGRAM (TOP VIEW)



### CURRENT AND VOLTAGE CONVENTIONS



## THERMAL DATA

Symbol	Parameter	Max	Value				Unit
			S0-8	PENTAWATT	P <sup>2</sup> PAK	PPAK	
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	-	2.1	2.1	2.1	°C/W
R <sub>thj-lead</sub>	Thermal Resistance Junction-lead	Max	30	-	-	-	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	93 (*)	62.1	52.1 (**)	77.1 (**)	°C/W

(\*) When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35µm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.

(\*\*) When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35µm thick). Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C unless otherwise specified)

## POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	Operating Supply Voltage		5.5	13	36	V
V <sub>USD</sub>	Undervoltage Shut-down		3	4	5.5	V
V <sub>USDhyst</sub>	Undervoltage Shut-down Hysteresis			0.5		V
V <sub>OV</sub>	Overvoltage Shut-down		36			V
R <sub>ON</sub>	On State Resistance	I <sub>OUT</sub> =2A; T <sub>j</sub> =25°C; V <sub>CC</sub> >8V I <sub>OUT</sub> =2A; V <sub>CC</sub> >8V		(#)	60 120	mΩ mΩ
I <sub>S</sub>	Supply Current	Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V; T <sub>j</sub> =25°C On State; V <sub>CC</sub> =13V; V <sub>IN</sub> =5V; I <sub>OUT</sub> =0A		10 10 2	25 20 3.5	µA µA mA
I <sub>L(off1)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V	0	(#)	50	µA
I <sub>L(off2)</sub>	Off State Output Current	V <sub>IN</sub> =0V; V <sub>OUT</sub> =3.5V	-75		0	µA
I <sub>L(off3)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =125°C			5	µA
I <sub>L(off4)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C			3	µA

SWITCHING (V<sub>CC</sub>=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	R <sub>L</sub> =6.5Ω from V <sub>IN</sub> rising edge to V <sub>OUT</sub> =1.3V		40		µs
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>L</sub> =6.5Ω from V <sub>IN</sub> falling edge to V <sub>OUT</sub> =11.7V		30		µs
dV <sub>OUT</sub> /dt <sub>(on)</sub>	Turn-on Voltage Slope	R <sub>L</sub> =6.5Ω from V <sub>OUT</sub> =1.3V to V <sub>OUT</sub> =10.4V		(#)		V/µs
dV <sub>OUT</sub> /dt <sub>(off)</sub>	Turn-off Voltage Slope	R <sub>L</sub> =6.5Ω from V <sub>OUT</sub> =11.7V to V <sub>OUT</sub> =1.3V		(#)		V/µs

## INPUT PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input Low Level			(#)	1.25	V
I <sub>IL</sub>	Low Level Input Current	V <sub>IN</sub> =1.25V	1	(#)		µA
V <sub>IH</sub>	Input High Level		3.25	(#)		V
I <sub>IH</sub>	High Level Input Current	V <sub>IN</sub> =3.25V		(#)	10	µA
V <sub>hyst</sub>	Input Hysteresis Voltage		0.5	(#)		V
V <sub>ICL</sub>	Input Clamp Voltage	I <sub>IN</sub> =1mA I <sub>IN</sub> =-1mA	6	6.8 -0.7	8	V V

(#) See relative diagram

## VN750 / VN750S / VN750PT / VN750-B5

### ELECTRICAL CHARACTERISTICS (continued)

#### STATUS PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{STAT}$	Status Low Output Voltage	$I_{STAT}=1.6mA$		(#)	0.5	V
$I_{LSTAT}$	Status Leakage Current	Normal Operation; $V_{STAT}=5V$		(#)	10	$\mu A$
$C_{STAT}$	Status Pin Input Capacitance	Normal Operation; $V_{STAT}=5V$			100	pF
$V_{SCL}$	Status Clamp Voltage	$I_{STAT}=1mA$	6	6.8	8	V
		$I_{STAT}=-1mA$		-0.7		V

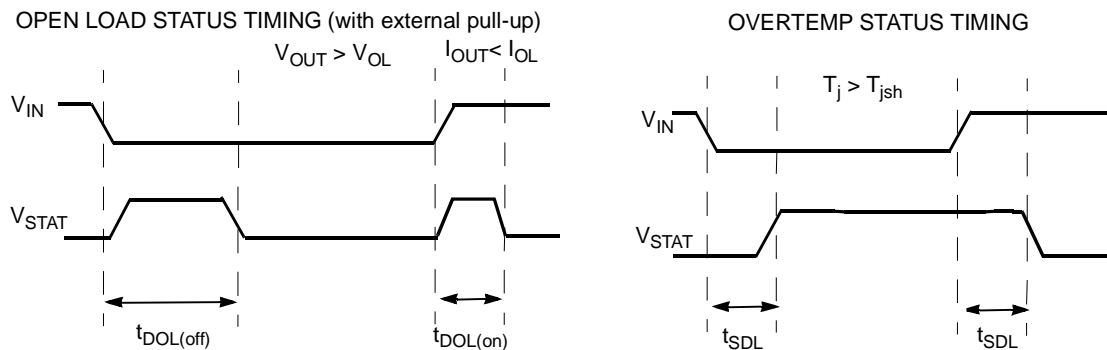
#### PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{TSD}$	Shut-down Temperature		150	175	200	$^{\circ}C$
$T_R$	Reset Temperature		135			$^{\circ}C$
$T_{hyst}$	Thermal Hysteresis		7	15		$^{\circ}C$
$t_{SDL}$	Status delay in overload condition	$T_j > T_{jsh}$			20	$\mu s$
$I_{lim}$	Current limitation	$9V < V_{CC} < 36V$	6	9	15	A
		$5V < V_{CC} < 36V$			15	A
$V_{demag}$	Turn-off Output Clamp Voltage	$I_{OUT}=2A$ ; $V_{IN}=0V$ ; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V

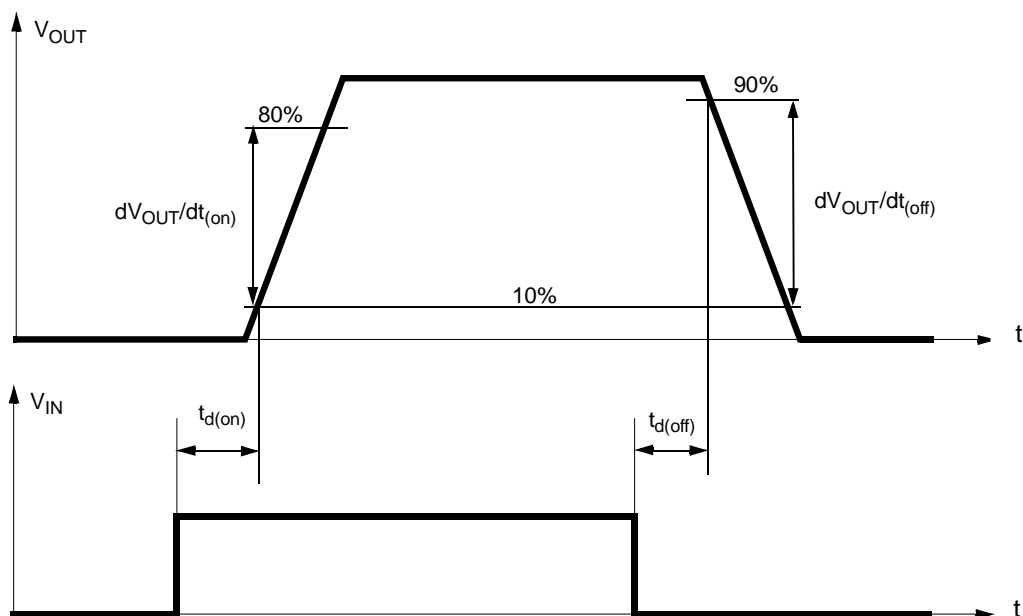
#### OPENLOAD DETECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{OL}$	Openload ON State Detection Threshold	$V_{IN}=5V$	50	(#)	200	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT}=0A$			200	$\mu s$
$V_{OL}$	Openload OFF State Voltage Detection Threshold	$V_{IN}=0V$	1.5	(#)	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	$\mu s$

(#) See relative diagram



Switching time Waveforms



TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H
	H	X	$(T_j > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output Voltage > $V_{OL}$	L	H	L
	H	H	H
Output Current < $I_{OL}$	L	L	H
	H	H	L

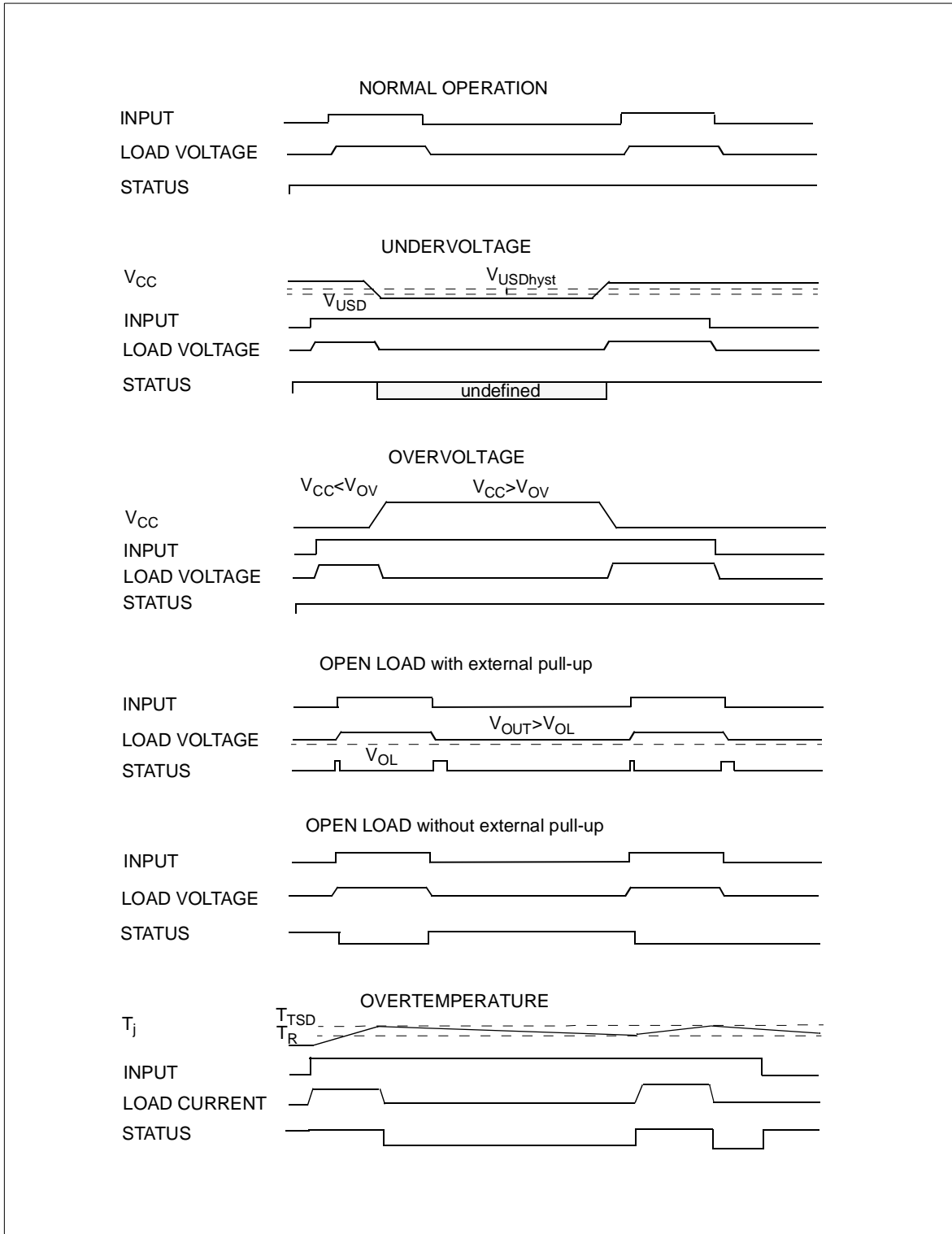
**ELECTRICAL TRANSIENT REQUIREMENTS ON V<sub>CC</sub> PIN**

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

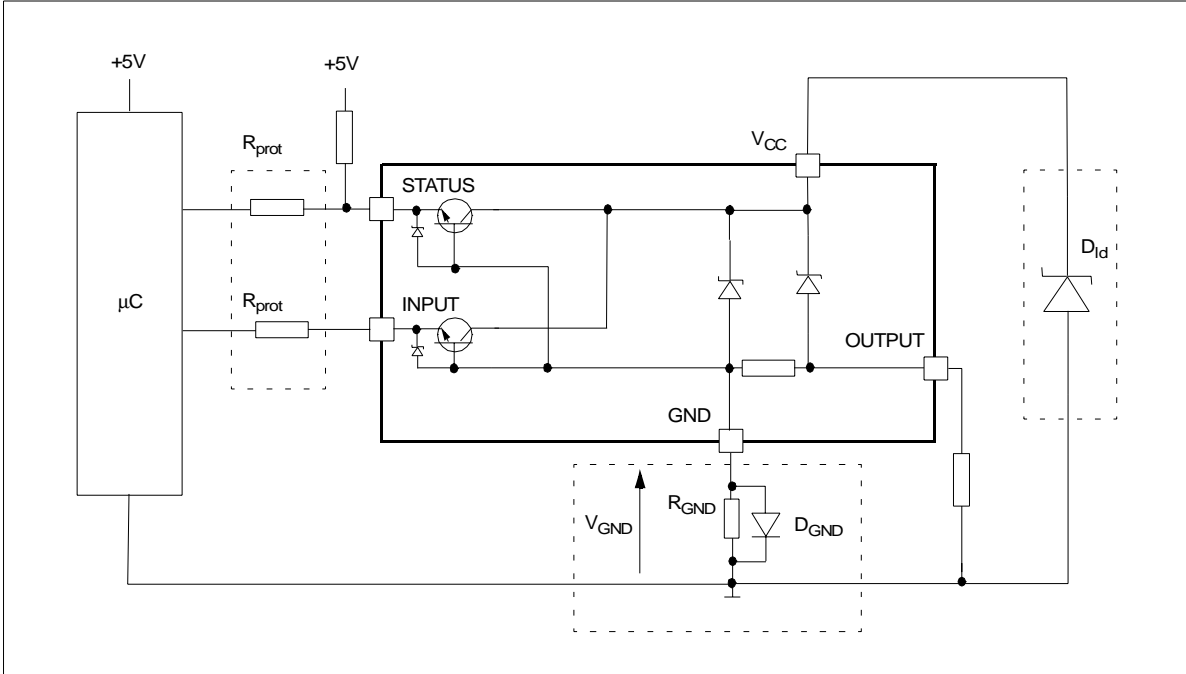
ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
<b>C</b>	All functions of the device are performed as designed after exposure to disturbance.
<b>E</b>	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 1: Waveforms



APPLICATION SCHEMATIC



**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

**Solution 1:** Resistor in the ground line (R<sub>GND</sub> only). This can be used with any type of load.

The following is an indication on how to dimension the R<sub>GND</sub> resistor.

- 1)  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I<sub>GND</sub> is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R<sub>GND</sub> (when V<sub>CC</sub><0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where I<sub>S(on)max</sub> becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R<sub>GND</sub> will produce a shift (I<sub>S(on)max</sub> \* R<sub>GND</sub>) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R<sub>GND</sub>.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

**Solution 2:** A diode (D<sub>GND</sub>) in the ground line.

A resistor (R<sub>GND</sub>=1kΩ) should be inserted in parallel to D<sub>GND</sub> if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

**LOAD DUMP PROTECTION**

D<sub>Id</sub> is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V<sub>CC</sub> max DC rating. The same applies if the device will be subject to transients on the V<sub>CC</sub> line that are greater than the ones shown in the ISO T/R 7637/1 table.

**µC I/Os PROTECTION:**

If a ground protection network is used and negative transients are present on the V<sub>CC</sub> line, the control pins will be pulled negative. ST suggests to insert a resistor (R<sub>prot</sub>) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V<sub>CCpeak</sub>= - 100V and I<sub>latchup</sub> ≥ 20mA; V<sub>OHµC</sub> ≥ 4.5V

$$5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$$

Recommended R<sub>prot</sub> value is 10kΩ.

### OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor ( $R_{PU}$ ) connected between OUTPUT pin and a positive supply voltage ( $V_{PU}$ ) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

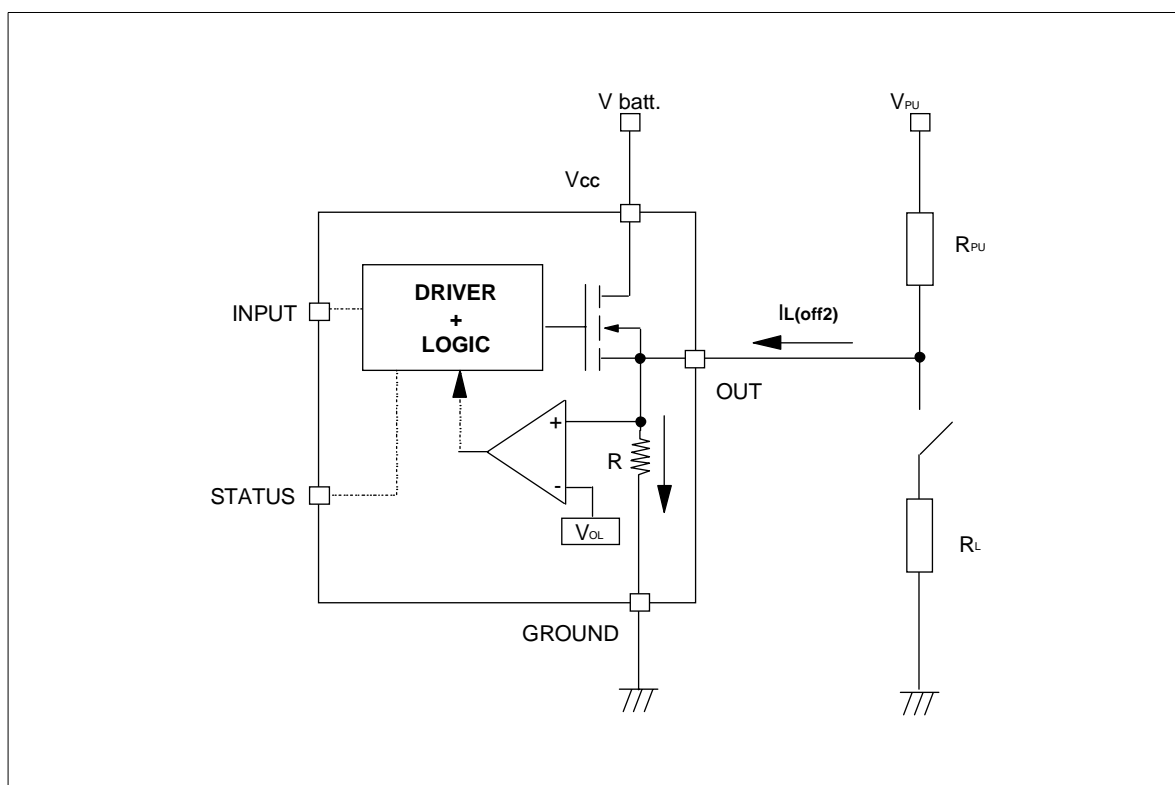
- 1) no false open load indication when load is connected: in this case we have to avoid  $V_{OUT}$  to be higher than  $V_{OLmin}$ ; this results in the following condition  $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$ .

- 2) no misdetection when load is disconnected: in this case the  $V_{OUT}$  has to be higher than  $V_{OLmax}$ ; this results in the following condition  $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$ .

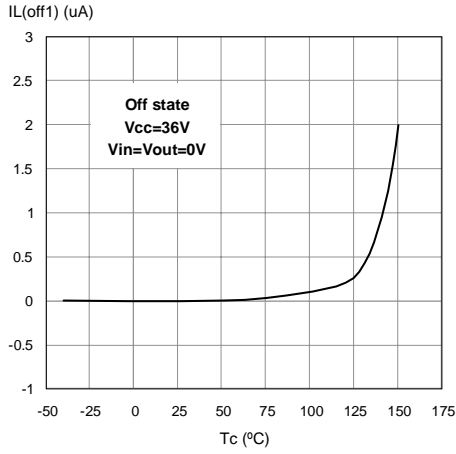
Because  $I_{S(OFF)}$  may significantly increase if  $V_{OUT}$  is pulled high (up to several mA), the pull-up resistor  $R_{PU}$  should be connected to a supply that is switched OFF when the module is in standby.

The values of  $V_{OLmin}$ ,  $V_{OLmax}$  and  $I_{L(off2)}$  are available in the Electrical Characteristics section.

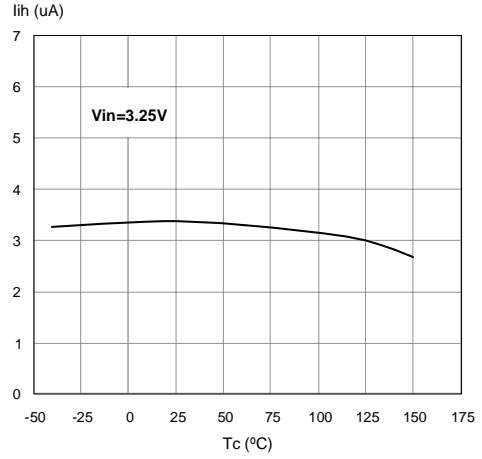
### Open Load detection in off state



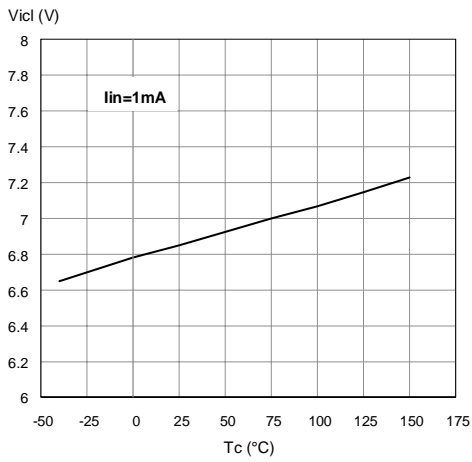
Off State Output Current



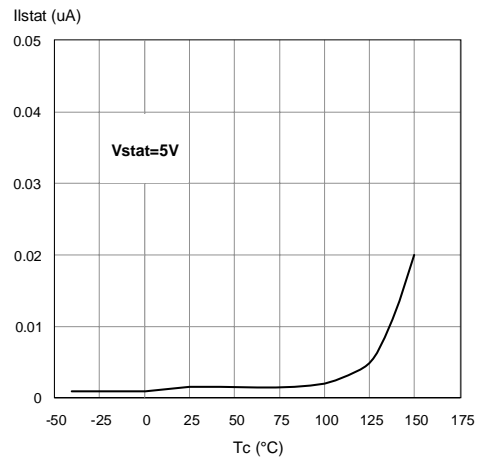
High Level Input Current



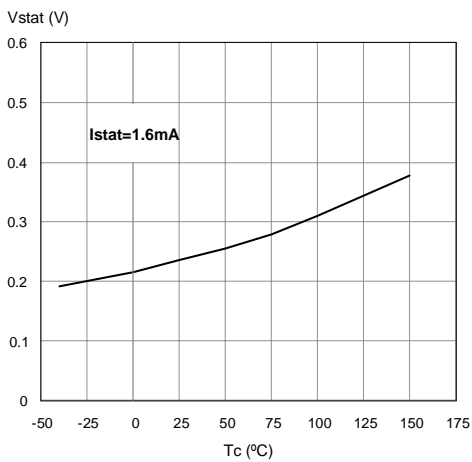
Input Clamp Voltage



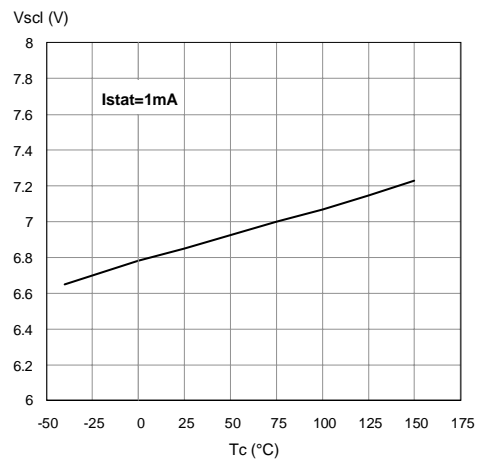
Status Leakage Current



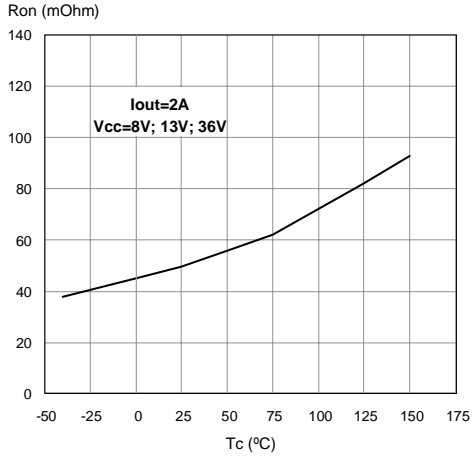
Status Low Output Voltage



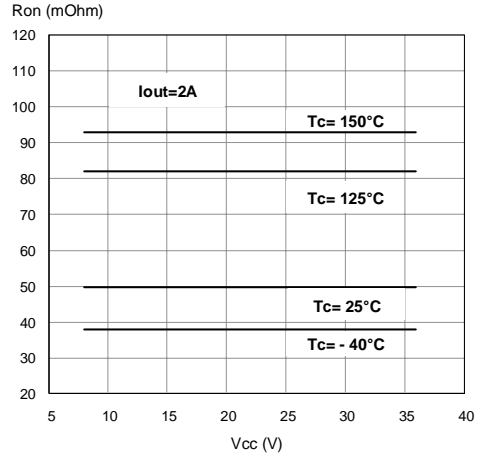
Status Clamp Voltage



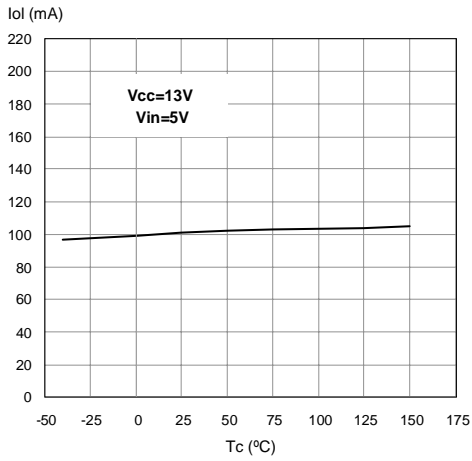
On State Resistance Vs  $T_{case}$



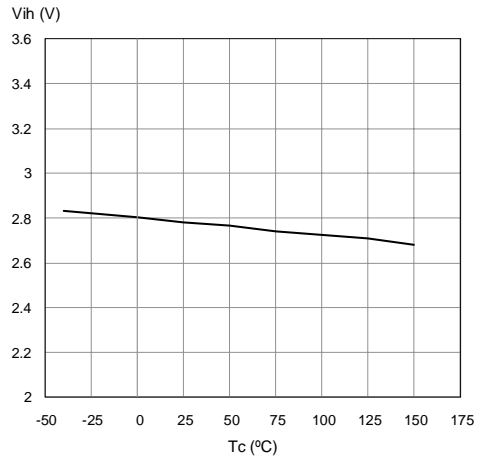
On State Resistance Vs  $V_{CC}$



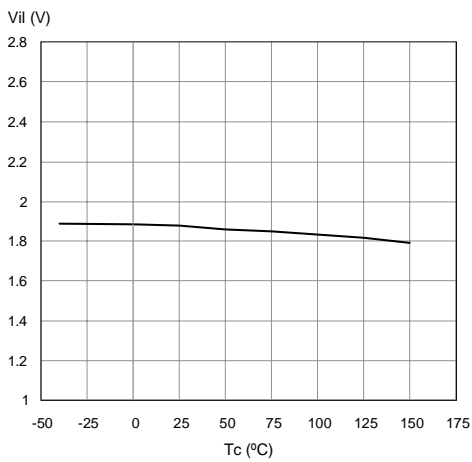
Openload On State Detection Threshold



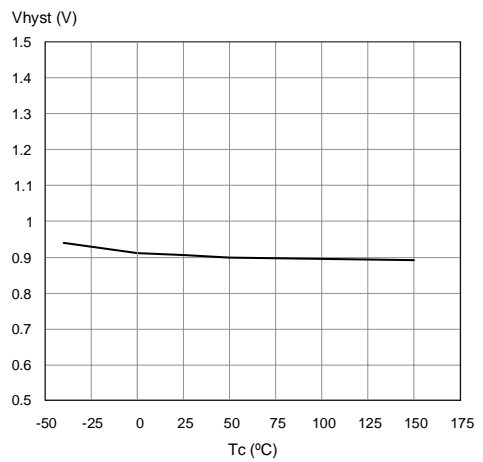
Input High Level



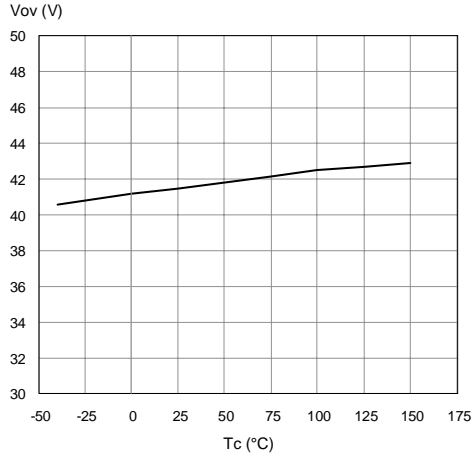
Input Low Level



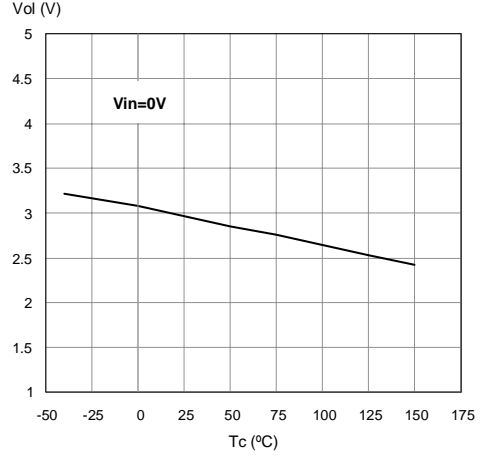
Input Hysteresis Voltage



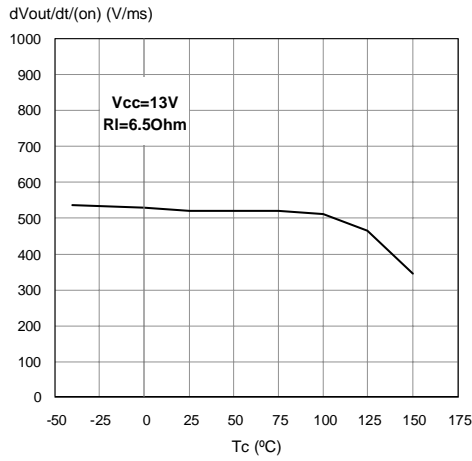
Overvoltage Shutdown



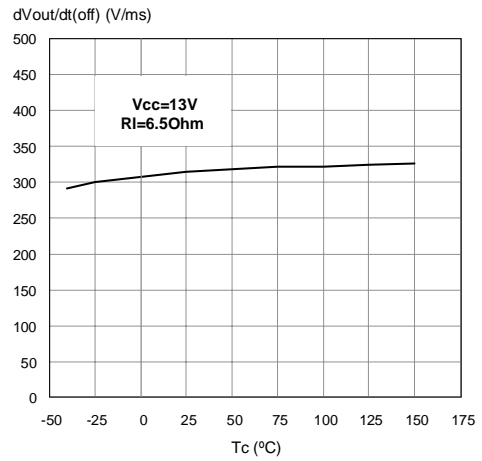
Openload Off State Voltage Detection Threshold



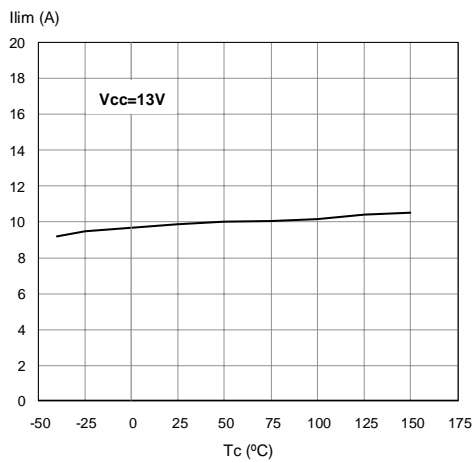
Turn-on Voltage Slope



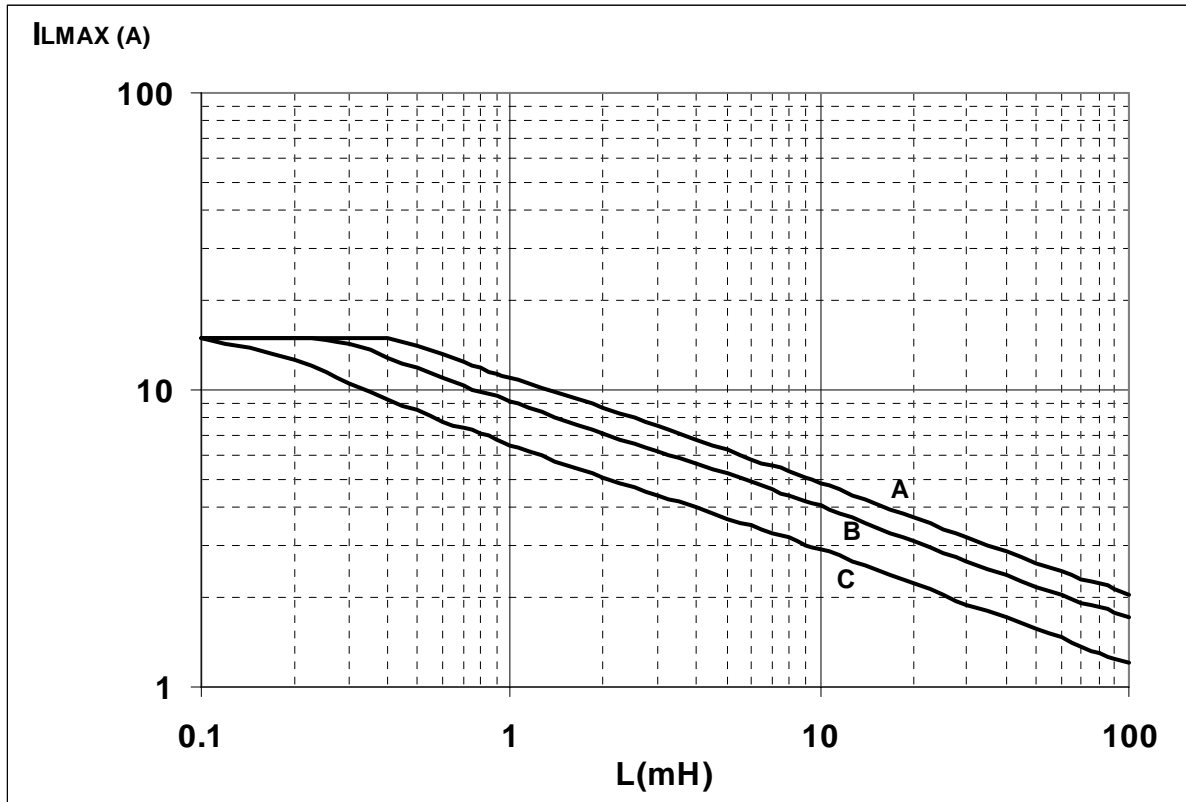
Turn-off Voltage Slope



I<sub>lim</sub> Vs T<sub>case</sub>



SO-8 Maximum turn off current versus load inductance



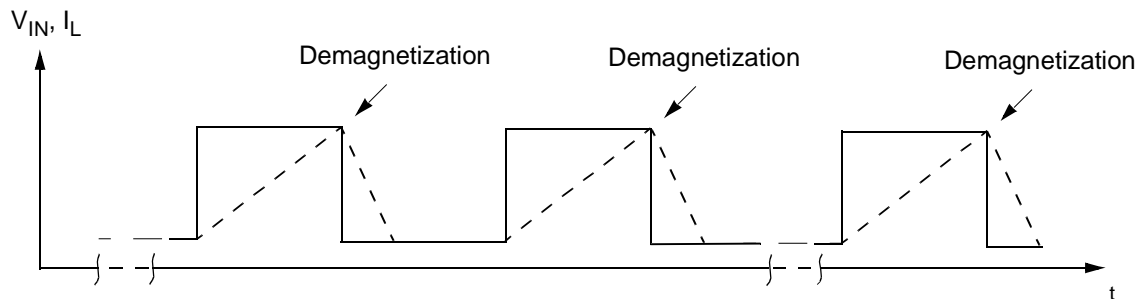
- A = Single Pulse at  $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at  $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at  $T_{Jstart}=125^{\circ}C$

Conditions:

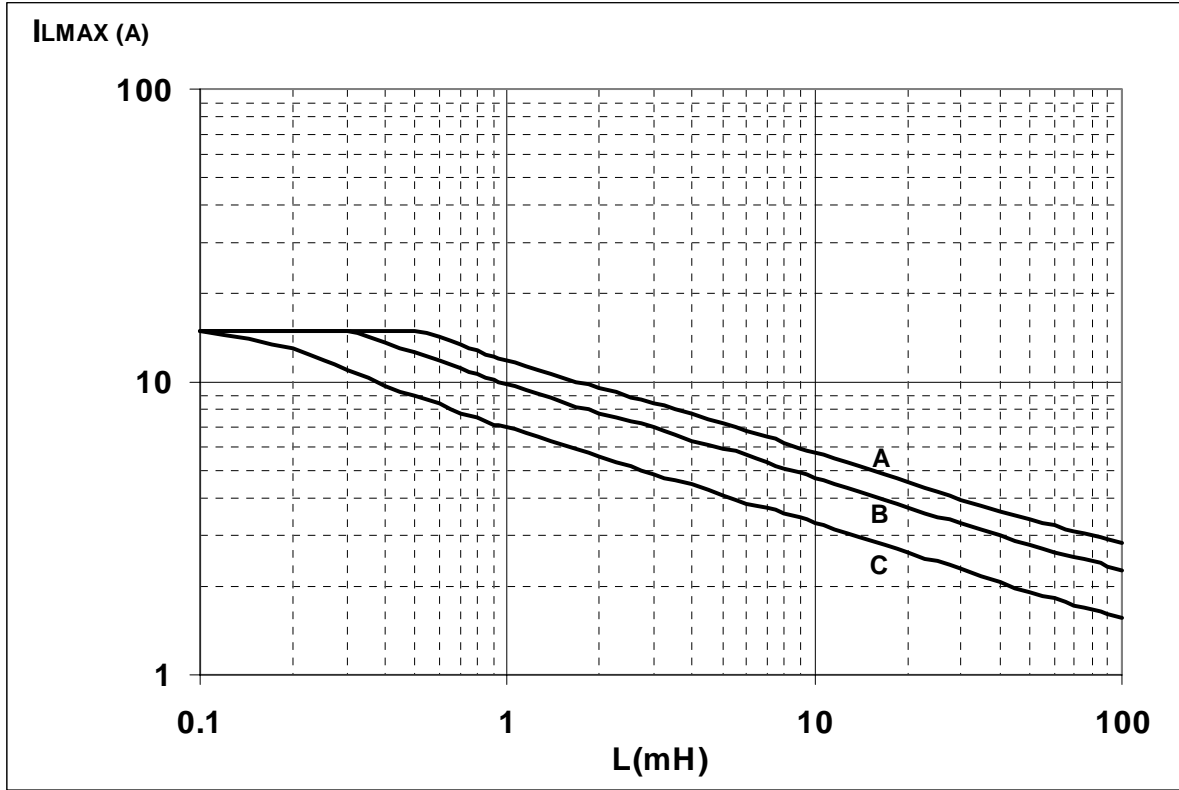
$V_{CC}=13.5V$

Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



PPAK, P<sup>2</sup>PAK Maximum turn off current versus load inductance



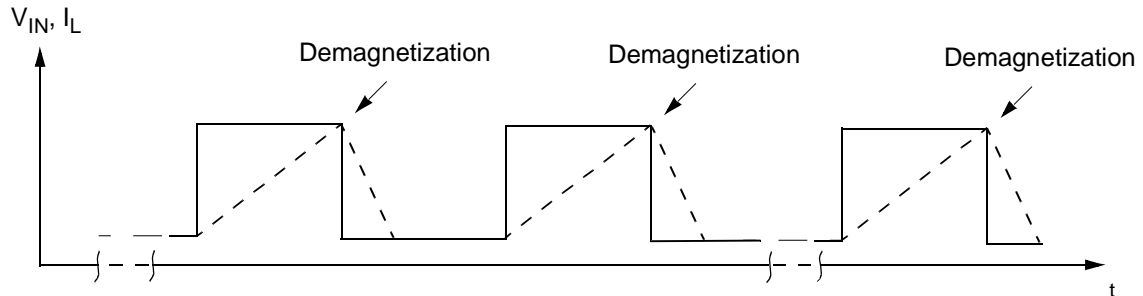
- A = Single Pulse at  $T_{jstart}=150^{\circ}C$
- B= Repetitive pulse at  $T_{jstart}=100^{\circ}C$
- C= Repetitive Pulse at  $T_{jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5V$

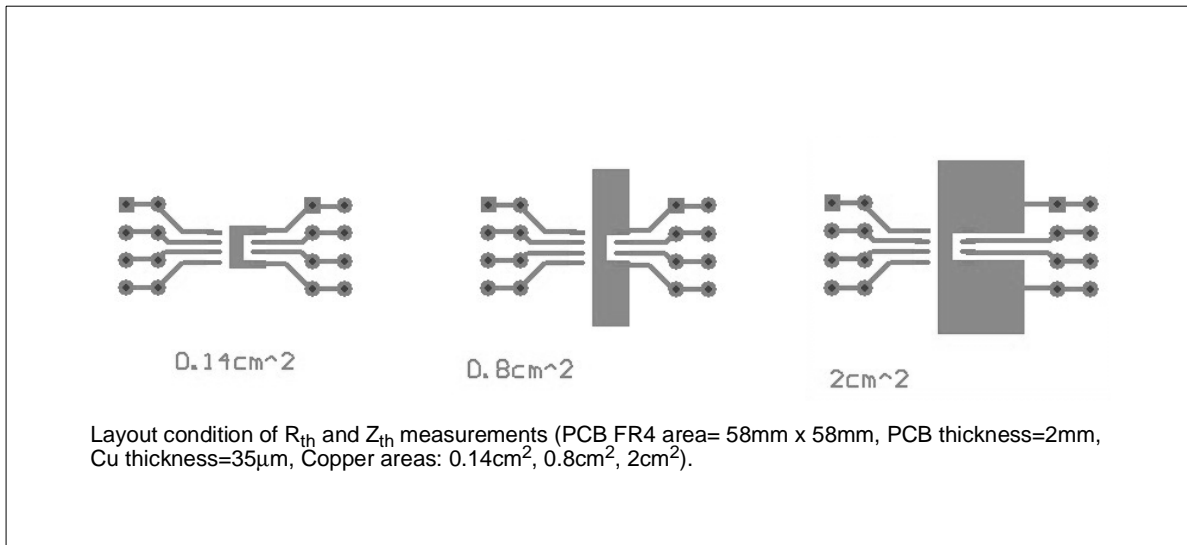
Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

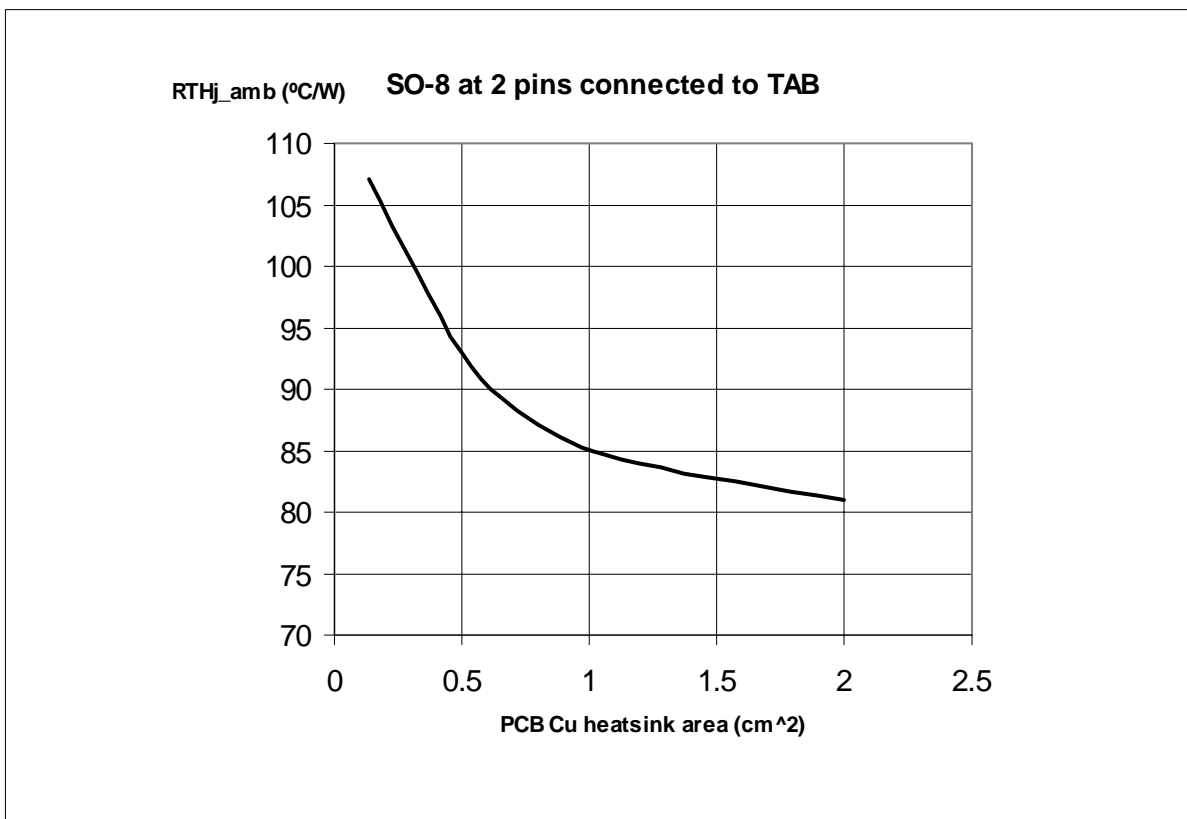


**SO-8 THERMAL DATA**

**SO-8 PC Board**

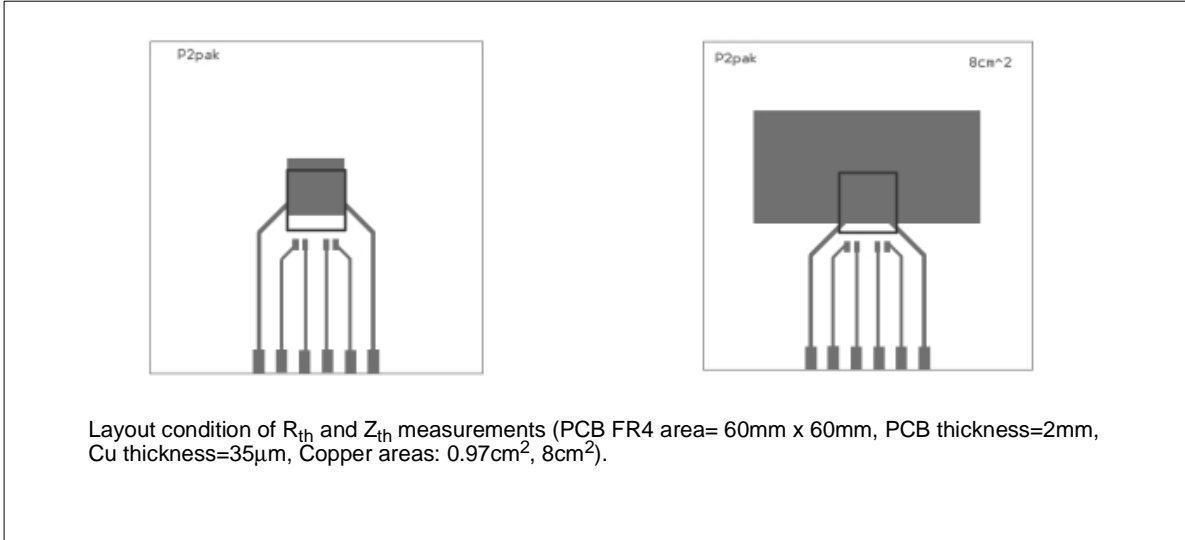


**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**

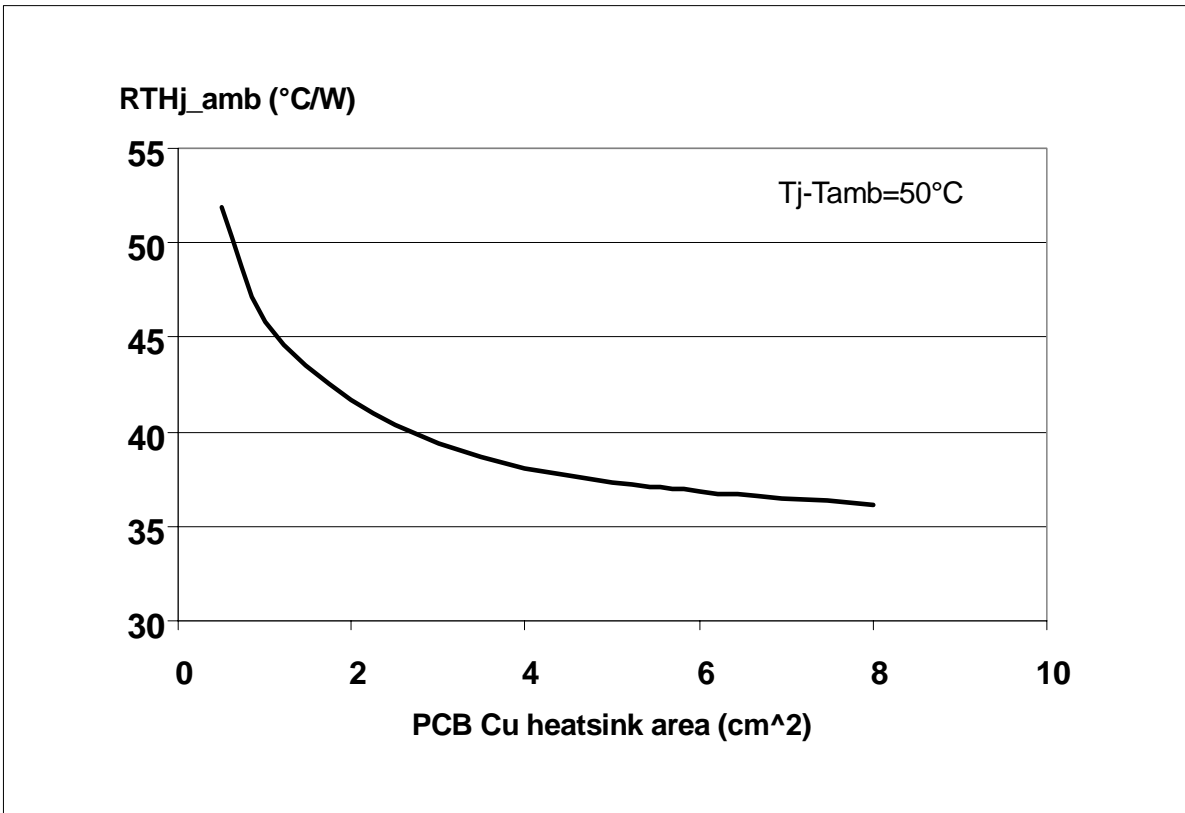


**P<sup>2</sup>PAK THERMAL DATA**

**P<sup>2</sup>PAK PC Board**

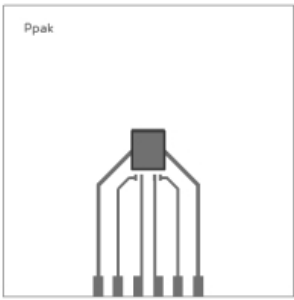


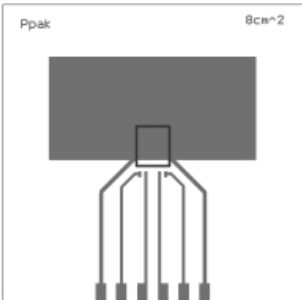
**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**



**PPAK THERMAL DATA**

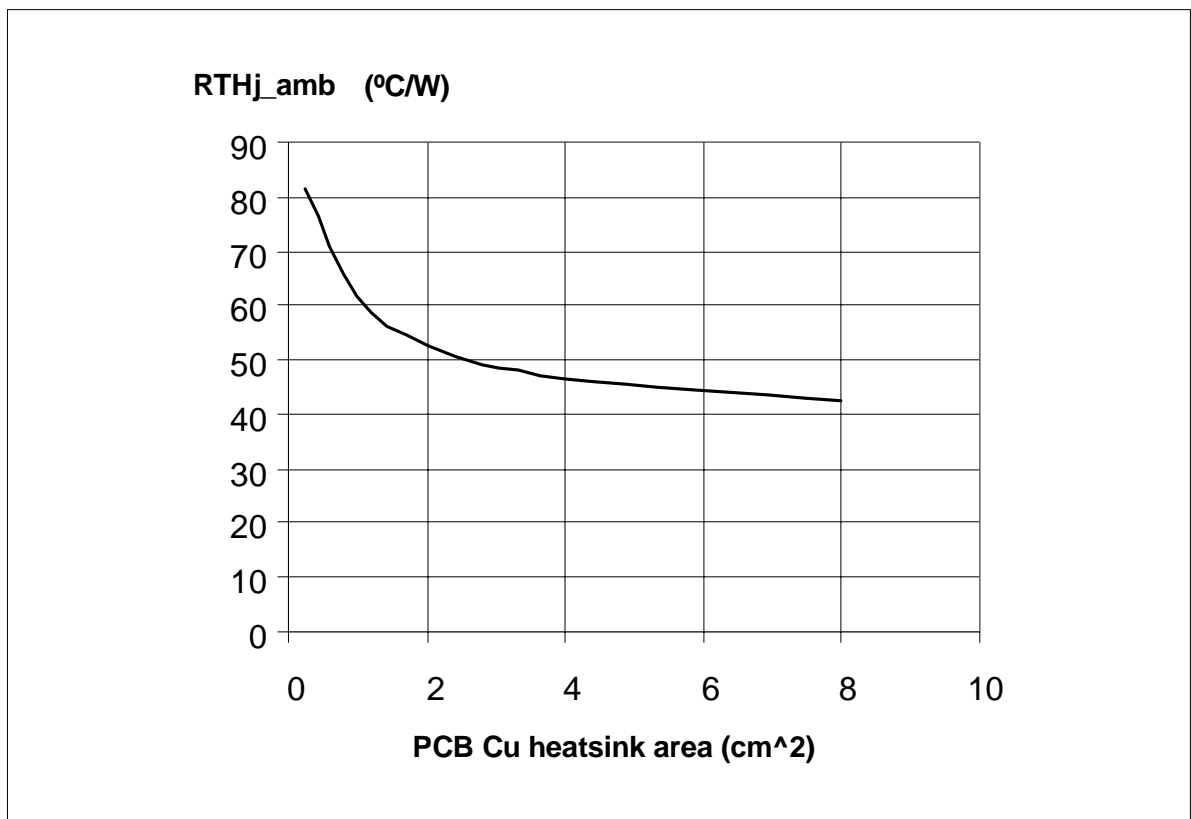
**PPAK PC Board**



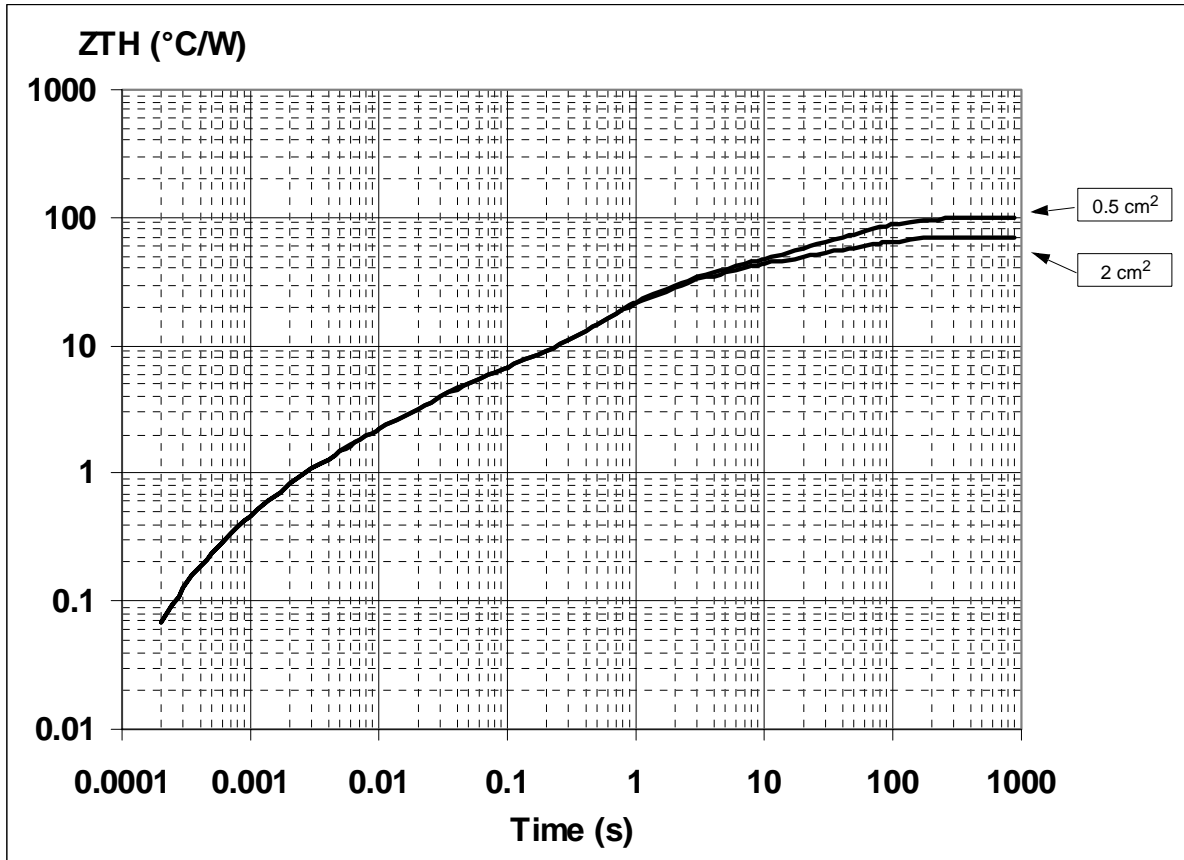


Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: 0.44cm<sup>2</sup>, 8cm<sup>2</sup>).

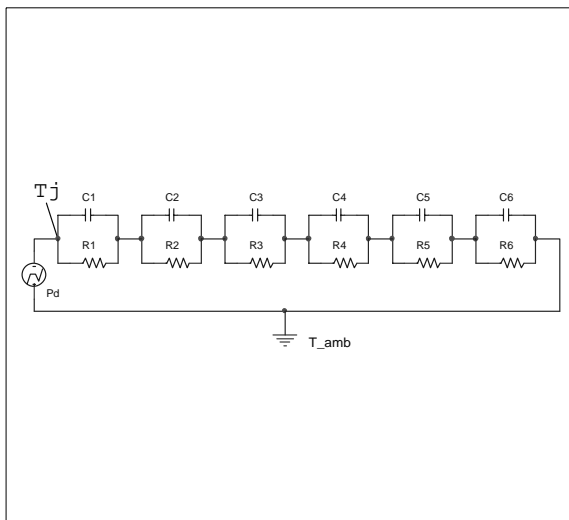
**$R_{thj-amb}$  Vs PCB copper area in open box free air condition**



SO-8 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in SO-8



Pulse calculation formula

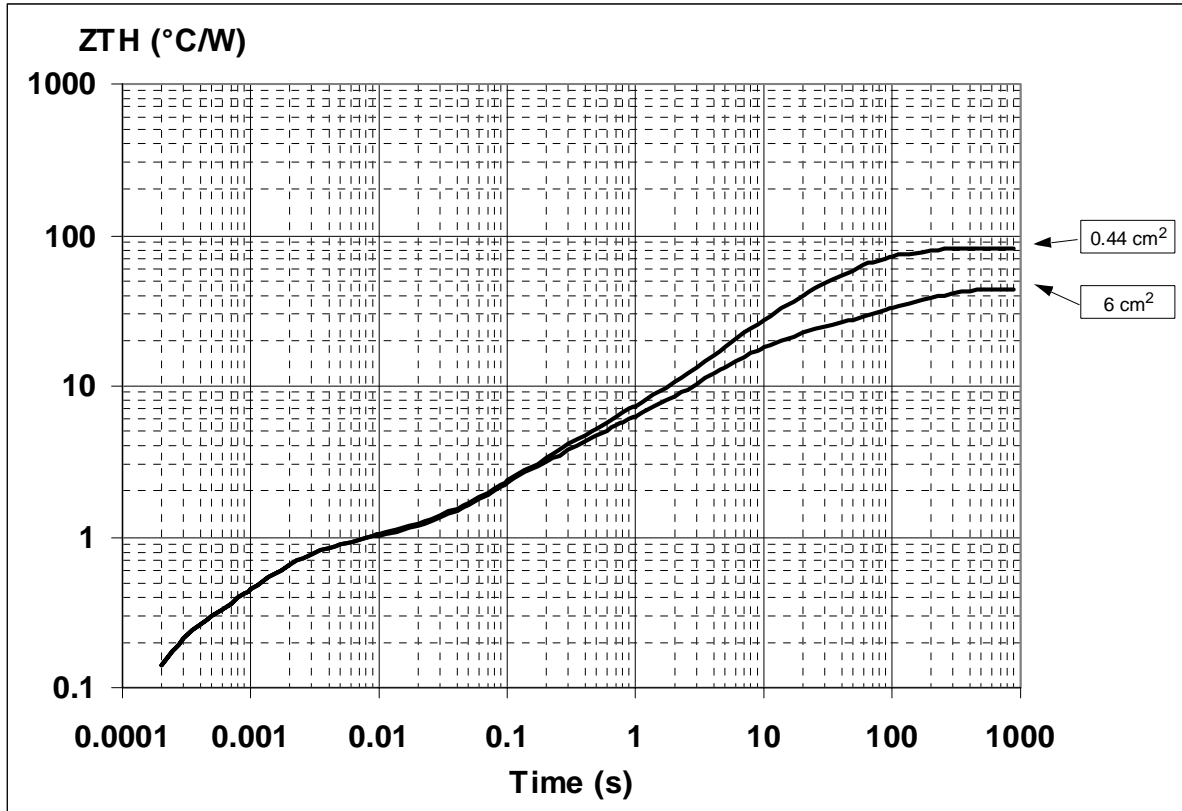
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

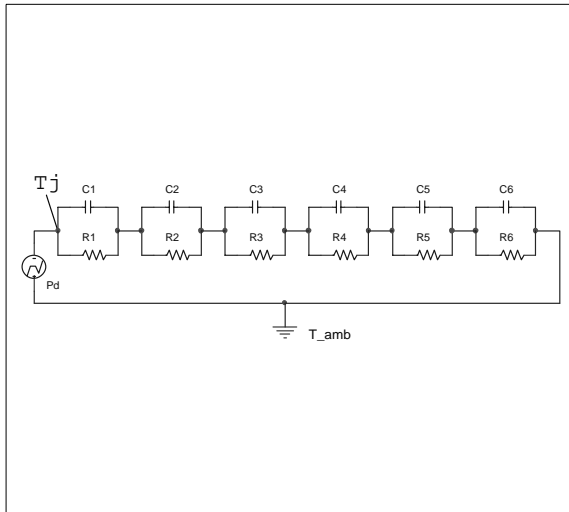
Thermal Parameter

Area/island (cm <sup>2</sup> )	0.5	2
R1 (°C/W)	0.05	
R2 (°C/W)	0.8	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.006	
C2 (W.s/°C)	2.60E-03	
C3 (W.s/°C)	0.0075	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

PPAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in PPAK



Pulse calculation formula

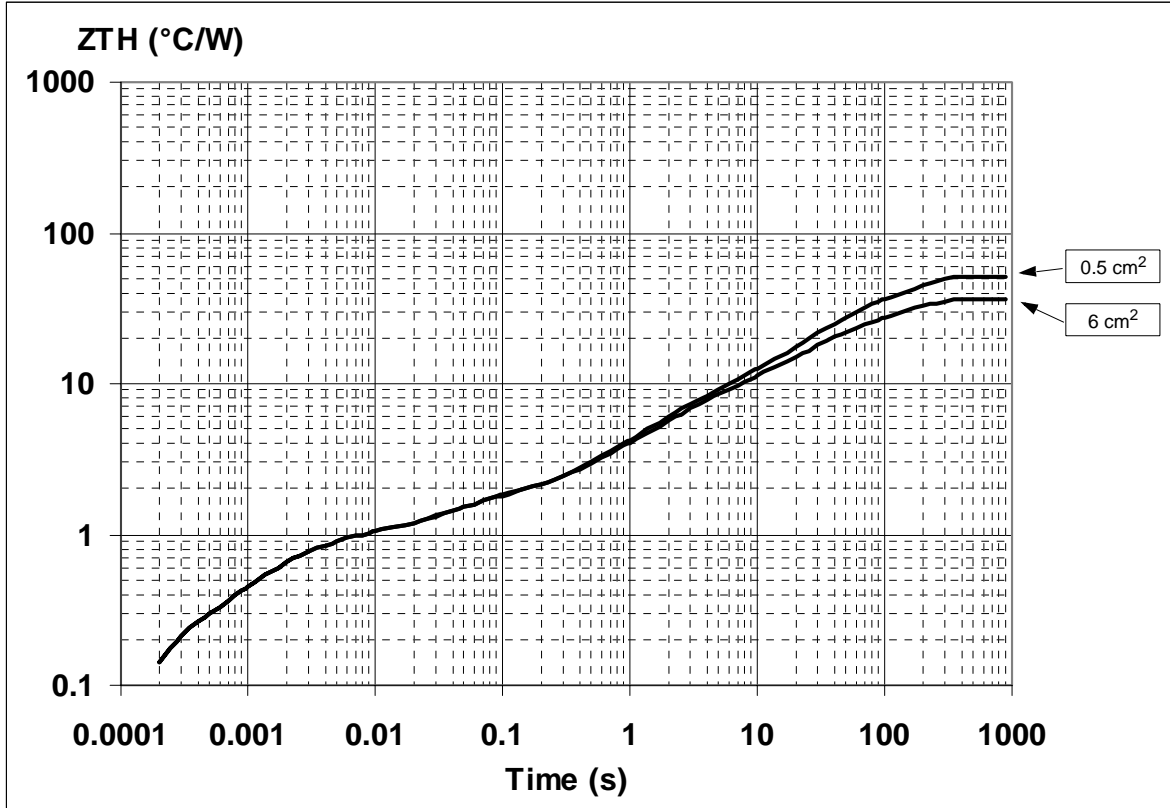
$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

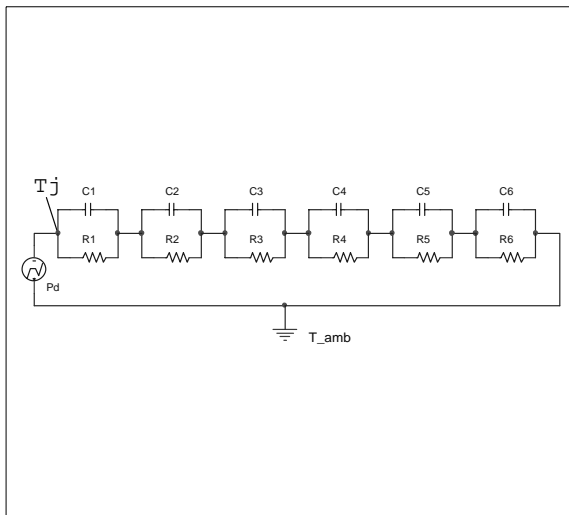
Thermal Parameter

Area/island (cm <sup>2</sup> )	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	1.6	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.08	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

P<sup>2</sup>PAK Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in P<sup>2</sup>PAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THt_p}(1 - \delta)$$

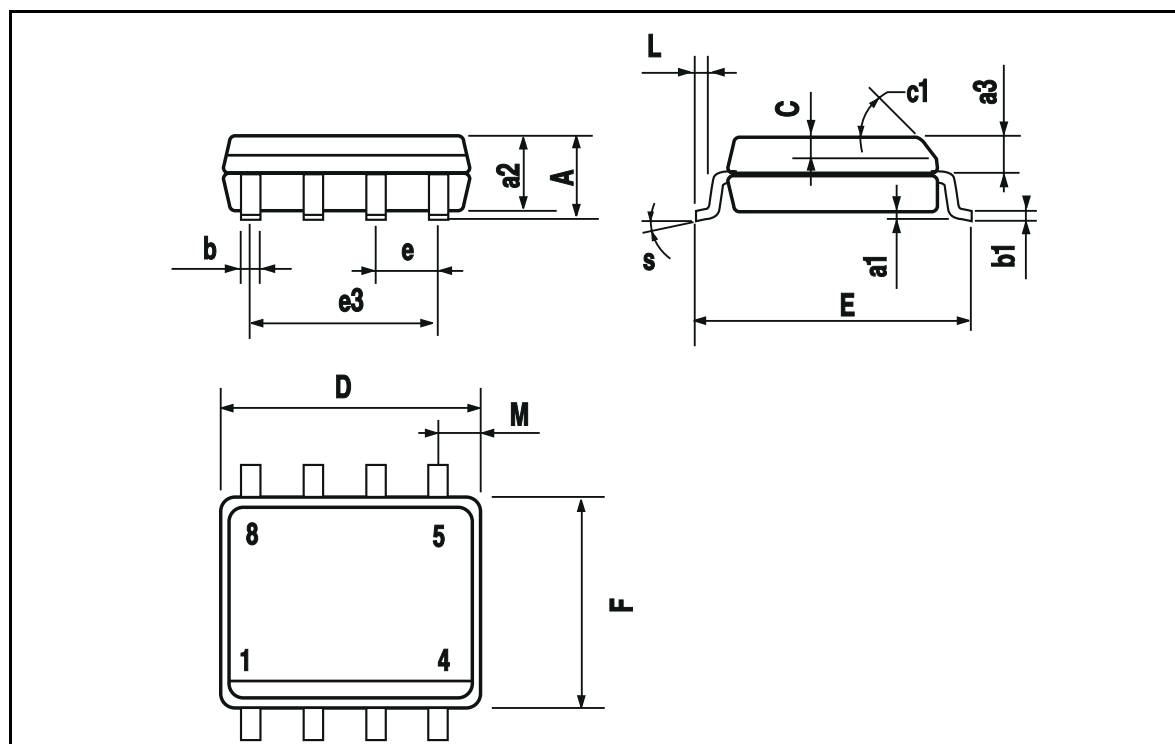
where  $\delta = t_p/T$

Thermal Parameter

Area/island (cm <sup>2</sup> )	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	0.7	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	0.0025	
C3 (W.s/°C)	0.055	
C4 (W.s/°C)	0.4	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

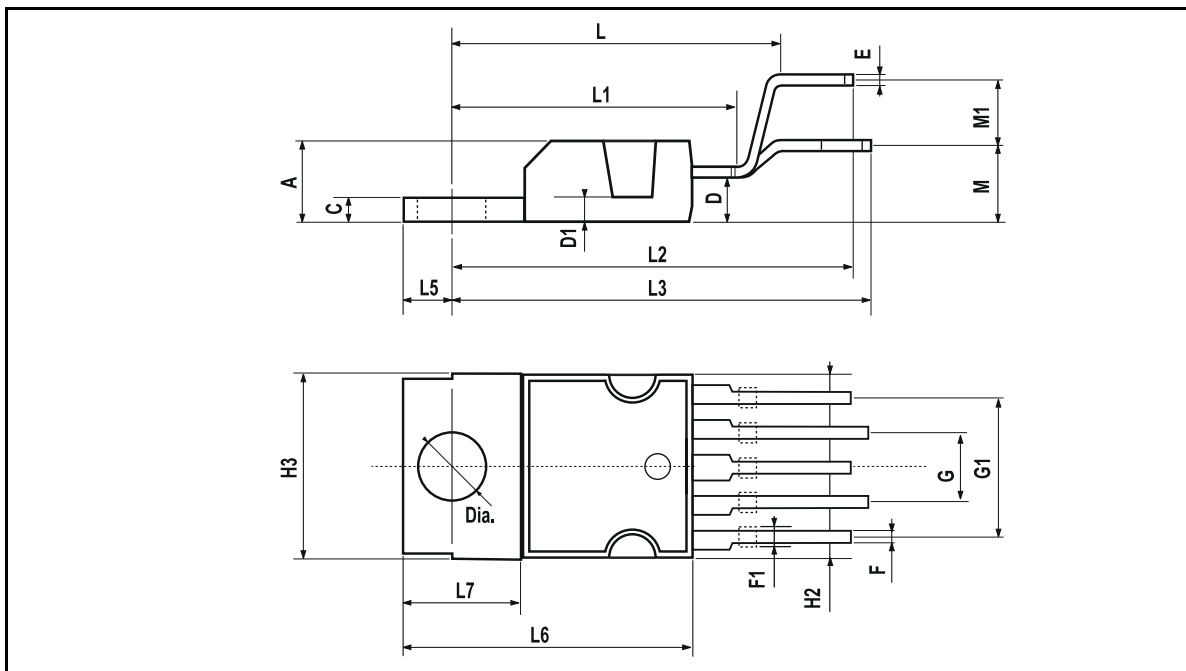
## SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					
L1	0.8		1.2	0.031		0.047



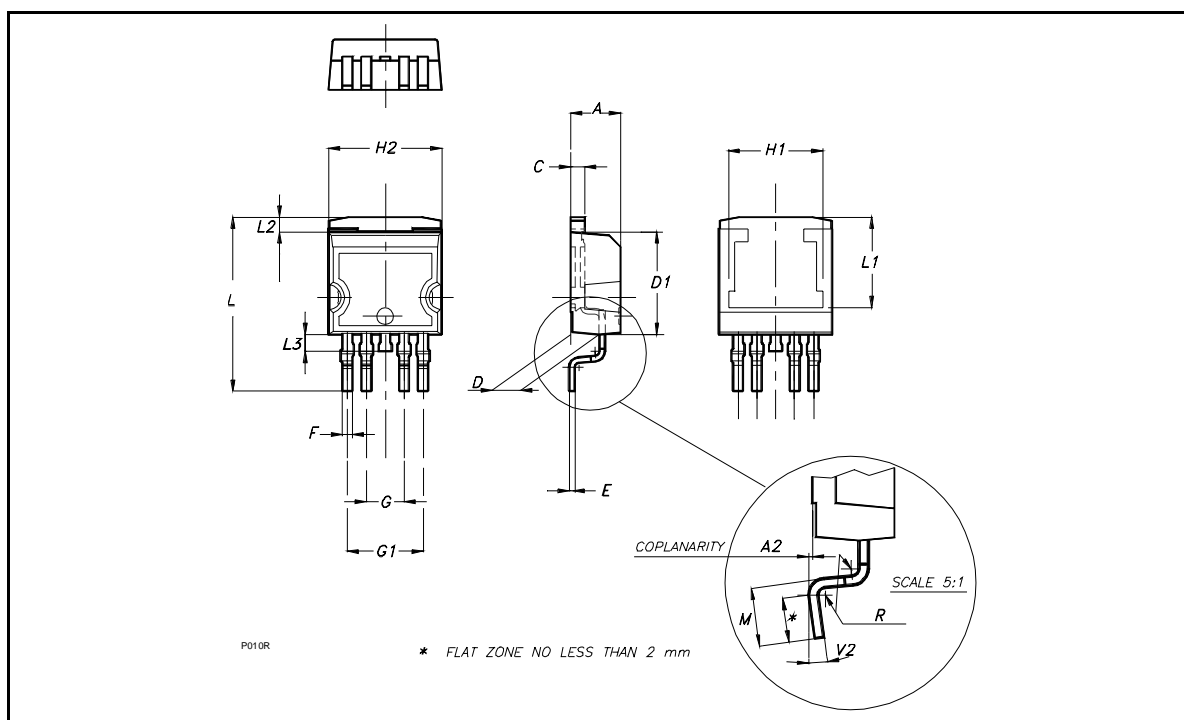
**PENTAWATT (VERTICAL) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Diam.	3.65		3.85	0.144		0.152



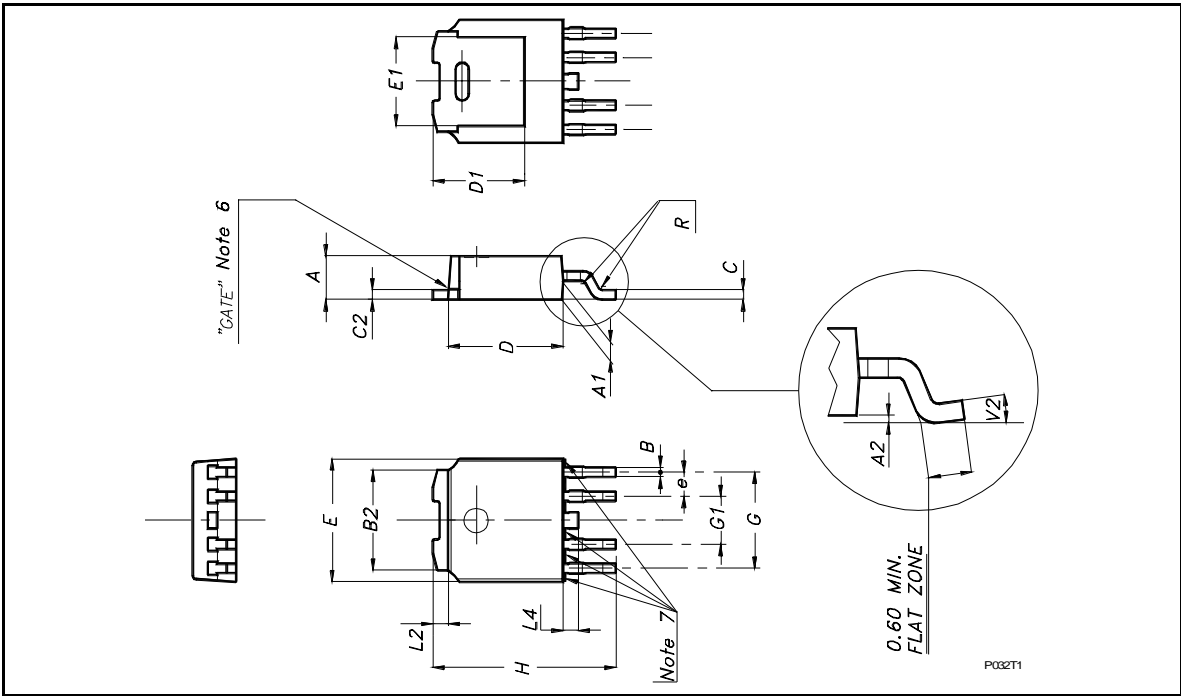
## P<sup>2</sup>PAK MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	4.30		4.80
A2	0.03		0.23
C	1.17		1.37
D	2.40		2.80
D1	8.95		9.35
E	0.45		0.60
F	0.80		1.05
G	3.20		3.60
G1	6.60		7.00
H1		8.5	
H2	10.00		10.40
L	15		15.85
L1		8	
L2	1.27		1.40
L3	1.30		1.70
M	2.40		3.20
R		0.40	
V2	0°		8°
Package Weight	1.43 Gr (typ)		

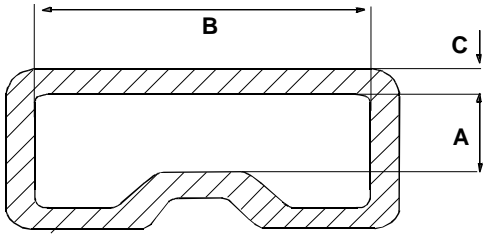


**PPAK MECHANICAL DATA**

DIM.	MIN.	TYP	MAX.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0°		8°
Package Weight	Gr. 0.3		



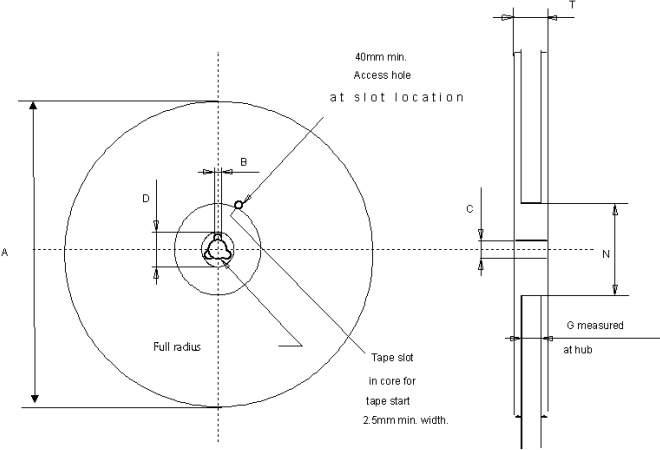
**SO-8 TUBE SHIPMENT (no suffix)**



<b>Base Q.ty</b>	100
<b>Bulk Q.ty</b>	2000
<b>Tube length (± 0.5)</b>	532
<b>A</b>	3.2
<b>B</b>	6
<b>C (± 0.1)</b>	0.6

All dimensions are in mm.

**TAPE AND REEL SHIPMENT (suffix "13TR")**



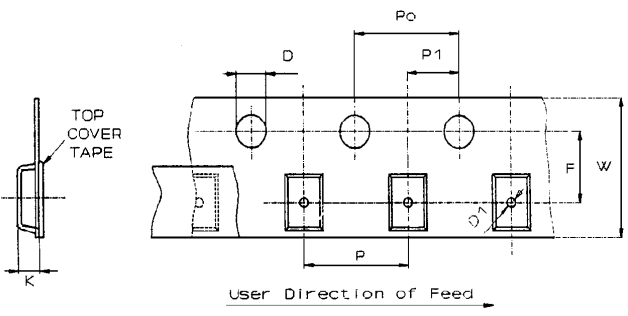
<b>Base Q.ty</b>	2500
<b>Bulk Q.ty</b>	2500
<b>A (max)</b>	330
<b>B (min)</b>	1.5
<b>C (± 0.2)</b>	13
<b>F</b>	20.2
<b>G (+ 2 / -0)</b>	12.4
<b>N (min)</b>	60
<b>T (max)</b>	18.4

All dimensions are in mm.

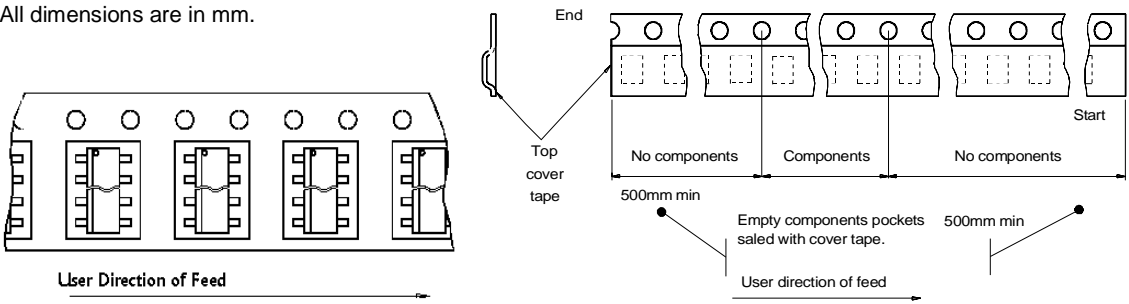
**TAPE DIMENSIONS**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

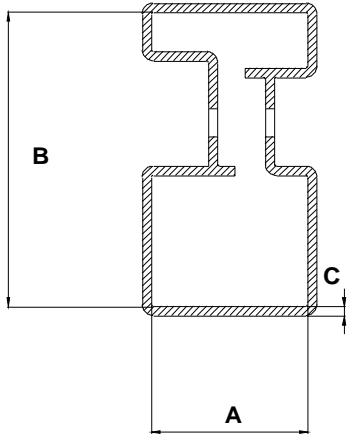
<b>Tape width</b>	<b>W</b>	12
<b>Tape Hole Spacing</b>	<b>P0 (± 0.1)</b>	4
<b>Component Spacing</b>	<b>P</b>	8
<b>Hole Diameter</b>	<b>D (± 0.1/-0)</b>	1.5
<b>Hole Diameter</b>	<b>D1 (min)</b>	1.5
<b>Hole Position</b>	<b>F (± 0.05)</b>	5.5
<b>Compartment Depth</b>	<b>K (max)</b>	4.5
<b>Hole Spacing</b>	<b>P1 (± 0.1)</b>	2



All dimensions are in mm.



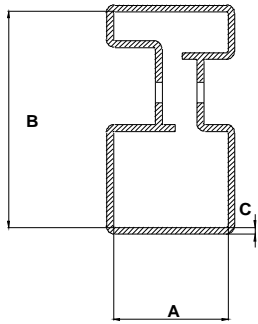
**PENTAWATT TUBE SHIPMENT (no suffix)**



<b>Base Q.ty</b>	50
<b>Bulk Q.ty</b>	1000
<b>Tube length (<math>\pm 0.5</math>)</b>	532
<b>A</b>	18
<b>B</b>	33.1
<b>C (<math>\pm 0.1</math>)</b>	1

All dimensions are in mm.

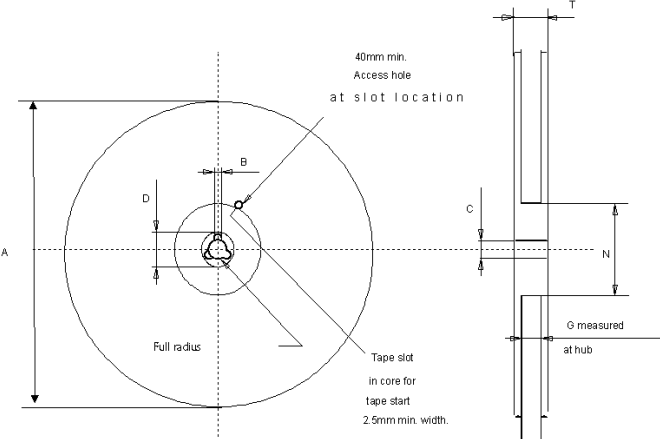
**P<sup>2</sup>PAK TUBE SHIPMENT (no suffix)**



<b>Base Q.ty</b>	50
<b>Bulk Q.ty</b>	1000
<b>Tube length (± 0.5)</b>	532
<b>A</b>	18
<b>B</b>	33.1
<b>C (± 0.1)</b>	1

All dimensions are in mm.

**TAPE AND REEL SHIPMENT (suffix "13TR")**



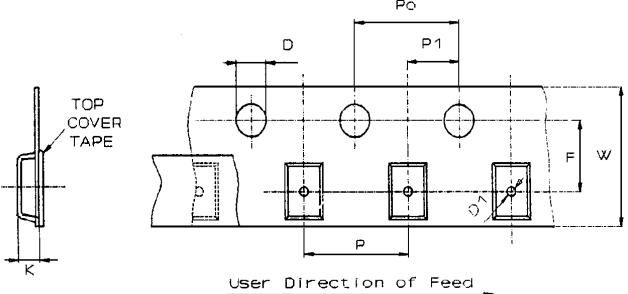
<b>Base Q.ty</b>	1000
<b>Bulk Q.ty</b>	1000
<b>A (max)</b>	330
<b>B (min)</b>	1.5
<b>C (± 0.2)</b>	13
<b>F</b>	20.2
<b>G (+ 2 / -0)</b>	24.4
<b>N (min)</b>	60
<b>T (max)</b>	30.4

All dimensions are in mm.

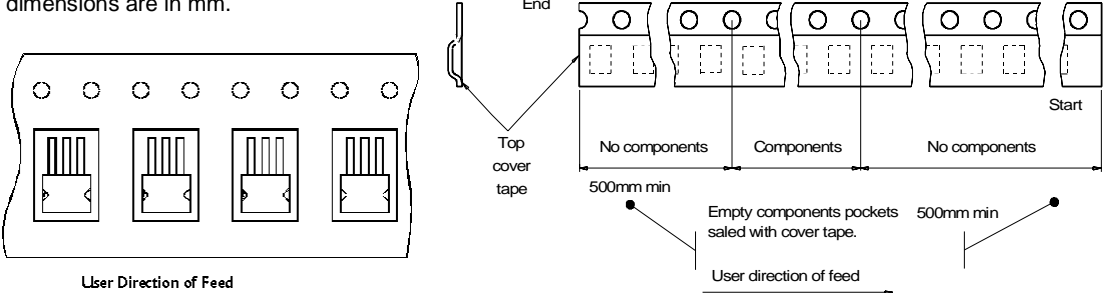
**TAPE DIMENSIONS**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

<b>Tape width</b>	<b>W</b>	24
<b>Tape Hole Spacing</b>	<b>P0 (± 0.1)</b>	4
<b>Component Spacing</b>	<b>P</b>	16
<b>Hole Diameter</b>	<b>D (± 0.1/-0)</b>	1.5
<b>Hole Diameter</b>	<b>D1 (min)</b>	1.5
<b>Hole Position</b>	<b>F (± 0.05)</b>	11.5
<b>Compartment Depth</b>	<b>K (max)</b>	6.5
<b>Hole Spacing</b>	<b>P1 (± 0.1)</b>	2

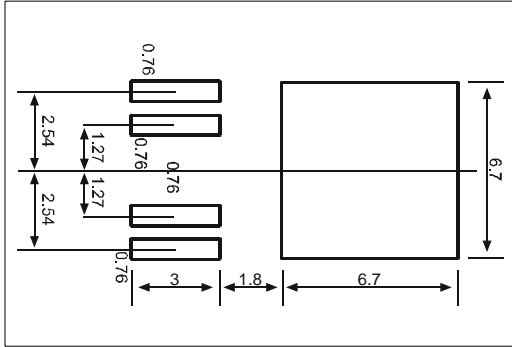


All dimensions are in mm.

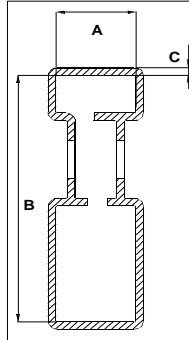


**VN750 / VN750S / VN750PT / VN750-B5**

**PPAK SUGGESTED PAD LAYOUT**



**PPAK TUBE SHIPMENT (no suffix)**



<b>Base Q.ty</b>	75
<b>Bulk Q.ty</b>	3000
<b>Tube length (± 0.5)</b>	532
<b>A</b>	6
<b>B</b>	21.3
<b>C (± 0.1)</b>	0.6

All dimensions are in mm.

**TAPE AND REEL SHIPMENT (suffix "13TR")**

Diagram of a reel showing dimensions A (reel diameter), B (slot width), C (slot depth), D (slot offset), F (slot length), G (measured at hub), N (reel thickness), and T (reel width). Labels include "40mm min. Access hole at slot location" and "Full radius".

**REEL DIMENSIONS**

<b>Base Q.ty</b>	2500
<b>Bulk Q.ty</b>	2500
<b>A (max)</b>	330
<b>B (min)</b>	1.5
<b>C (± 0.2)</b>	13
<b>F</b>	20.2
<b>G (+ 2 / -0)</b>	16.4
<b>N (min)</b>	60
<b>T (max)</b>	22.4

All dimensions are in mm.

**TAPE DIMENSIONS**  
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

<b>Tape width</b>	<b>W</b>	16
<b>Tape Hole Spacing</b>	<b>P0 (± 0.1)</b>	4
<b>Component Spacing</b>	<b>P</b>	8
<b>Hole Diameter</b>	<b>D (± 0.1/-0)</b>	1.5
<b>Hole Diameter</b>	<b>D1 (min)</b>	1.5
<b>Hole Position</b>	<b>F (± 0.05)</b>	7.5
<b>Compartment Depth</b>	<b>K (max)</b>	2.75
<b>Hole Spacing</b>	<b>P1 (± 0.1)</b>	2

All dimensions are in mm.

Diagram of a tape showing dimensions D (hole diameter), P (component spacing), P0 (hole spacing), P1 (hole spacing), F (hole position), W (tape width), and K (compartment depth). Labels include "TOP COVER TAPE" and "User Direction of Feed".

Diagram showing the tape layout with components and empty pockets. Labels include "End", "Start", "Top cover tape", "No components", "Components", "Empty components pockets sealed with cover tape.", and "User direction of feed".

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