



VNP49N04FI VNB49N04 / VNV49N04

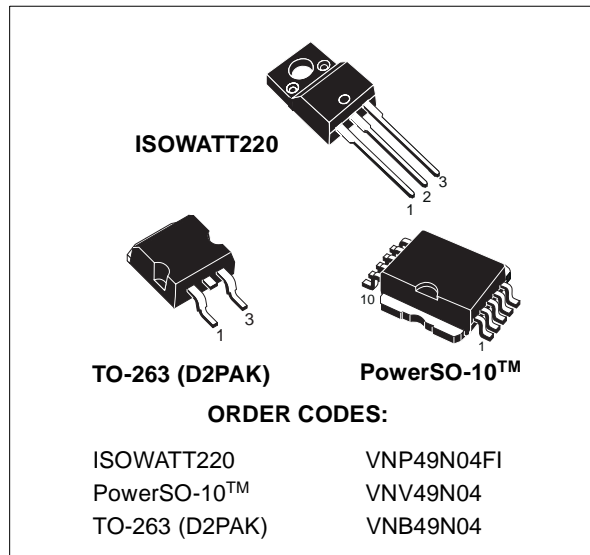
“OMNIFET”: FULLY AUTOPROTECTED POWER MOSFET

TYPE	V _{CLAMP}	R _{DS(ON)}	I _{LIM}
VNP49N04FI VNB49N04 VNV49N04	42 V	20 mΩ	49 A

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

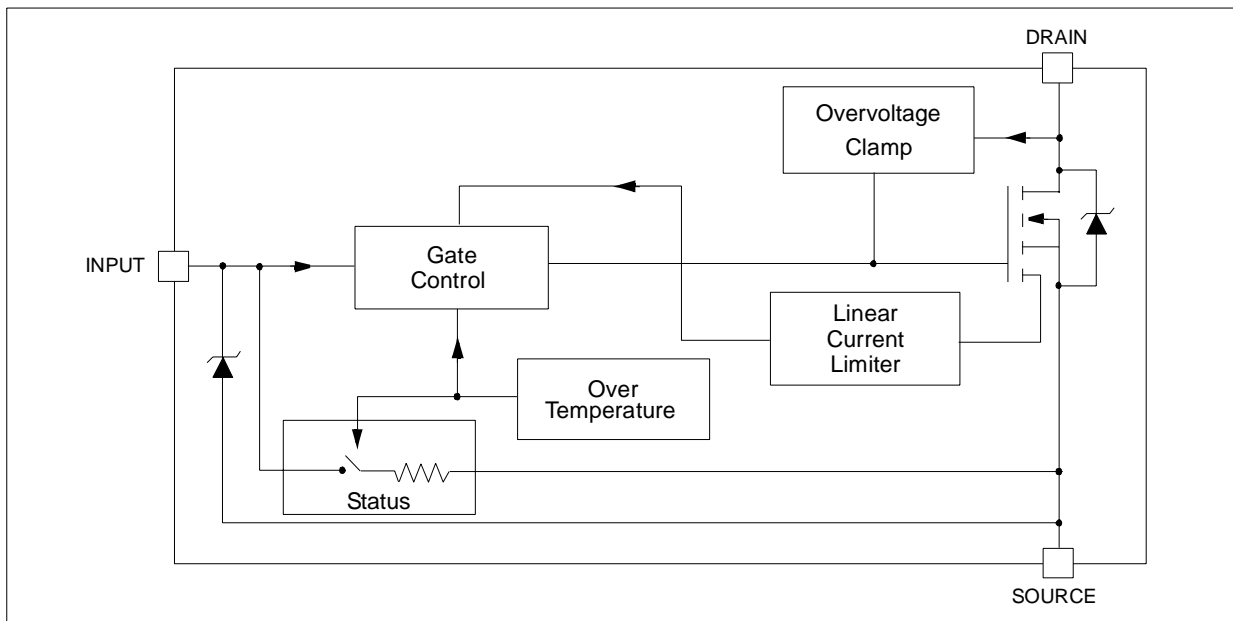
The VNP49N04FI, VNB49N04, VNV49N04 are monolithic devices designed in STMicroelectronics VIPower M0 Technology, intended for replacement of standard Power



MOSFETS from DC up to 50KHz applications. Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

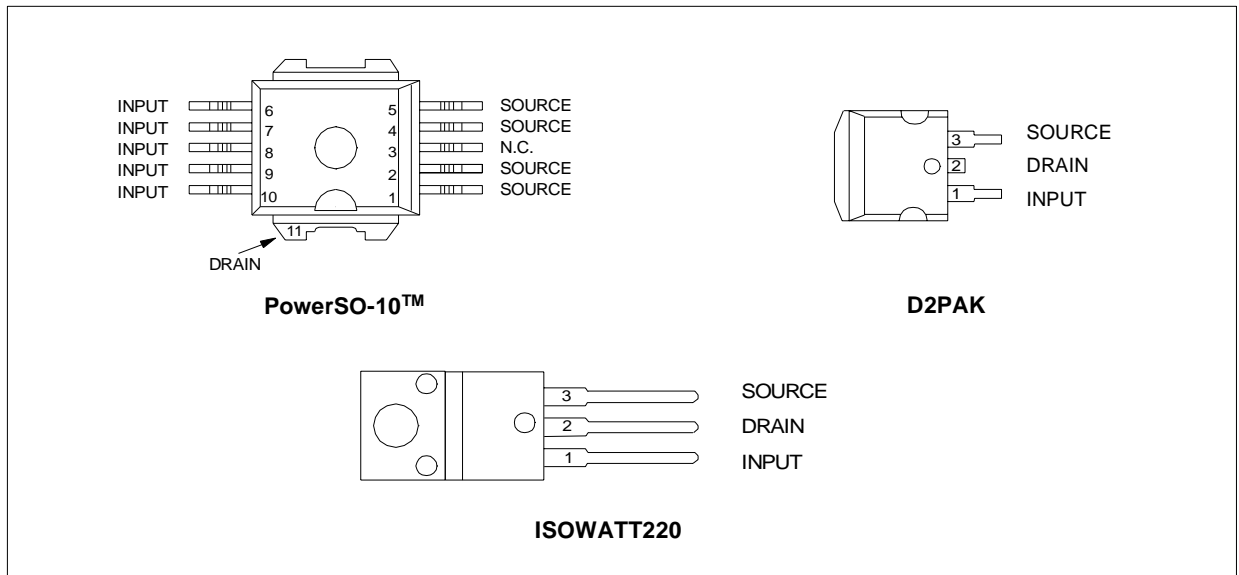
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value			Unit
		PowerSO-10™	D2PAK	ISOWATT220	
V_{DS}	Drain-source Voltage ($V_{IN}=0V$)	Internally Clamped			V
V_{IN}	Input Voltage	18			V
I_D	Drain Current	Internally Limited			A
I_R	Reverse DC Output Current	-50			A
V_{ESD}	Electrostatic Discharge ($R=1.5K\Omega$, $C=100pF$)	2000			V
P_{tot}	Total Dissipation at $T_c=25^\circ C$	125	125	40	W
T_j	Operating Junction Temperature	Internally limited			$^\circ C$
T_c	Case Operating Temperature	Internally limited			$^\circ C$
T_{stg}	Storage Temperature	-55 to 150			$^\circ C$

CONNECTION DIAGRAM (TOP VIEW)



THERMAL DATA

Symbol	Parameter	MAX	Value			Unit
			PowerSO-10	D2PAK	ISOWATT220	
R _{thj-case}	Thermal Resistance Junction-case	MAX	1	1	3.12	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	MAX	50	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (-40°C < T_j < 125°C, unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CLAMP}	Drain-source Clamp Voltage	I _D =200 mA; V _{IN} =0	34	42	50	V
V _{CLTH}	Drain-source Clamp Threshold Voltage	I _D =2mA; V _{IN} =0	33			V
V _{INCL}	Input-Source Reverse Clamp Voltage	I _{IN} = -1mA	-1.2		-0.1	V
I _{DSS}	Zero Input Voltage Drain Current (V _{IN} =0V)	V _{DS} =13V; V _{IN} =0V V _{DS} =25V; V _{IN} =0V			70 220	μA μA
I _{ISS}	Supply Current from Input Pin	V _{DS} =0V; V _{IN} =10V		250	550	μA

ON (*)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{IN(th)}	Input Threshold Voltage	V _{DS} =V _{IN} ; I _D + I _{IN} =1mA	0.8		3	V
R _{DS(on)}	Static Drain-source On Resistance	V _{IN} =10V; I _D =25A V _{IN} =5V; I _D =25A			0.04 0.05	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} =13V; I _D =25A; T _c =25°C	25	30		S
C _{OSS}	Output Capacitance	V _{DS} =13V; f=1MHz; V _{IN} =0V; T _c =25°C		1100	1500	pF

SWITCHING ()**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V; I _D =25A V _{gen} =10V; R _{gen} =10 Ω (see figure 3)		200	600	ns
t _r	Rise Time			1300	3600	ns
t _{d(off)}	Turn-off Delay Time			800	2400	ns
t _f	Fall Time			300	900	ns
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V; I _D =25A V _{gen} =10V; R _{gen} =1000Ω (see figure 3)		1.3	3.8	μs
t _r	Rise Time			3.8	10.4	μs
t _{d(off)}	Turn-off Delay Time			12	24	μs
t _f	Fall Time			6.1	17	μs
(di/dt) _{on}	Turn-on Current Slope	V _{DS} =15V; I _D =25A V _{IN} =10V; R _{gen} =10 Ω		25		A/μs
Q _i	Total Input Charge	V _{DS} =15V; I _D =25A; V _{IN} =10V		100		nC

VNP49N04FI / VNB49N04 / VNV49N04

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{SD}^{(*)}$	Forward On Voltage	$I_{SD}=25A; V_{IN}=0V$			1.8	V
$t_{rr}^{(**)}$	Reverse Recovery Time	$I_{SD}=25A; di/dt=100A/\mu s$		250		ns
$Q_{rr}^{(**)}$	Reverse Recovery Charge	$V_{DS}=30V; T_j=25^{\circ}C$		910		nC
$I_{RRM}^{(**)}$	Reverse Recovery Current	(see test circuit, figure 5)		7.5		A

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LIM}	Drain Current Limit	$V_{IN}=10V; V_{DS}=13V$	28	49	70	A
		$V_{IN}=5V; V_{DS}=13V$	28	49	70	A
$t_{dlim}^{(**)}$	Step Response Current Limit	$V_{IN}=10V$		35	50	μs
		$V_{IN}=5V$		90	150	μs
$T_{jsh}^{(**)}$	Overtemperature Shutdown		150			$^{\circ}C$
$T_{jrs}^{(**)}$	Overtemperature Reset		135			$^{\circ}C$
$I_{gf}^{(**)}$	Fault Sink Current	$V_{IN}=10V; V_{DS}=13V$		50		mA
		$V_{IN}=5V; V_{DS}=13V$		20		mA
$E_{as}^{(**)}$	Single Pulse Avalanche Energy	Starting $T_j=25^{\circ}C; V_{DS}=20V$ $V_{IN}=10V; R_{gen}=1K\Omega; L=6mH$	4			J

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

(**) Parameters guaranteed by design/characterization

PROTECTION FEATURES

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50KHz. The only difference from the user's standpoint is that a small DC current (I_{ISS}) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- OVERVOLTAGE CLAMP PROTECTION:

internally set at 42V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- LINEAR CURRENT LIMITER CIRCUIT:

limits the drain current I_D to I_{LIM} whatever the INPUT pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough,

junction temperature may reach the overtemperature threshold T_{jsh} .

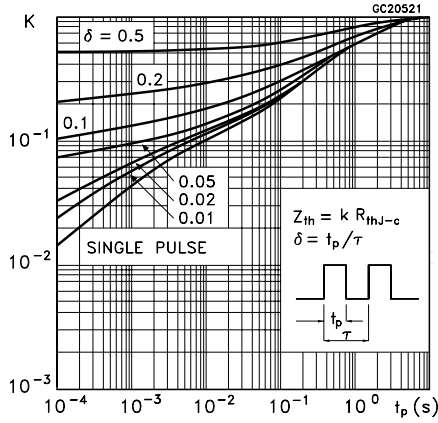
- OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:

these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150°C. The device is automatically restarted when the chip temperature falls below 135°C.

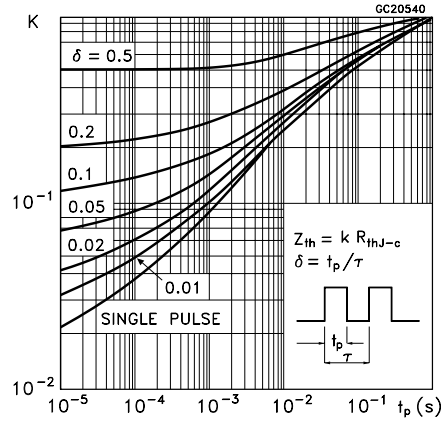
- STATUS FEEDBACK:

in the case of an overtemperature fault condition, a status feedback is provided through the INPUT pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100Ω. The failure can be detected by monitoring the voltage at the INPUT pin, which will be close to ground potential. Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(ON)}$).

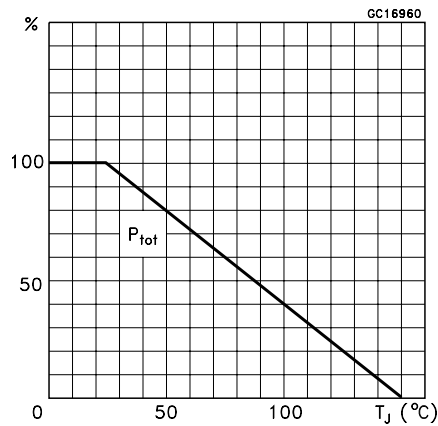
Thermal Impedance for ISOWATT220



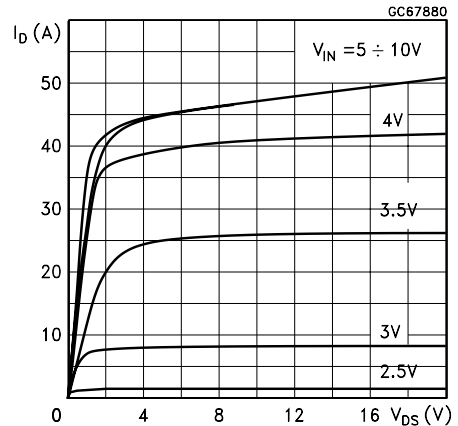
Thermal Impedance for D2PAK / PowerSO-10



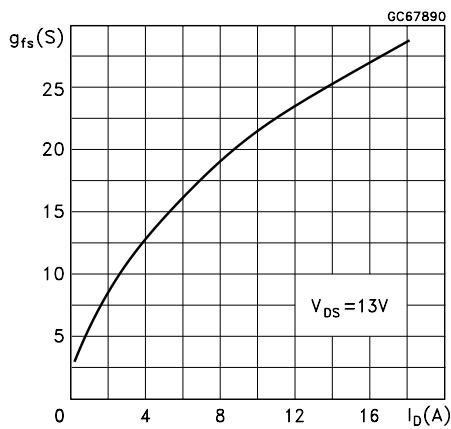
Derating Curve



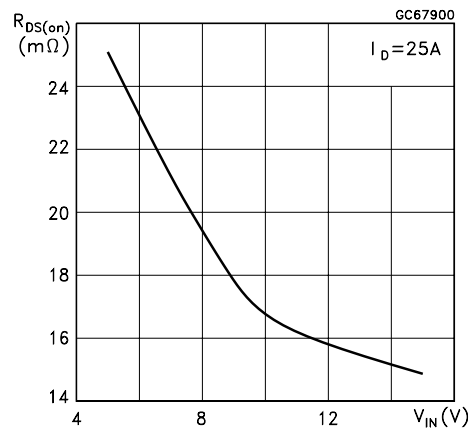
Output Characteristics



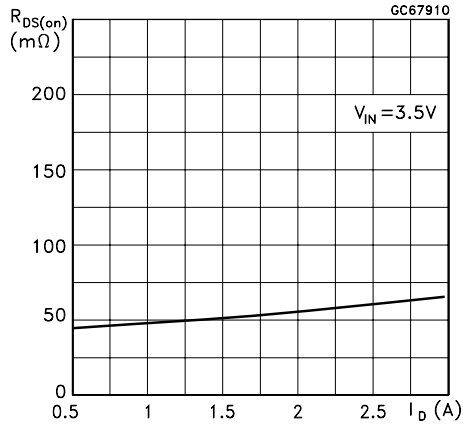
Transconductance



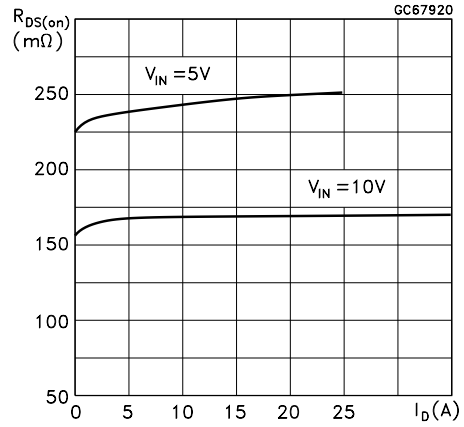
Static Drain-Source On Resistance vs Input Voltage



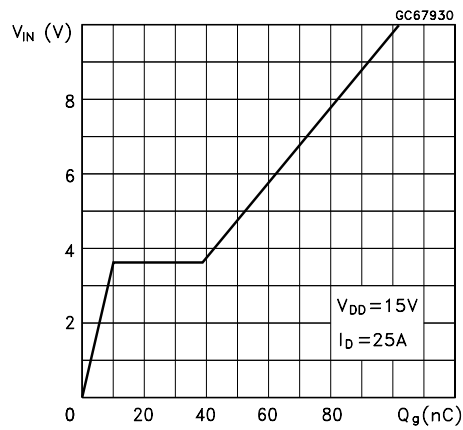
Static Drain-Source On Resistance



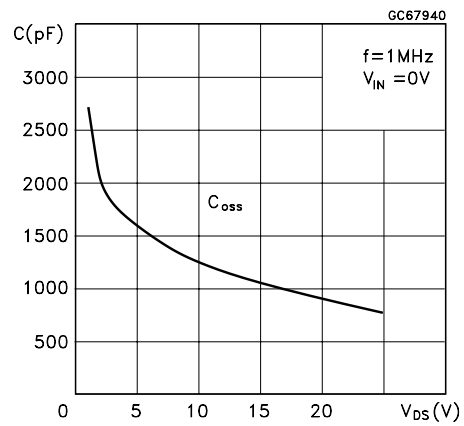
Static Drain-Source On Resistance



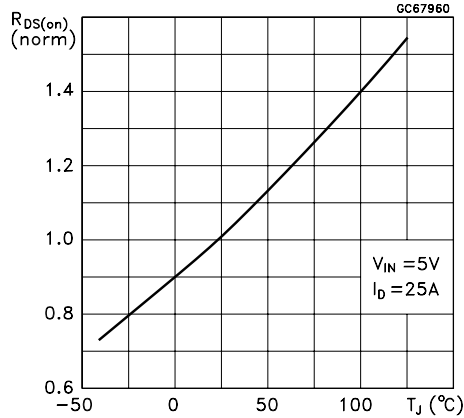
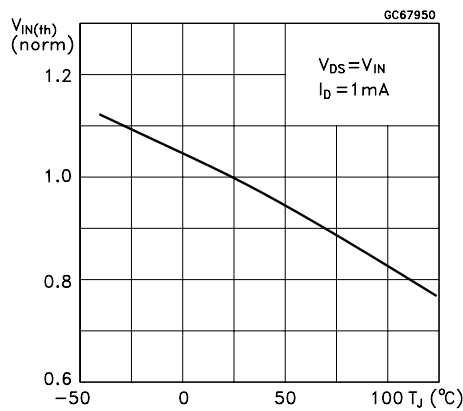
Input Charge vs Input Voltage



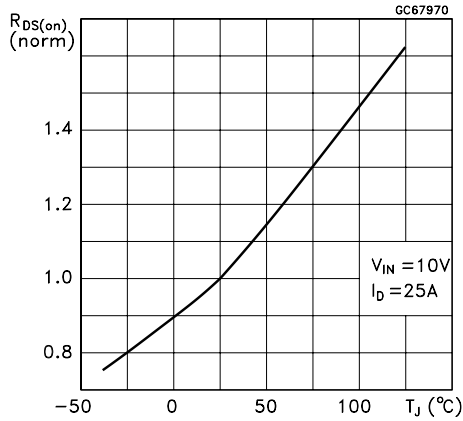
Capacitance Variations



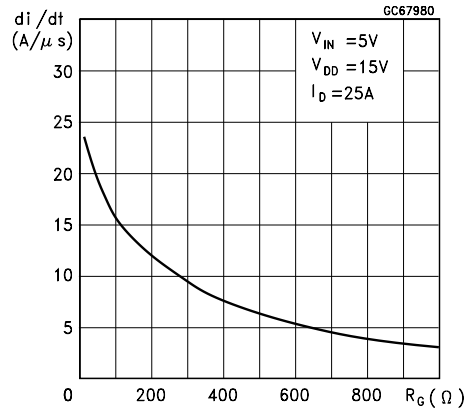
Normalized Input Threshold Voltage vs Normalized On Resistance vs Temperature



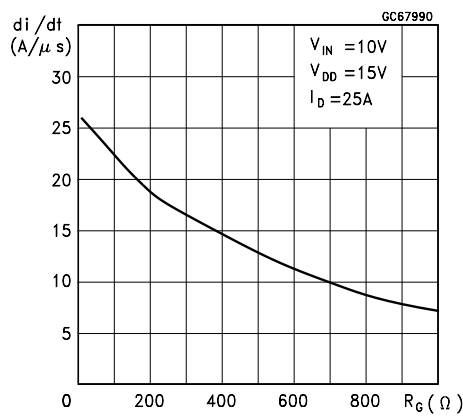
Normalized On Resistance vs Temperature



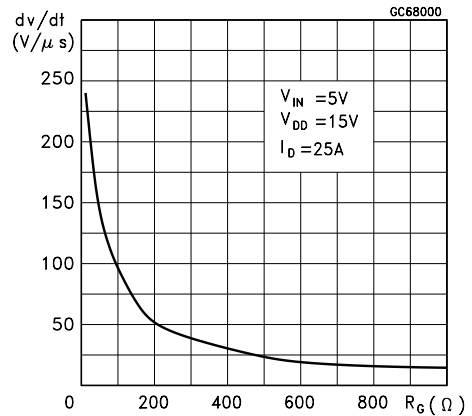
Turn-on Current Slope



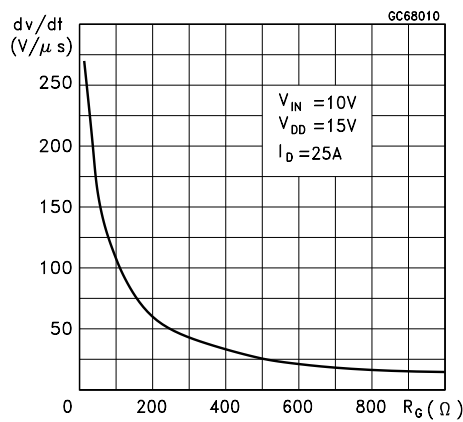
Turn-on Current Slope



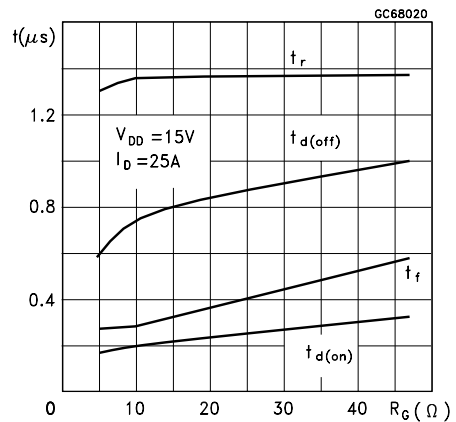
Turn-off Drain-Source Voltage Slope



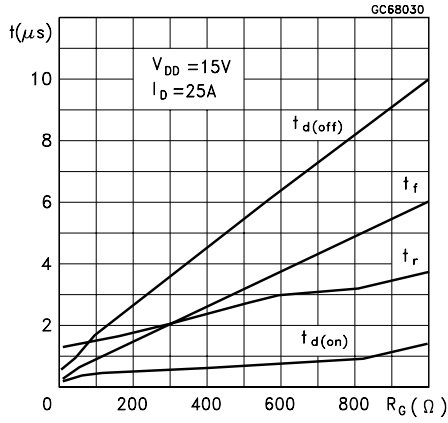
Turn-off Drain-Source Voltage Slope



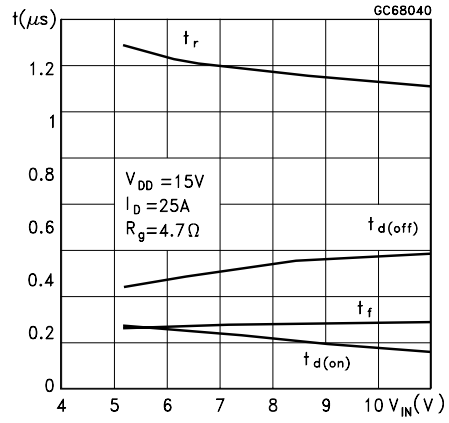
Switching Time Resistive Load



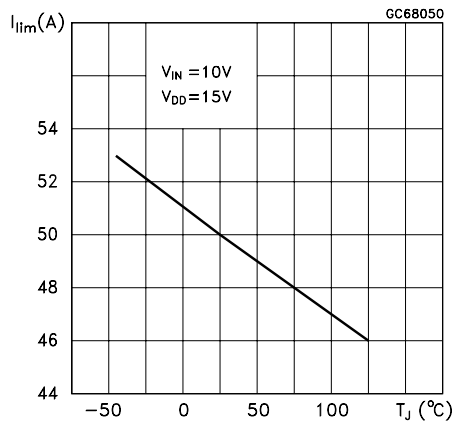
Switching Time Resistive Load



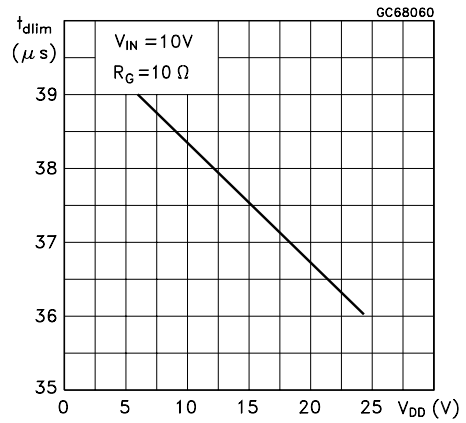
Switching Time Resistive Load



Current Limit vs Junction Temperature



Step Response Current Limit



Source Drain Diode Forward Characteristics

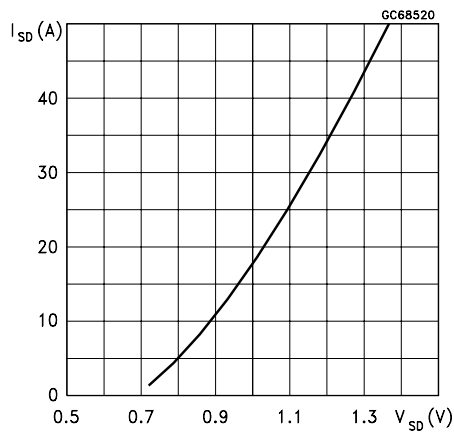


Fig. 1: Unclamped Inductive Load Test Circuits

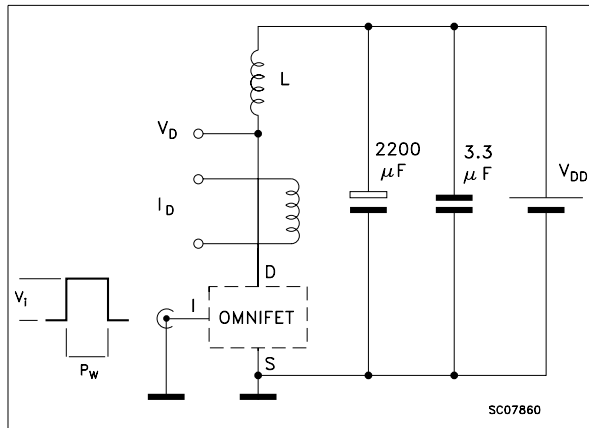


Fig. 2: Unclamped Inductive Waveforms

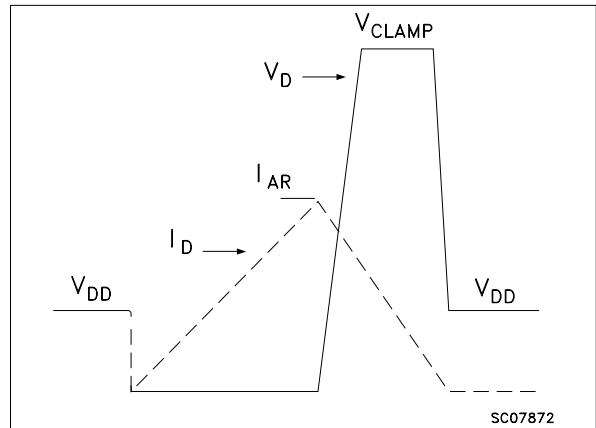


Fig. 3: Switching Time Test Circuits for Resistive Load

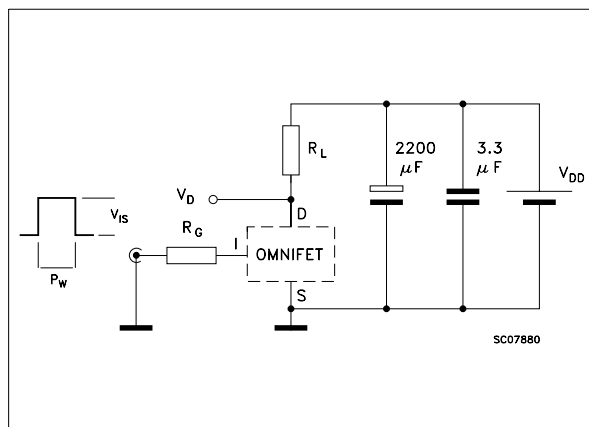


Fig. 4: Input Charge Test Circuit

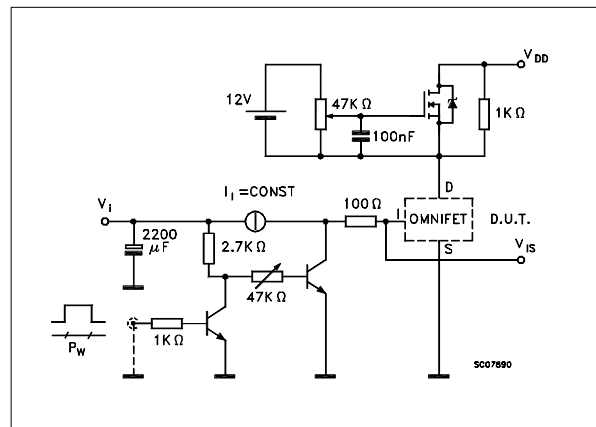


Fig. 5: Test Circuit for Inductive Load Switching and Diode Recovery Times

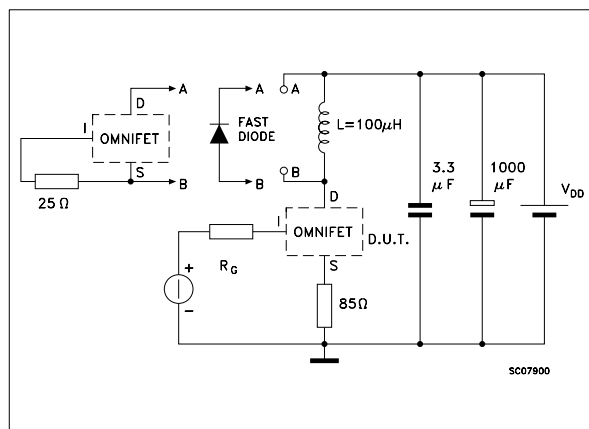
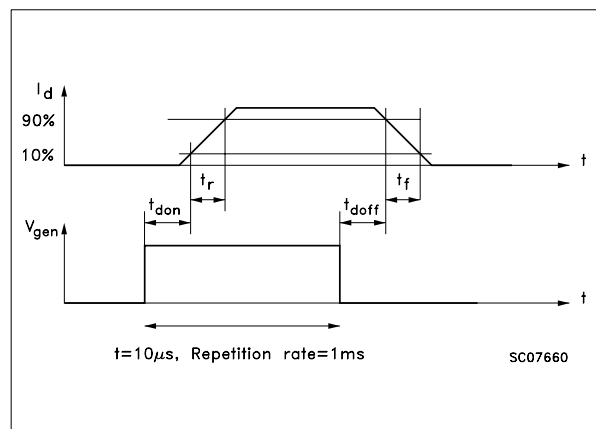
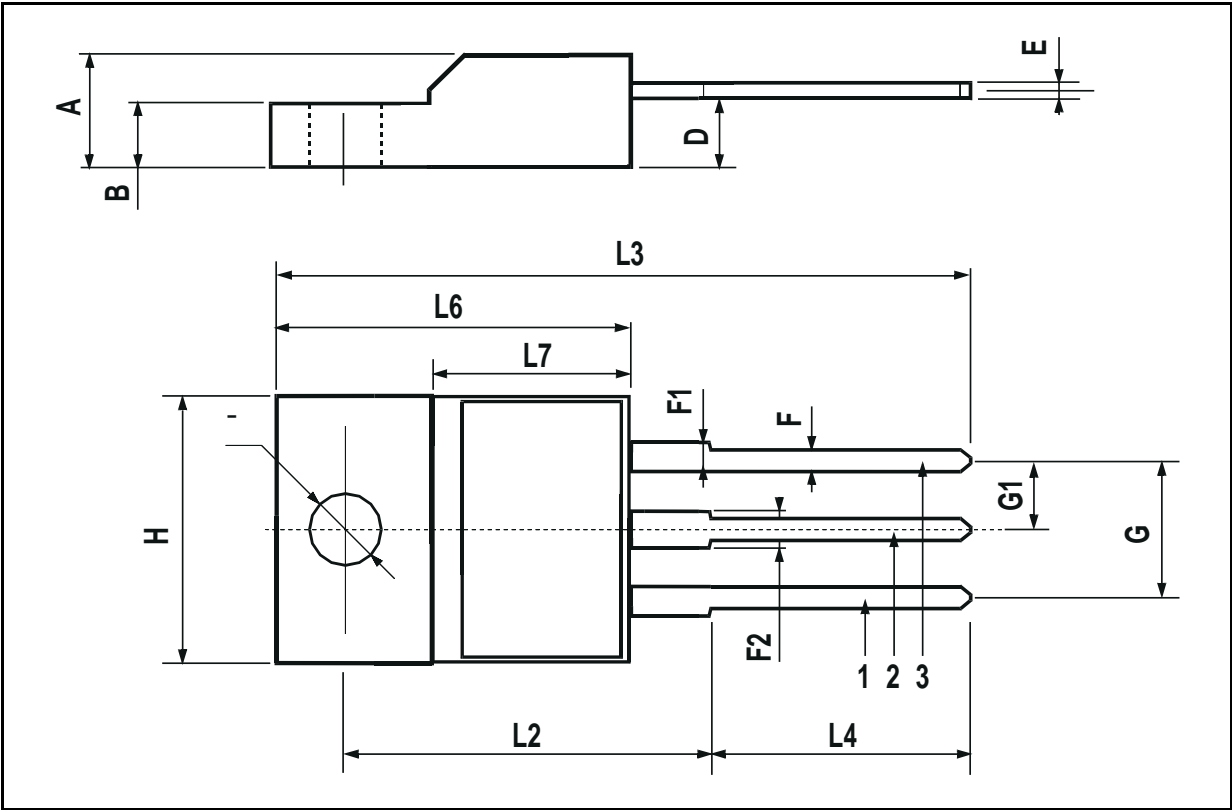


Fig. 6: Waveforms



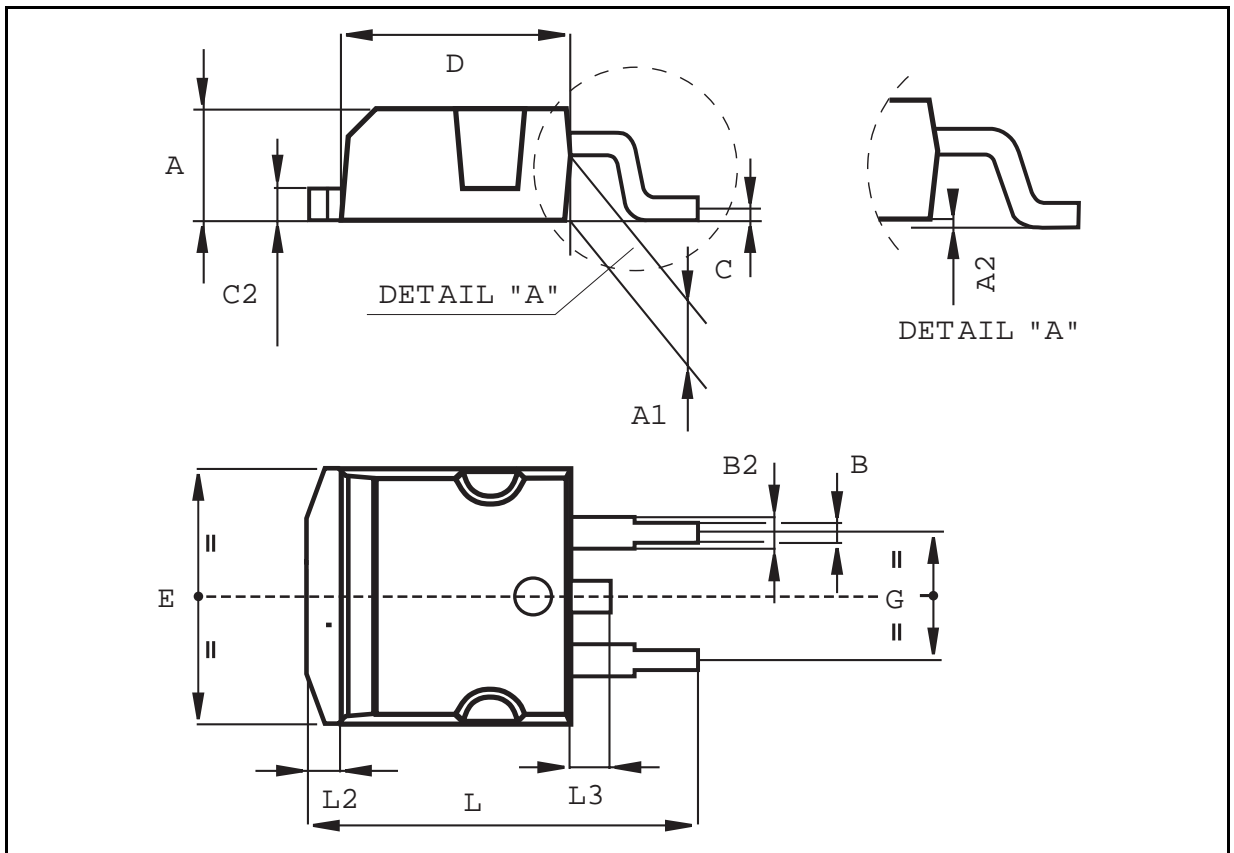
ISOWATT220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
	3		3.2	0.118		0.126



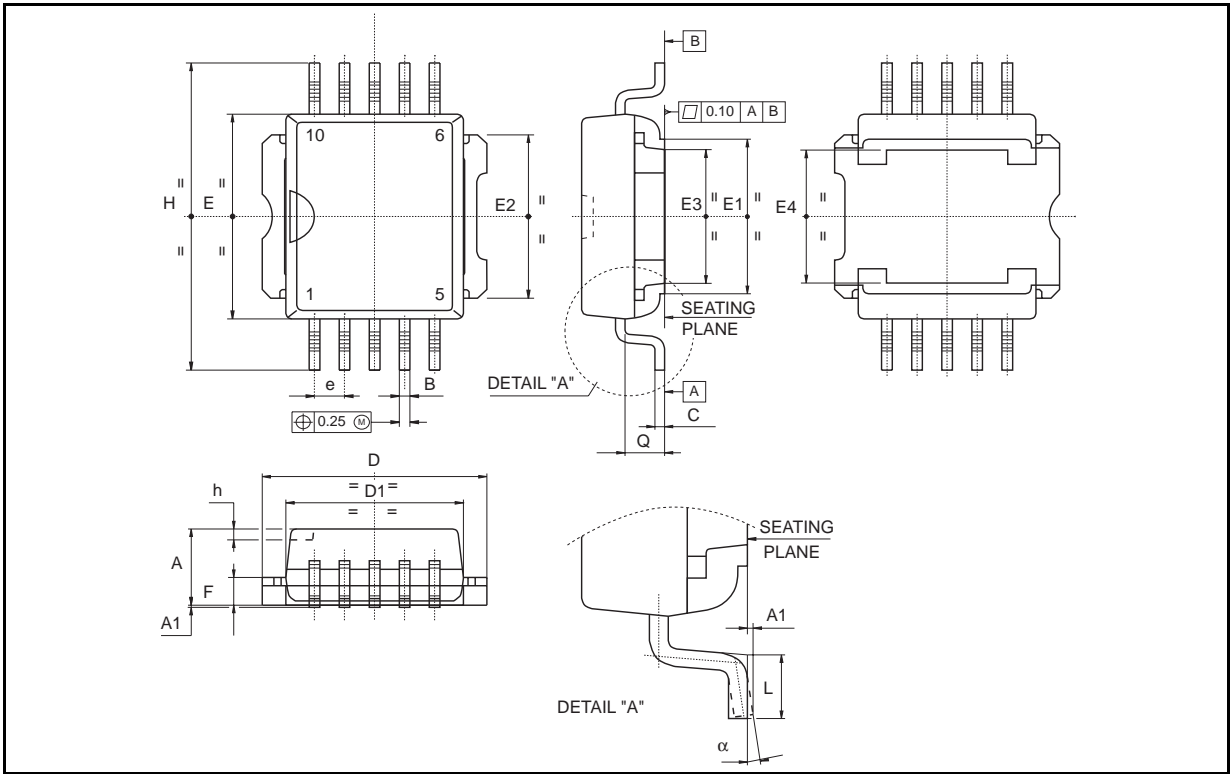
TO-263 (D2PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.30		4.60	0.169		0.181
A1	2.49		2.69	0.098		0.106
B	0.70		0.93	0.027		0.036
B2	1.25		1.4	0.049		0.055
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.28	0.393		0.404
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
Q		1.70			0.067	
α	0°		8°			



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