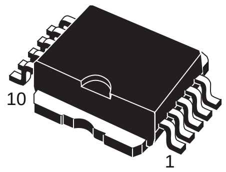
VNQ660SP

QUAD CHANNEL HIGH SIDE SOLID STATE RELAY

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VNQ660SP	50mΩ (*)	6A	36 V

(*) Per each channel



PowerSO-10™

ORDER CODES		
PACKAGE	**TUBE**	**T&R**
PowerSO-10™	VNQ660SP	VNQ660SP13TR

- OUTPUT CURRENT PER CHANNEL: 6A
- CMOS COMPATIBLE INPUTS
- OPEN LOAD DETECTION (OFF STATE)
- UNDERVOLTAGE & OVERVOLTAGE SHUT- DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST: LOSS OF GROUND & LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (**)

DESCRIPTION

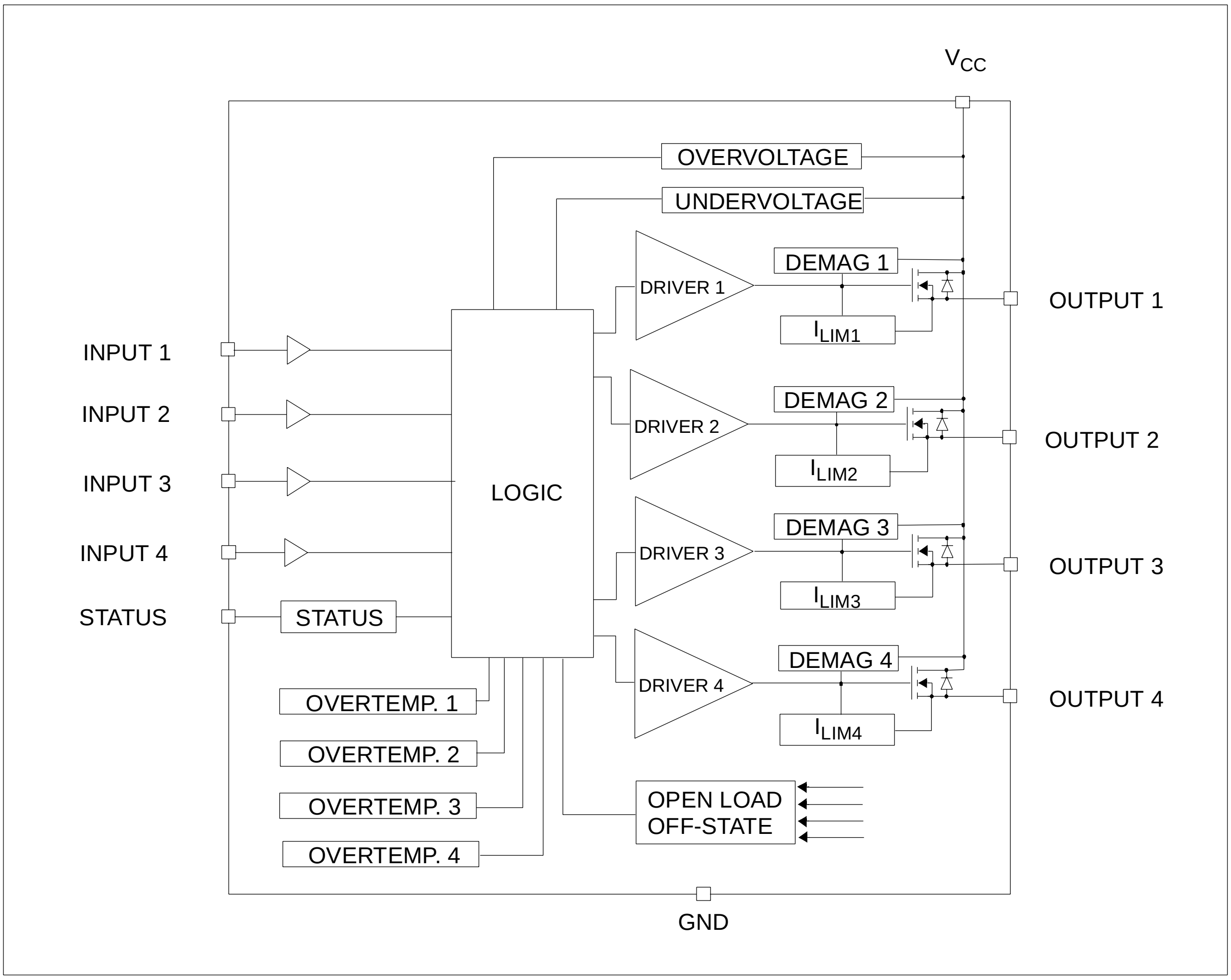
The VNQ660SP is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving resistive or inductive loads with one side connected to ground. This device has four independent channels. Built-in thermal shut down and output current limitation protect the chip from over temperature and short circuit.

ABSOLUTE MAXIMUM RATING

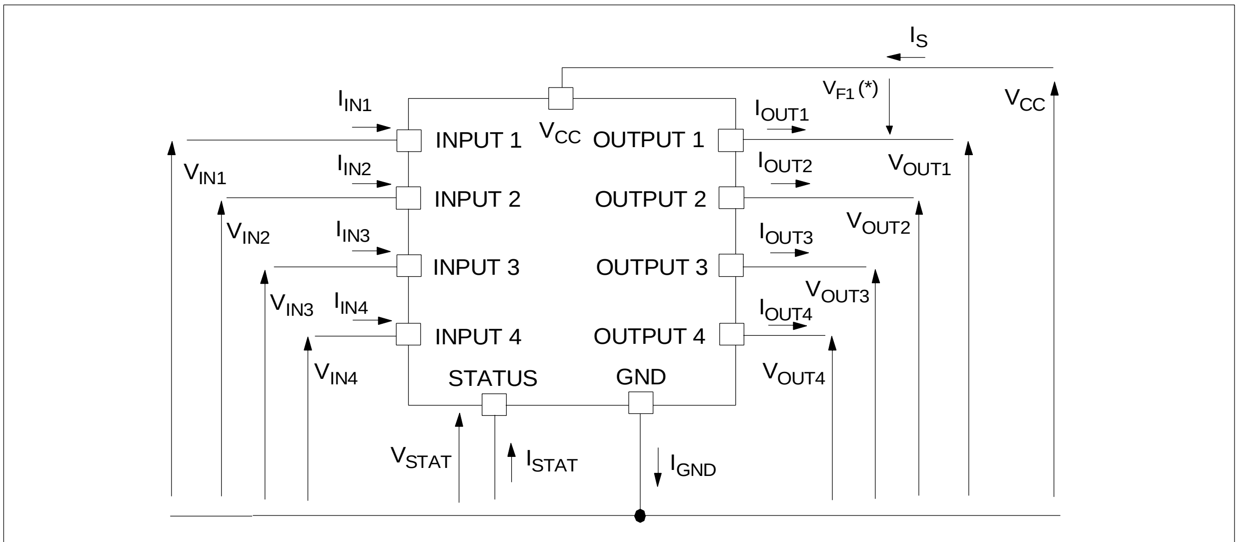
Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (continuous)	41	V
$-V_{CC}$	Reverse supply voltage (continuous)	-0.3	V
I_{OUT}	Output current (continuous), per each channel	Internally limited	A
I_R	Reverse output current (continuous), per each channel	-15	A
I_{IN}	Input current	+/- 10	mA
I_{STAT}	Status current	+/- 10	mA
I_{GND}	Ground current at $T_C \leq 25°C$ (continuous)	-200	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000	 V V V V
E_{MAX}	Maximum Switching Energy (L=1.46mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_L=10A)	101	mJ
P_{tot}	Power dissipation at T_C=25°C	113.6	W
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-65 to 150	°C
E_C	Non repetitive clamping energy at T_C=25°C	150	mJ

(**) See application schematic at page 8

BLOCK DIAGRAM

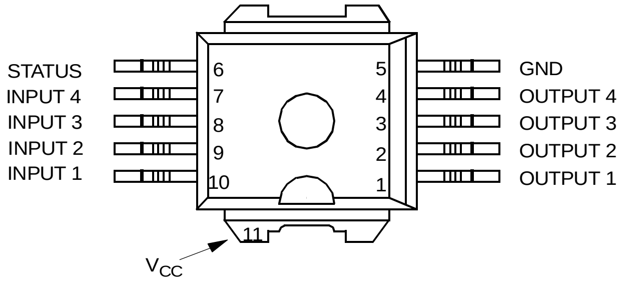


CURRENT AND VOLTAGE CONVENTIONS



(*) $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition

CONFIGURATION DIAGRAM (TOP VIEW) & SUGGESTED CONNECTIONS FOR UNUSED AND N.C. PINS



Connection / Pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To Ground		X		Through 10KΩ resistor

THERMAL DATA

Symbol	Parameter	Value		Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX) (all channels on)	1.1 (1)	52 (2)	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (MAX)	51.1 (1)	33 (2)	°C/W

(1) When mounted on a standard single-sided FR-4 board with 1cm² of Cu (at least 35 µm thick). Horizontal mounting and no artificial air flow.
(2) When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35 µm thick). Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (V_{CC}=6V up to 24V; -40°C<T_j<150°C unless otherwise specified)

POWER (per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC} (**)	Operating supply voltage		6	13	36	V
V_{USD} (**)	Undervoltage shutdown		3.5	4.6	6	V
V_{UVhyst} (**)	Undervoltage hysteresis		0.2		1	V
V_{OV} (**)	Overvoltage shutdown		36			V
V_{OVhyst} (**)	Overvoltage hysteresis		0.25			V
I_S (**)	Supply current	Off state; Input=0V; V_{CC}=13.5V Off state; Input=0V; V_{CC}=13.5V T_j=25°C On state Input=3.25V; 9V<V_{CC}<18V		12 12 6	40 25 12	µA µA mA
$R_{DS(on)}$	On state resistance	I_{OUT}=1A; T_j=25°C; 9V<V_{CC}<18V I_{OUT}=1A, T_j=150°C; 9V<V_{CC}<18V I_{OUT}=1A; V_{CC}=6V		40 85	50 100 130	mΩ mΩ mΩ
$I_{L(off1)}$	Off state output current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =25°C			3	µA

(**) Per device.

VCC - OUTPUT DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward on Voltage	-I_{OUT}=1.6A; T_j=150°C			0.6	V

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	R_L=13Ω channels 1,2,3,4		40	70	µs
$t_{d(off)}$	Turn-on delay time	R_L=13Ω channels 1,2,3,4		40	140	µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L=13Ω channels 1,2,3,4		See relative diagram		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L=13Ω channels 1,2,3,4		See relative diagram		V/µs

PROTECTIONS (per each channel) (see note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shutdown temperature		150	170	200	°C
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15	25	°C
I_{lim}	DC Short circuit current	9V<V_{CC}<36V 6V<V_{CC}<36V	6	10	18 18	A A
V_{demag}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0V; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{STAT}	Status low output voltage	I_{STAT}=1.6mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT}=5V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT}=5V			25	pF
V_{SCL}	Status clamp voltage	I_{STAT}=1mA I_{STAT}=-1mA	6	6.8 -0.7	8	V V

Note 1: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

LOGIC INPUT (per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage				1.25	V
V_{IH}	Input High Level Voltage		3.25			V
V_{HYST}	Input Hysteresis Voltage		0.5			V
I_{IH}	Input high level voltage	V_{IN}=3.25V			10	µA
I_{IL}	Input Current	V_{IN}=1.25V	1			µA
C_{IN}	Input Capacitance				40	pF
V_{ICL}	Input Clamp Voltage	I_{IN}=1mA I_{IN}=-1mA	6	6.8 -0.7	8	V V

OPENLOAD DETECTION (off state) per each channel

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{SDL}	Status Delay	(*)			20	µs
V_{OL}	Openload Voltage Detection Threshold	V_{IN}=0V	1.5	2.5	3.5	V
T_{DOL}	Openload Detection Delay at Turn Off	V_{CC}=18V (*)			300	µs

(*) See Figure 1

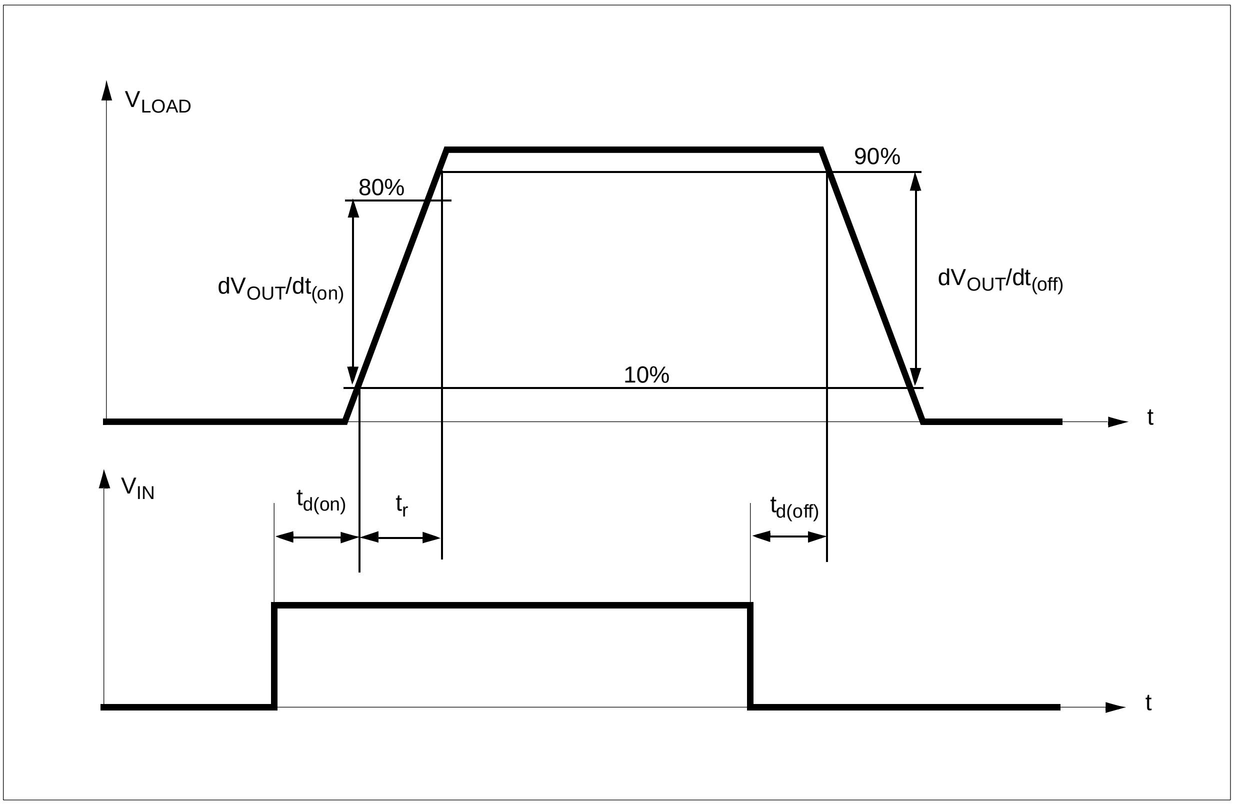
ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω

ISO T/R 7637/1 Test Pulse	Test Levels Result			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

SWITCHING CHARACTERISTICS



TRUTH TABLE (per each channel)

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > V_{OL}	L H	H H	L H
Output Current < I_{OL}	L H	L H	H L

Figure 1: Status timing waveforms

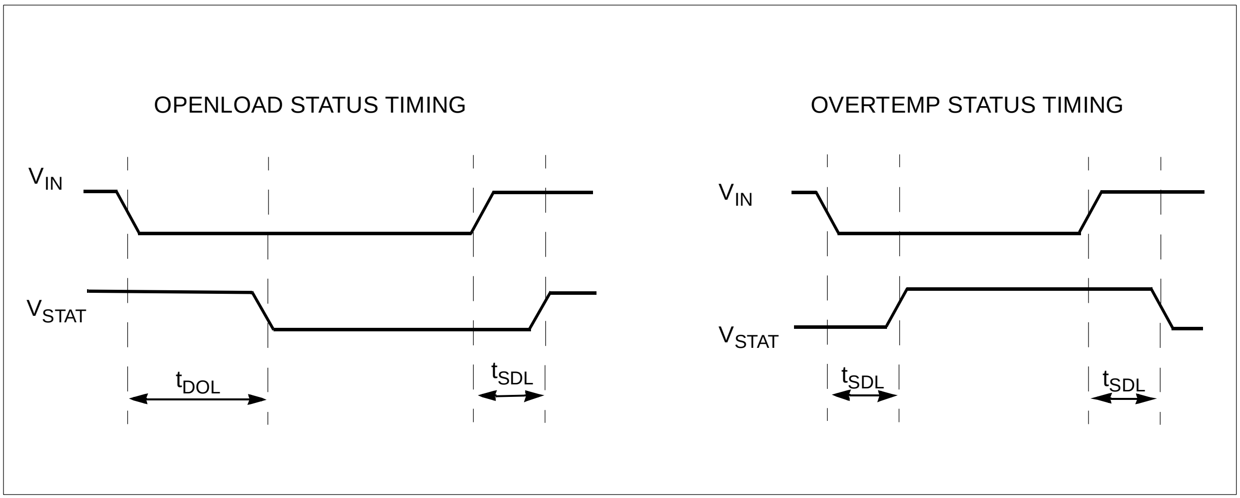
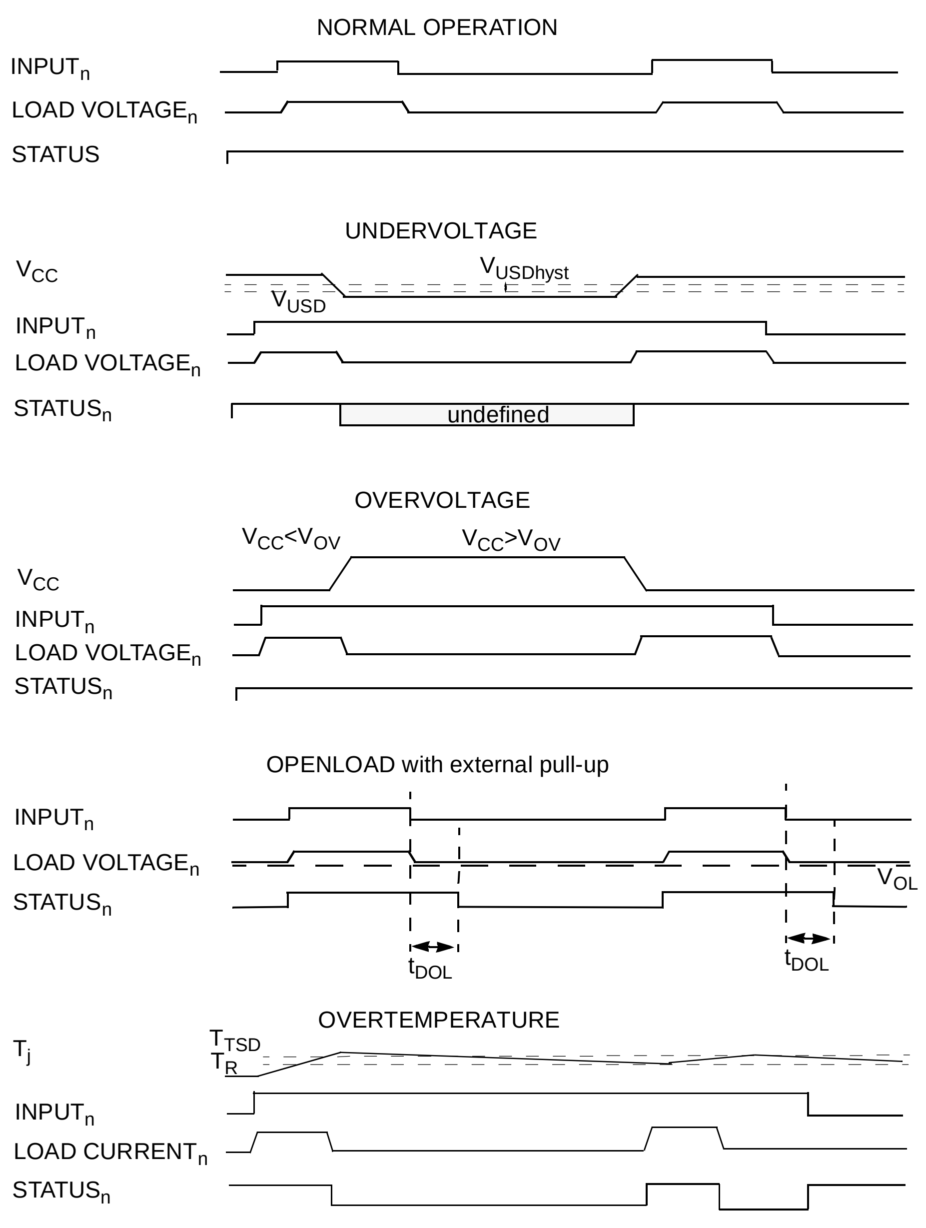
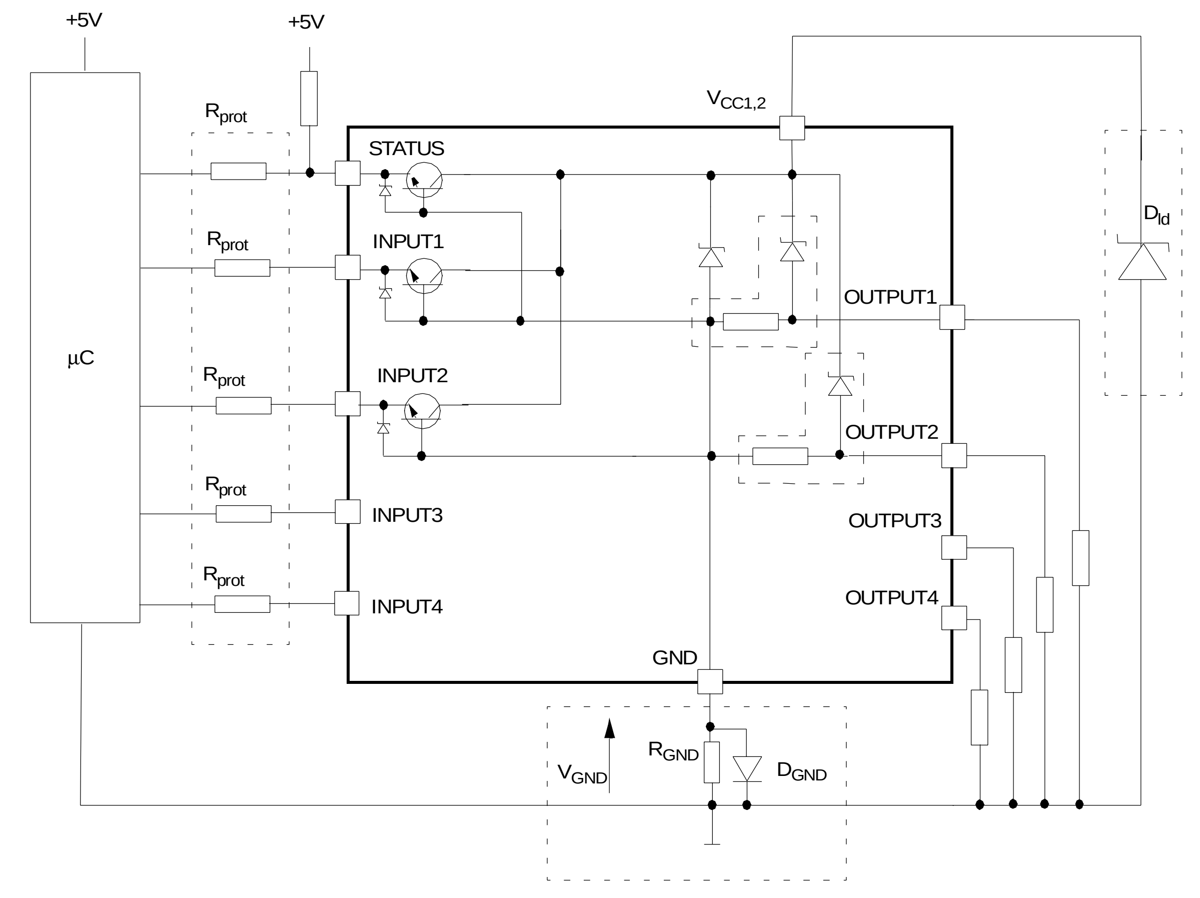


Figure 2: Waveforms



APPLICATION SCHEMATIC



Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≃600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

μC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

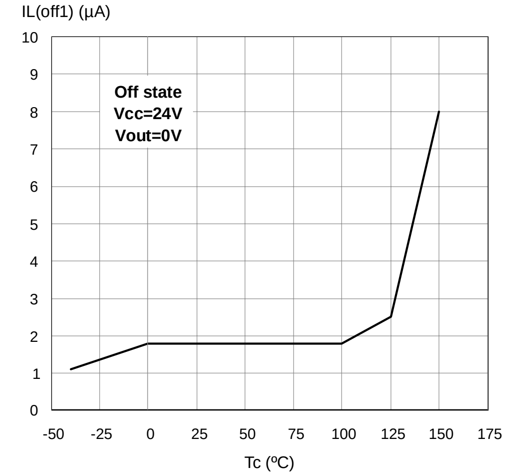
Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

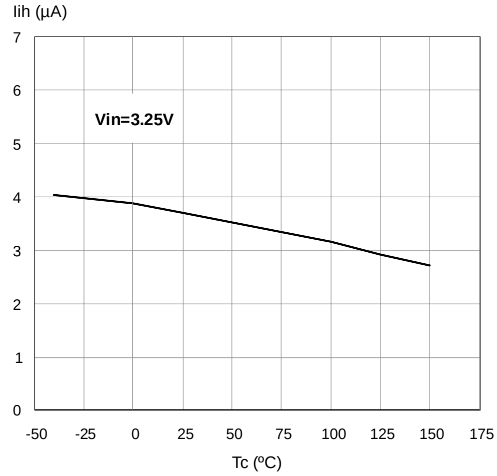
$5k\Omega \leq R_{prot} \leq 65k\Omega$.

Recommended R_{prot} value is 10kΩ.

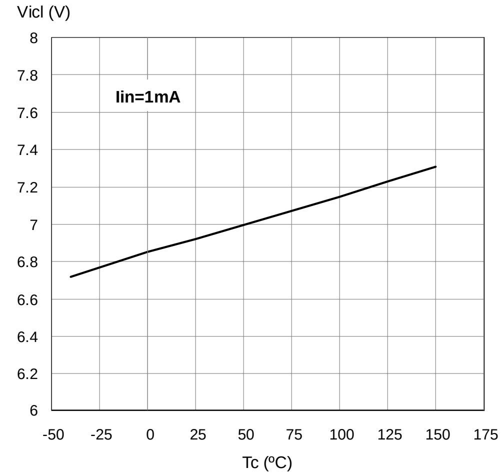
Off State Output Current



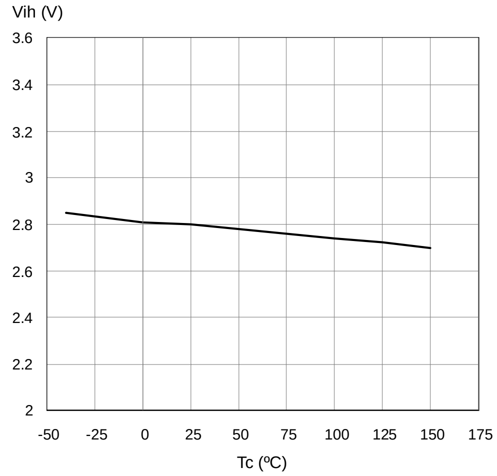
High Level Input Current



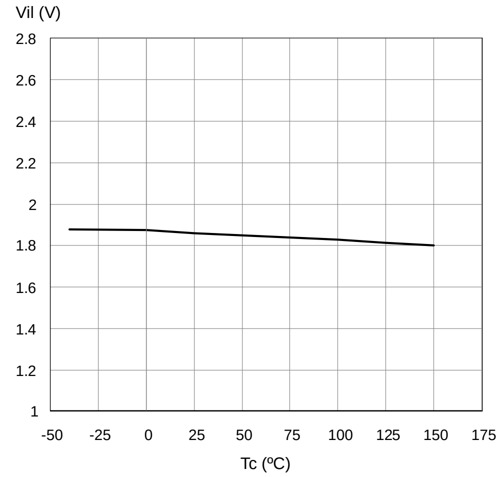
Input Clamp Voltage



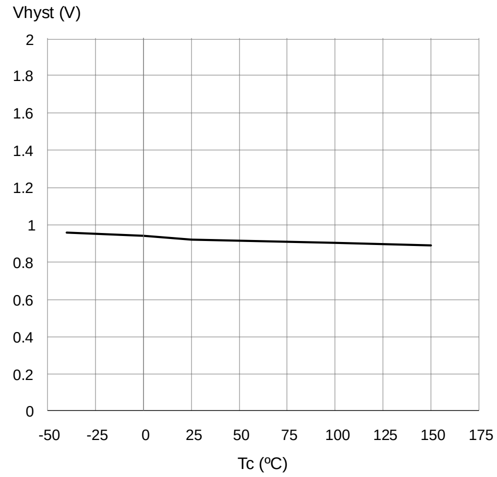
Input High Level



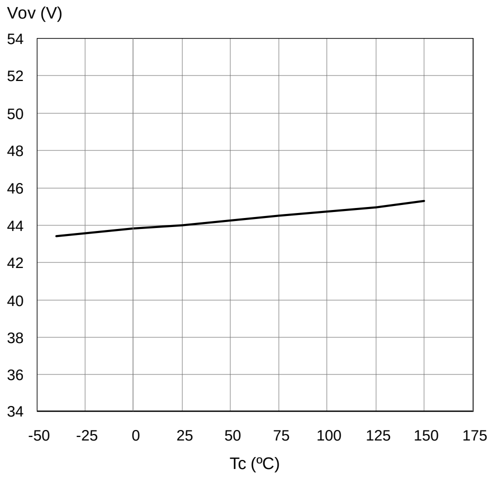
Input Low Level



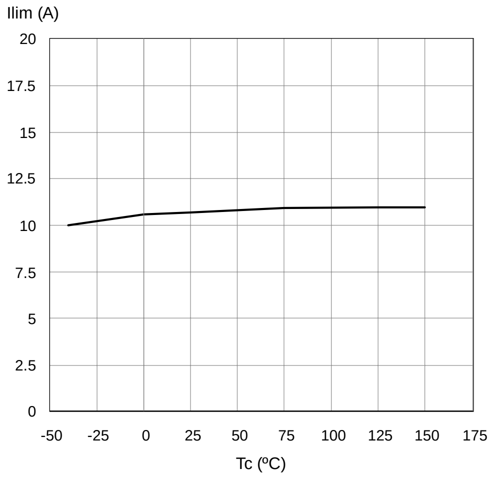
Input Hysteresis Voltage



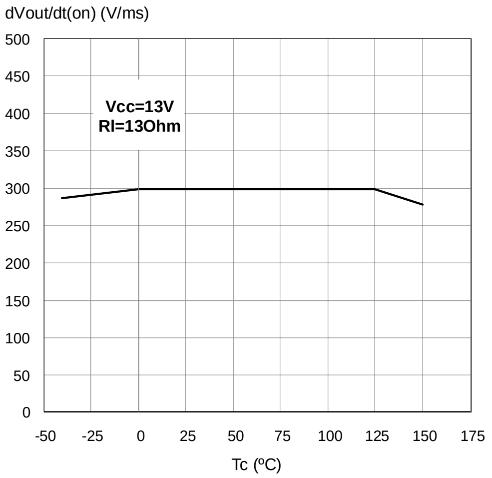
Overvoltage Shutdown



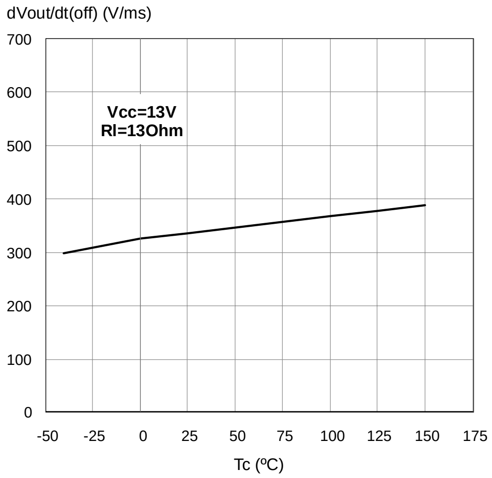
I_{LIM} Vs T_{case}



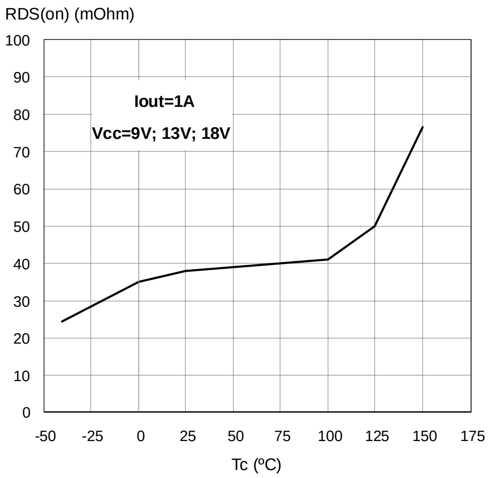
Turn-on Voltage Slope



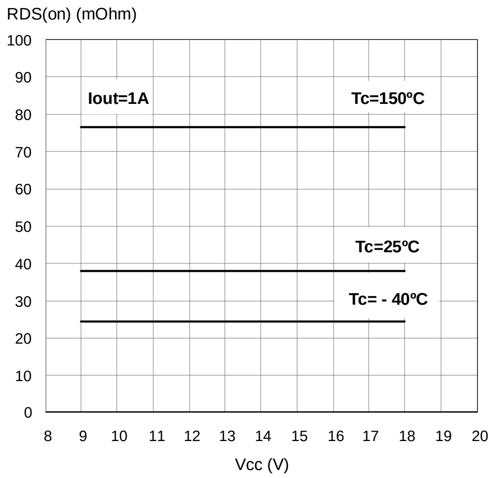
Turn-off Voltage Slope



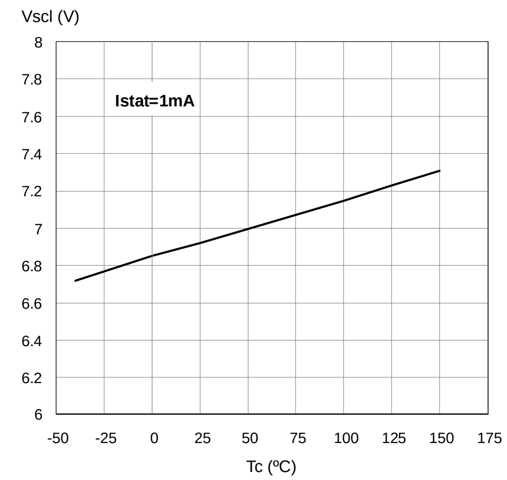
On State Resistance Vs T_{case}



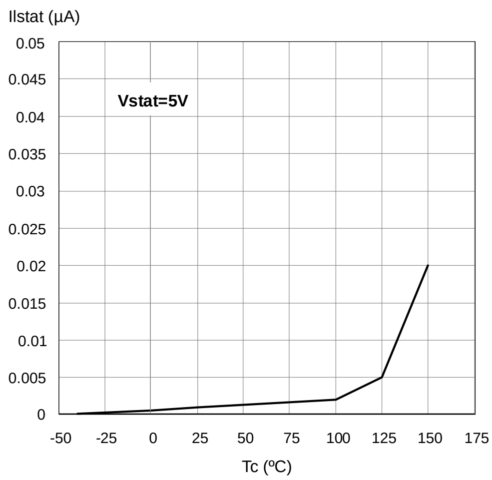
On State Resistance Vs V_{CC}



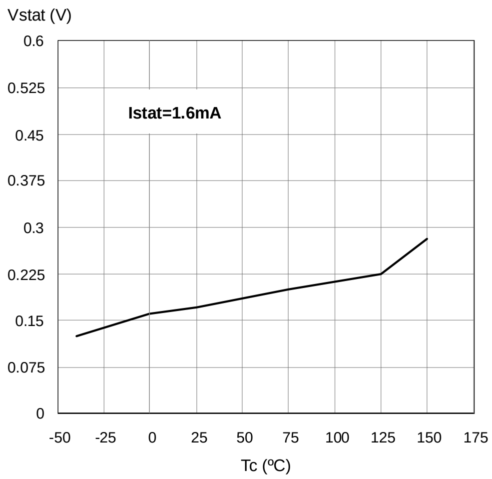
Status Clamp Voltage



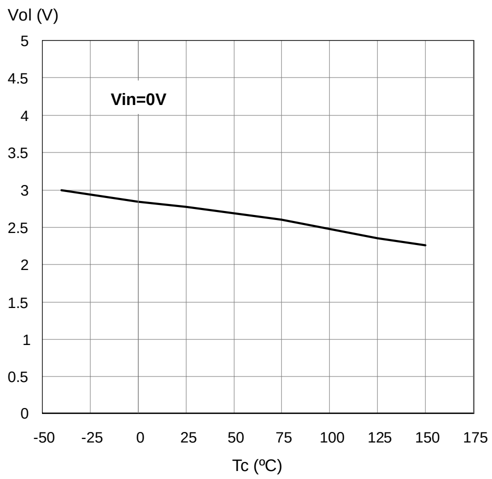
Status Leakage Current



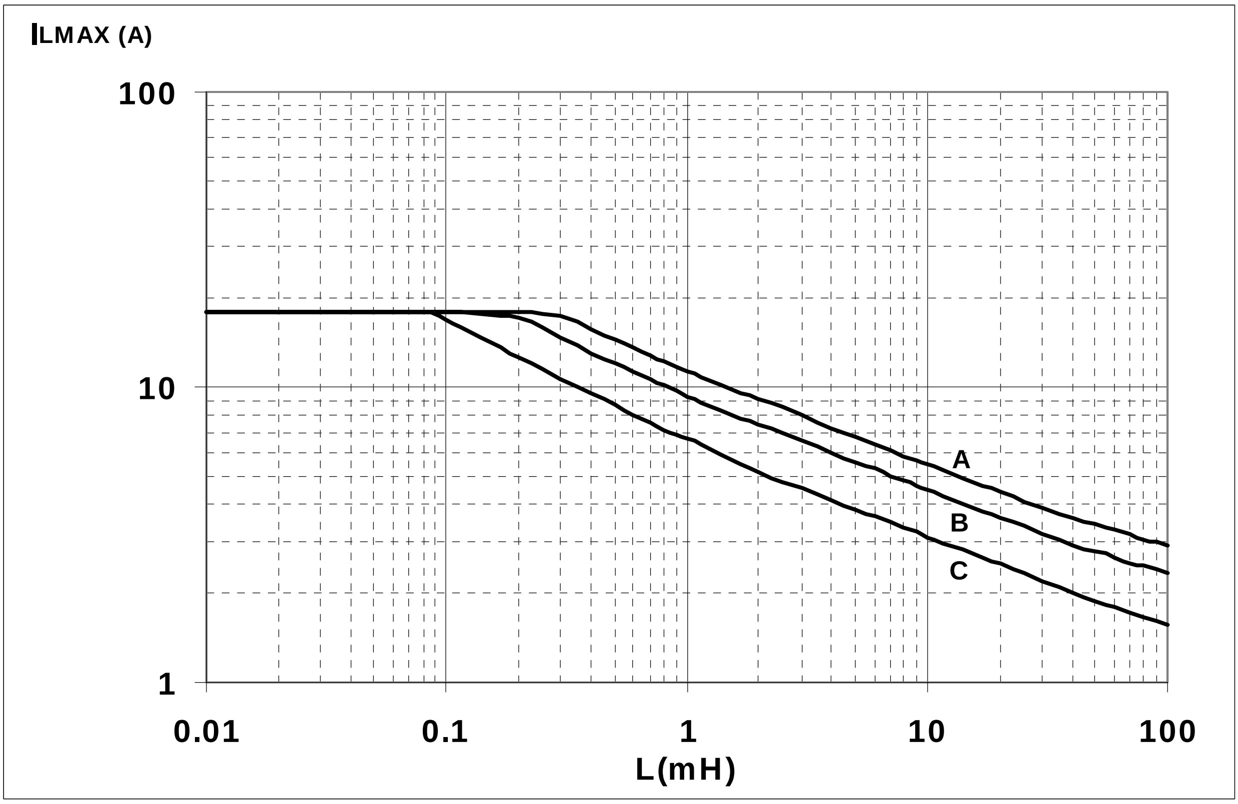
Status Low Output Voltage



Open Load Off State Voltage Detection Threshold



PowerSO-10 Maximum turn off current versus load inductance



A = Single Pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

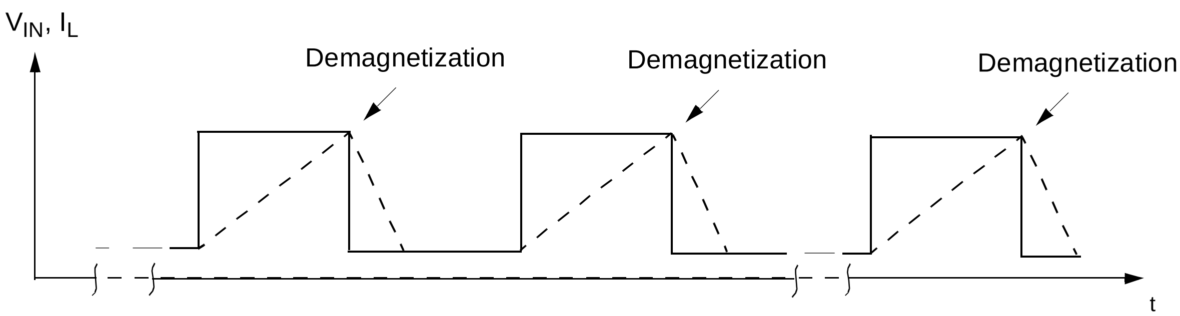
C= Repetitive Pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5V

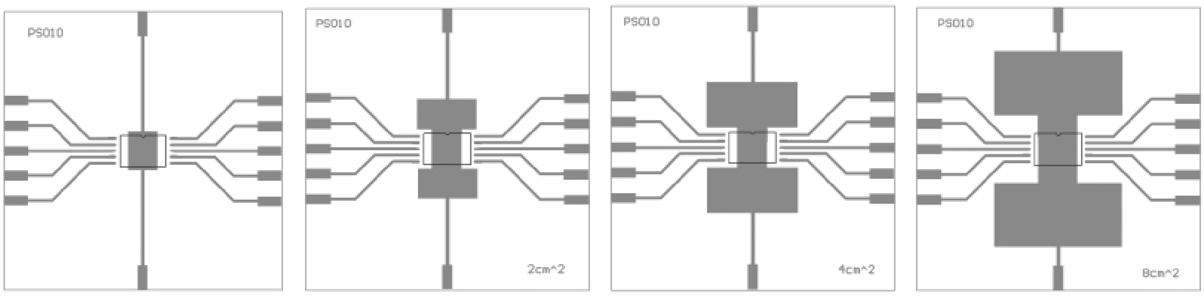
Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



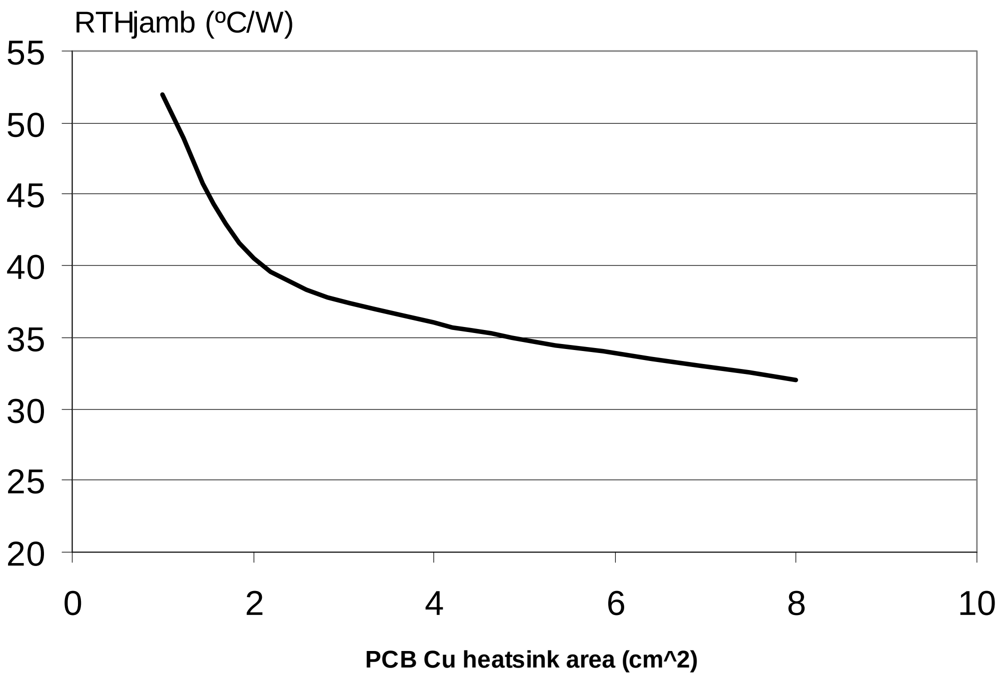
PowerSO-10™ THERMAL DATA

PowerSO-10™ PC Board

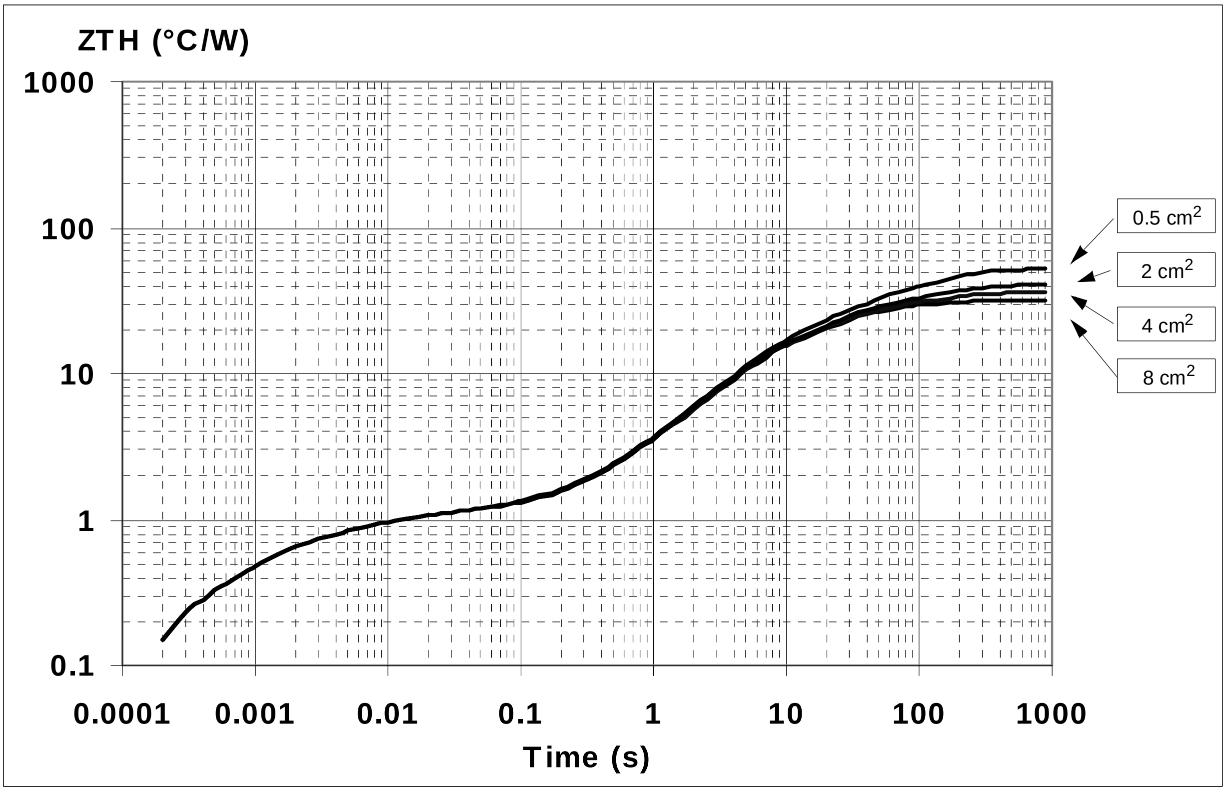


Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: from minimum pad lay-out to $8cm^2$).

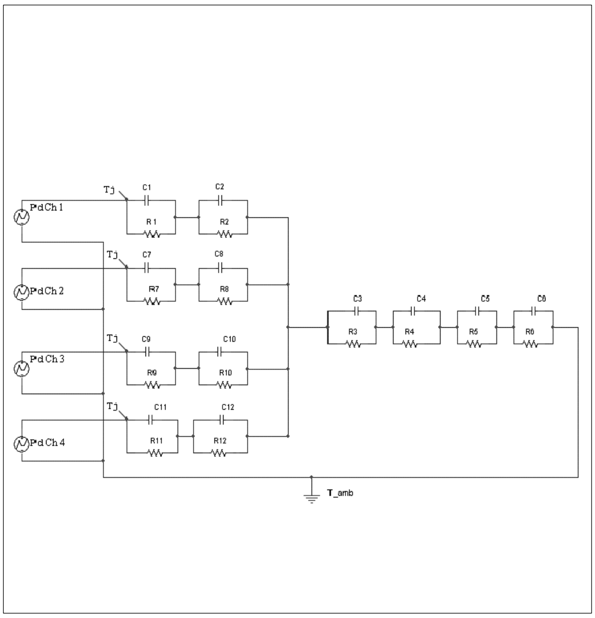
$R_{thj-amb}$ Vs. PCB copper area in open box free air condition



PowerSO-10 Thermal Impedance Junction Ambient Single Pulse



Thermal fitting model of a single channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

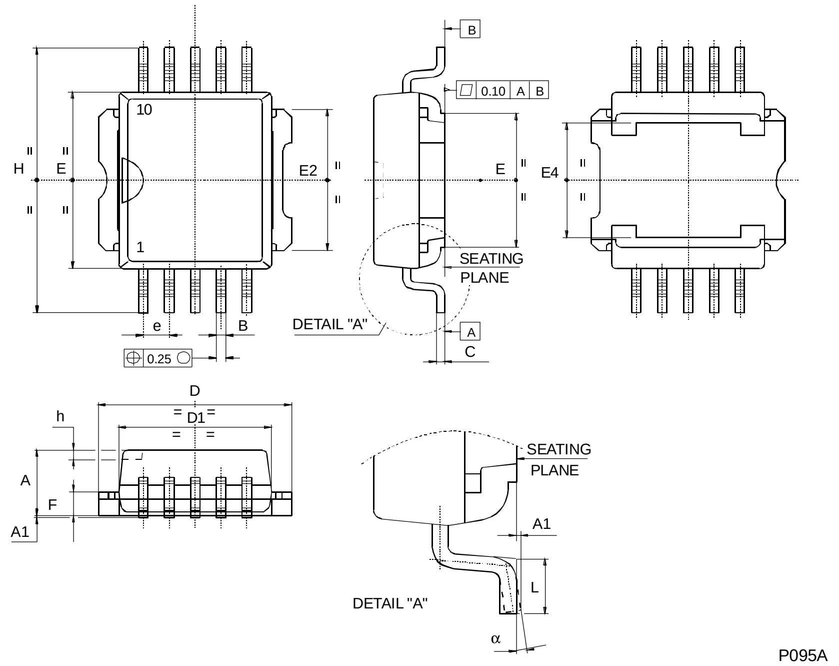
Thermal Parameter

Area/island (cm²)	**0.5**	**2**	**4**	**8**
R1=R7=R9=R11 (°C/W)	0.15			
R2=R8=R10=R12 (°C/W)	0.5			
R3 (°C/W)	0.4			
R4 (°C/W)	10			
R5 (°C/W)	15			
R6 (°C/W)	26	14.5	10	6
C1=C7=C9=C11 (W.s/°C)	0.0006			
C2=C8=C10=C12 (W.s/°C)	0.0021			
C3 (W.s/°C)	0.02			
C4 (W.s/°C)	0.5			
C5 (W.s/°C)	1.5			
C6 (W.s/°C)	5	10	14	18

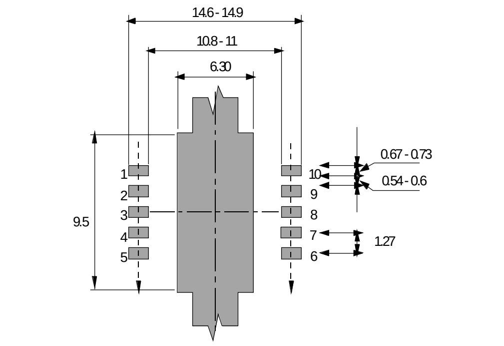
PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0º		8º	0º		8º
α (*)	2º		8º	2º		8º

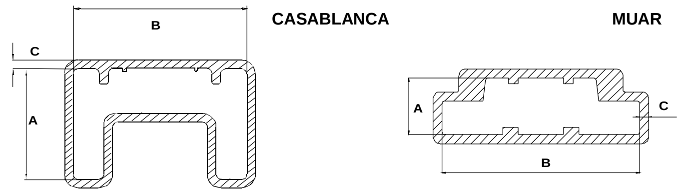
(*) Muar only POA P013P



PowerSO-10™ SUGGESTED PAD LAYOUT



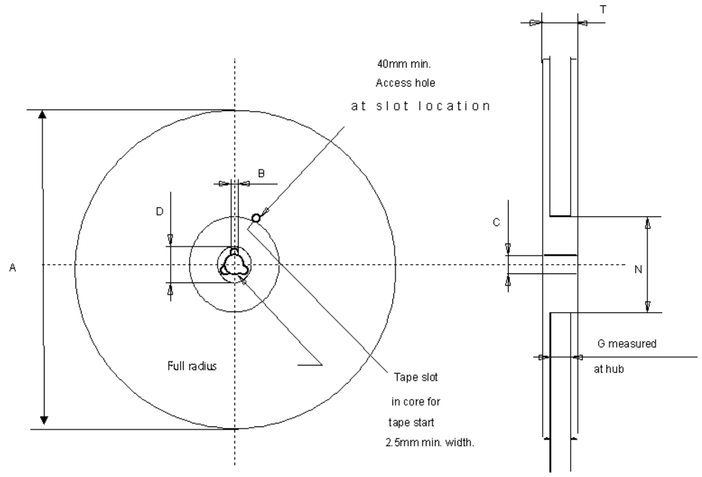
TUBE SHIPMENT (no suffix)



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

TAPE AND REEL SHIPMENT (suffix “13TR”)



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

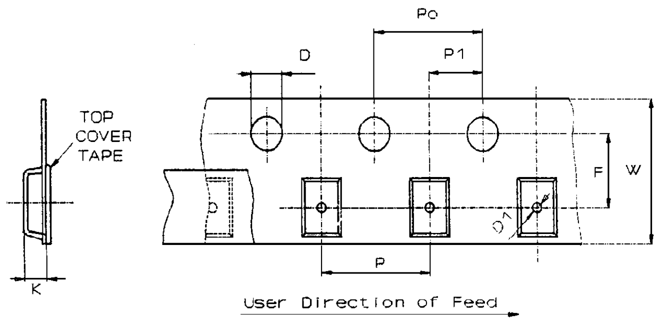
All dimensions are in mm.

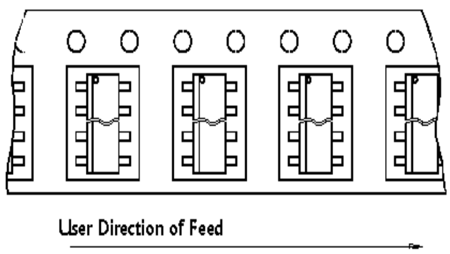
TAPE DIMENSIONS

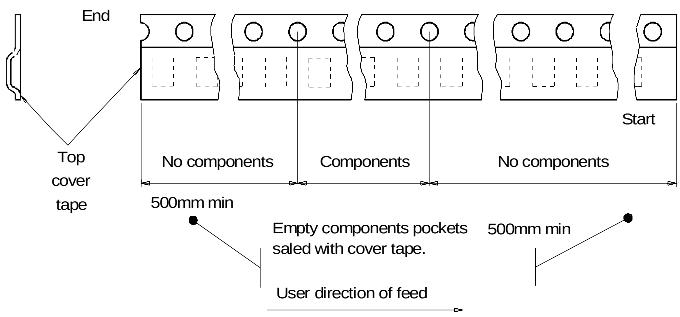
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







REVISION HISTORY

Date	Revision	Description of Changes
Jul 2004	1	- Minor changes - Current and voltage convention update (page 2). - "Configuration diagram (top view) & suggested connections for unused and n.c. pins" insertion (page 3). - 6 cm^2 Cu condition insertion in Thermal Data table (page 3). - V_{CC} - OUTPUT DIODE section update (page 3). - PROTECTIONS note insertion (page 4) - Revision History table insertion (page 18). - Disclaimers update (page 19).
Jul 2004	2	- Disclaimers update (page 19).

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