



# VNQ830A-E

## QUAD CHANNEL HIGH SIDE DRIVER

### TARGET SPECIFICATION

**Table 1. General Features**

| Type      | $R_{DS(on)}$     | $I_{out}$ | $V_{CC}$ |
|-----------|------------------|-----------|----------|
| VNQ830A-E | 60m $\Omega$ (*) | 6A (*)    | 36V      |

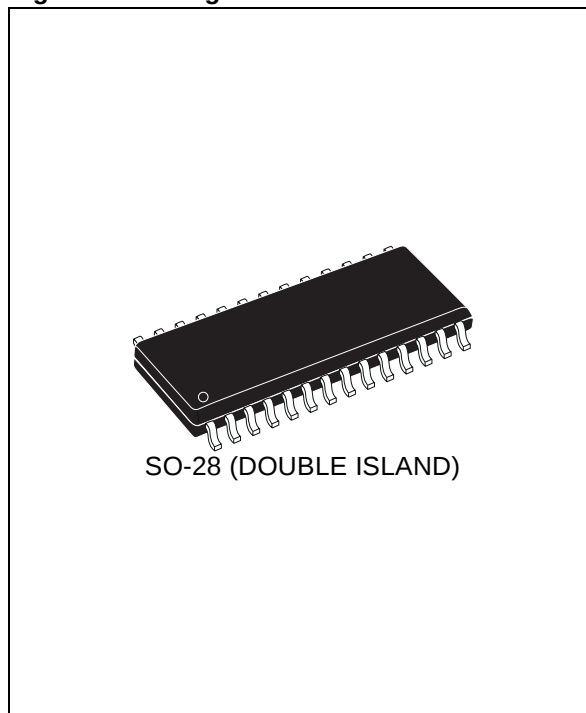
(\*) Per each channel

- DC SHORT CIRCUIT CURRENT: 6A
- CMOS COMPATIBLE INPUTS
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
  - LOSS OF GROUND AND LOSS OF  $V_{CC}$
- REVERSE BATTERY PROTECTION (\*\*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

### DESCRIPTION

The VNQ830A-E is a quad HSD formed by assembling two VND830A-E chips in the same SO-28 package. The VND830A-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology. The VNQ830A-E is intended for driving any type of multiple loads with one side connected to ground. This device has four independent channels and four analog sense outputs which deliver currents proportional to the outputs currents.

**Figure 1. Package**



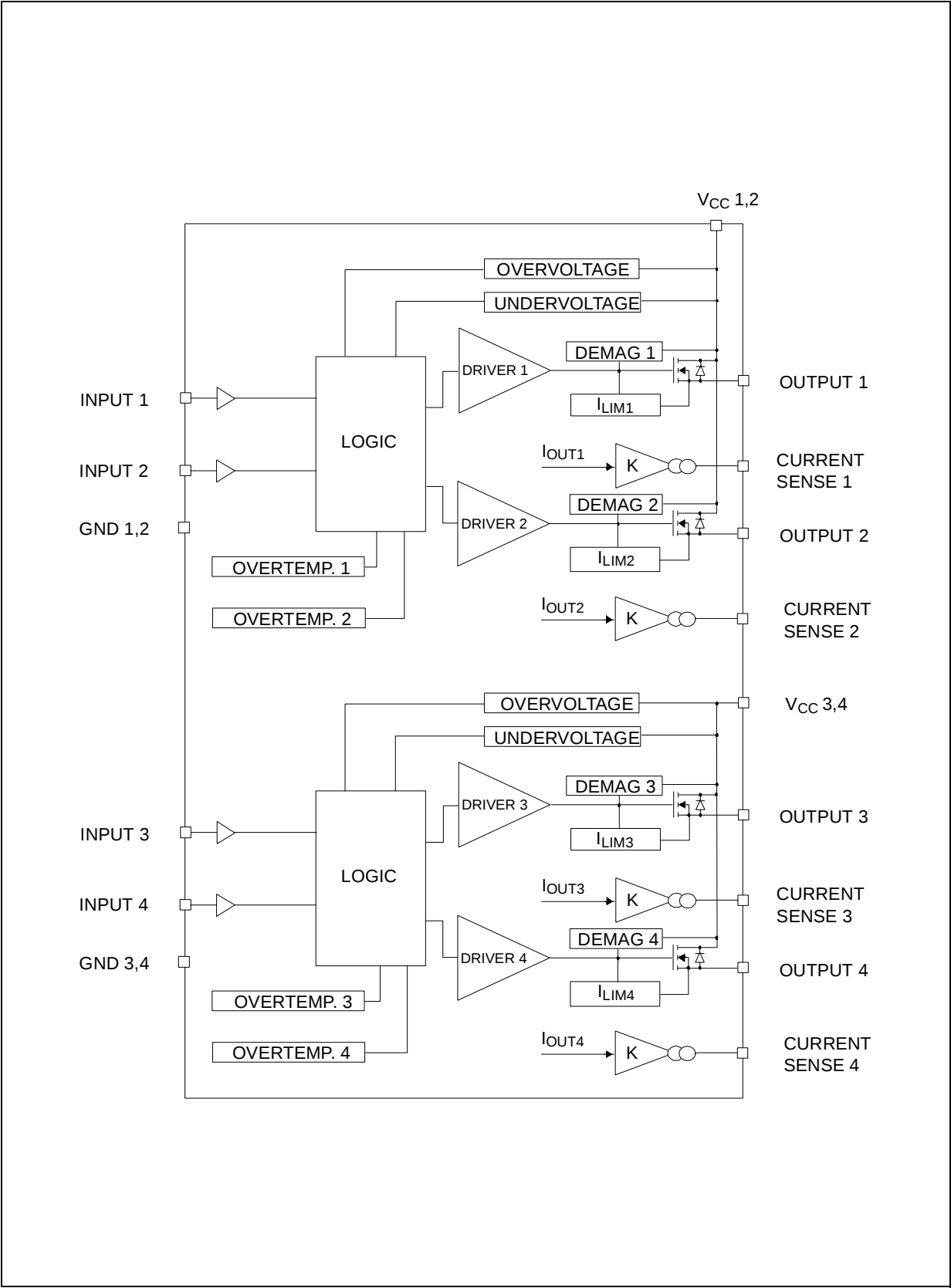
Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

**Table 2. Order Codes**

| Package | Tube      | Tape and Reel |
|---------|-----------|---------------|
| SO-28   | VNQ830A-E | VNQ830ATR-E   |

Note: (\*\*) See application schematic at page 10

Figure 2. Block Diagram



**Table 3. Absolute Maximum Ratings**

| Symbol              | Parameter                                                       | Value              | Unit   |
|---------------------|-----------------------------------------------------------------|--------------------|--------|
| V <sub>CC</sub>     | DC Supply Voltage                                               | 41                 | V      |
| - V <sub>CC</sub>   | Reverse DC Supply Voltage                                       | - 0.3              | V      |
| - I <sub>GND</sub>  | DC Reverse Ground Pin Current                                   | - 200              | mA     |
| I <sub>OUT</sub>    | DC Output Current                                               | Internally Limited | A      |
| I <sub>R</sub>      | Reverse Output Current                                          | - 6                | A      |
| I <sub>IN</sub>     | Input Current                                                   | +/- 10             | mA     |
| V <sub>CSENSE</sub> | Current Sense Maximum Voltage                                   | -3<br>+15          | V<br>V |
| V <sub>ESD</sub>    | Electrostatic Discharge (Human Body Model:<br>R=1.5KΩ; C=100pF) |                    |        |
|                     | - INPUT                                                         | 4000               | V      |
|                     | - CURRENT SENSE                                                 | 2000               | V      |
|                     | - OUTPUT                                                        | 5000               | V      |
|                     | - V <sub>CC</sub>                                               | 5000               | V      |
| P <sub>tot</sub>    | Power dissipation (per island) at T <sub>lead</sub> =25°C       | 6.25               | W      |
| T <sub>j</sub>      | Junction Operating Temperature                                  | Internally Limited | °C     |
| T <sub>stg</sub>    | Storage Temperature                                             | - 55 to 150        | °C     |

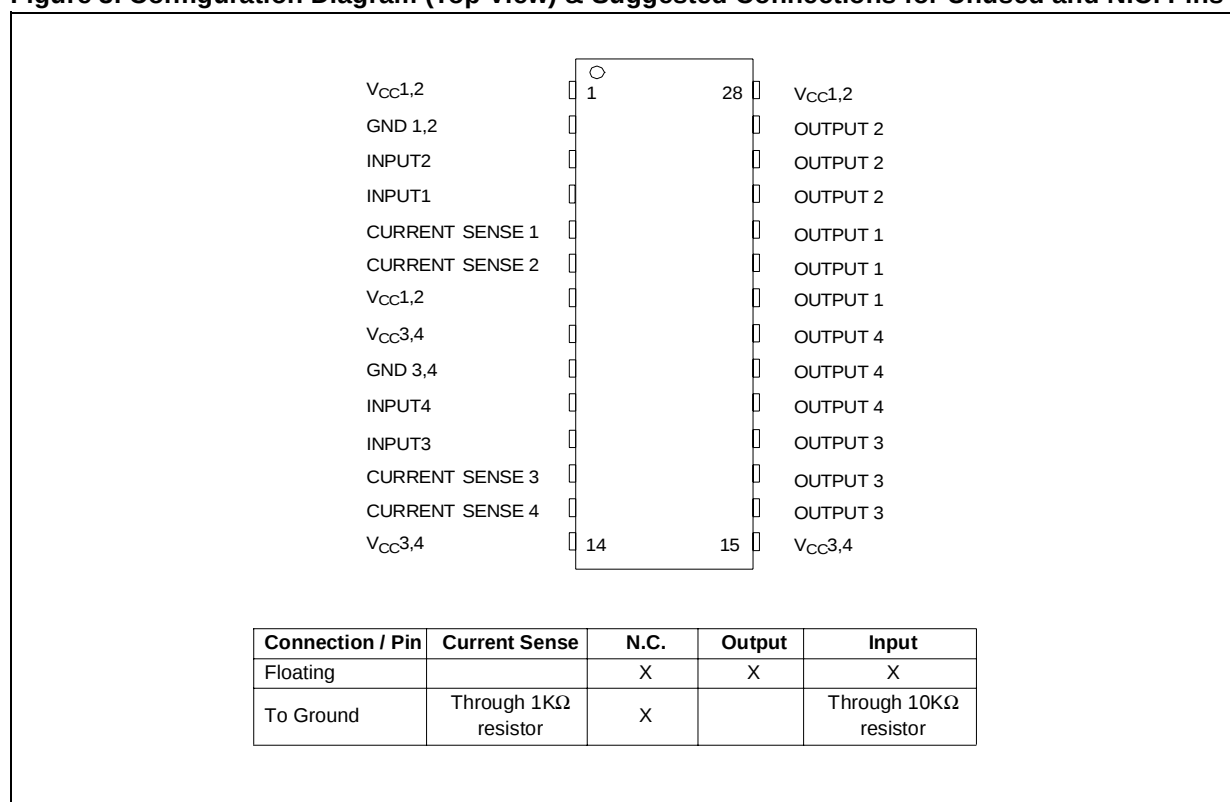
**Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins**

Figure 4. Current and Voltage Conventions

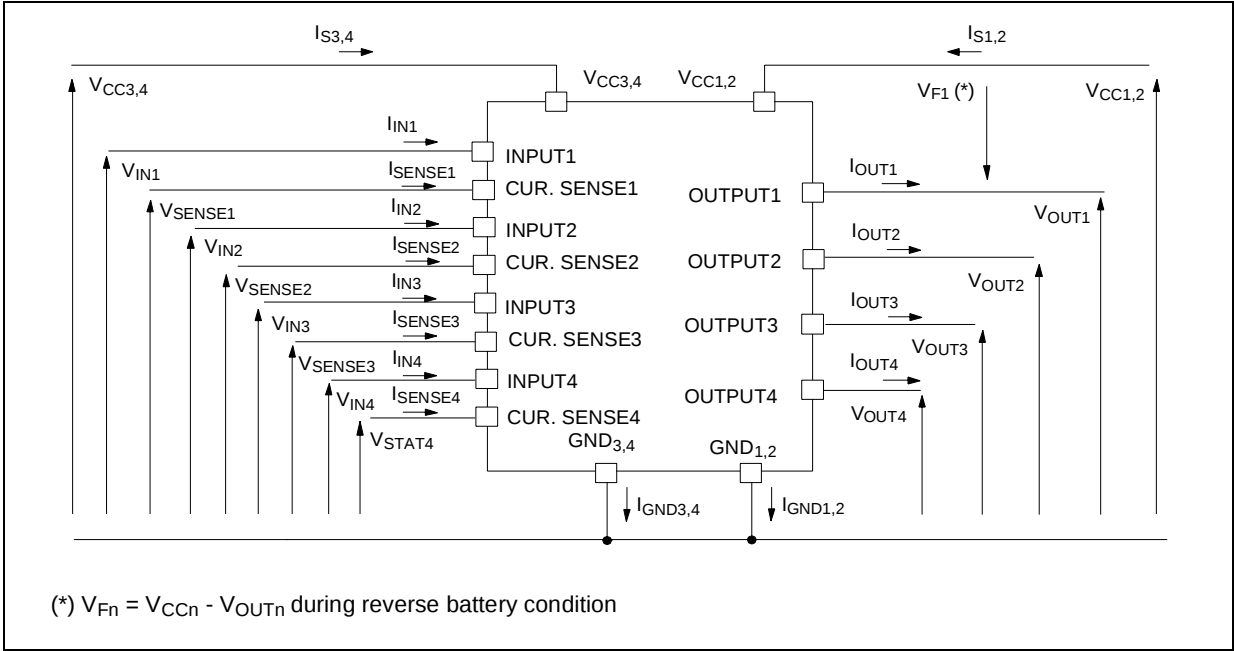


Table 4. Thermal Data (Per island)

| Symbol                | Parameter                                          | Value             |                   | Unit |
|-----------------------|----------------------------------------------------|-------------------|-------------------|------|
| R <sub>thj-lead</sub> | Thermal Resistance Junction-lead per chip          | 20                |                   | °C/W |
| R <sub>thj-amb</sub>  | Thermal Resistance Junction-ambient (one chip ON)  | 60 <sup>(1)</sup> | 44 <sup>(2)</sup> | °C/W |
| R <sub>thj-amb</sub>  | Thermal Resistance Junction-ambient (two chips ON) | 46 <sup>(1)</sup> | 31 <sup>(2)</sup> | °C/W |

Note: <sup>(1)</sup> When mounted on a standard single-sided FR-4 board with 50mm<sup>2</sup> of Cu per island (at least 35µm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.

Note: <sup>(2)</sup> When mounted on a standard single-sided FR-4 board with 6cm<sup>2</sup> of Cu per island (at least 35µm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.

**ELECTRICAL CHARACTERISTICS**(8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C, unless otherwise specified)

(Per each channel)

**Table 5. Power Output**

| Symbol                | Parameter                | Test Conditions                                                                                             | Min. | Typ. | Max.      | Unit     |
|-----------------------|--------------------------|-------------------------------------------------------------------------------------------------------------|------|------|-----------|----------|
| V <sub>CC</sub> (**)  | Operating Supply Voltage |                                                                                                             | 5.5  | 13   | 36        | V        |
| V <sub>USD</sub> (**) | Undervoltage Shut-down   |                                                                                                             | 3    | 4    | 5.5       | V        |
| V <sub>OV</sub> (**)  | Overvoltage Shut-down    |                                                                                                             | 36   |      |           | V        |
| R <sub>ON</sub>       | On State Resistance      | I <sub>OUT</sub> = 2A; T <sub>j</sub> = 25°C<br>I <sub>OUT</sub> = 2A; T <sub>j</sub> = 150°C               |      |      | 60<br>120 | mΩ<br>mΩ |
| V <sub>clamp</sub>    | Clamp voltage            | I <sub>CC</sub> = 20 mA (see note 1)                                                                        | 41   | 48   | 55        | V        |
| I <sub>S</sub> (**)   | Supply Current           | Off State; V <sub>CC</sub> = 13V; V <sub>IN</sub> = V <sub>OUT</sub> = 0V                                   |      | 12   | 40        | μA       |
|                       |                          | Off State; V <sub>CC</sub> = 13V; V <sub>IN</sub> = V <sub>OUT</sub> = 0V;<br>T <sub>j</sub> = 25°C         |      | 12   | 25        | μA       |
|                       |                          | On State; V <sub>IN</sub> = 5V; V <sub>CC</sub> = 13V; I <sub>OUT</sub> = 0A;<br>R <sub>SENSE</sub> = 3.9KΩ |      |      | 7         | mA       |
| I <sub>L(off1)</sub>  | Off State Output Current | V <sub>IN</sub> = V <sub>OUT</sub> = 0V                                                                     | 0    |      | 50        | μA       |
| I <sub>L(off3)</sub>  | Off State Output Current | V <sub>IN</sub> = V <sub>OUT</sub> = 0V; V <sub>CC</sub> = 13V; T <sub>j</sub> = 125°C                      |      |      | 5         | μA       |
| I <sub>L(off4)</sub>  | Off State Output Current | V <sub>IN</sub> = V <sub>OUT</sub> = 0V; V <sub>CC</sub> = 13V; T <sub>j</sub> = 25°C                       |      |      | 3         | μA       |

Note: (\*\*) Per island

Note: 1. V<sub>clamp</sub> and V<sub>OV</sub> are correlated. Typical difference is 5V**Table 6. Protection** (Per each channel) (see note 2)

| Symbol             | Parameter                      | Test Conditions                                       | Min                  | Typ                  | Max                  | Unit   |
|--------------------|--------------------------------|-------------------------------------------------------|----------------------|----------------------|----------------------|--------|
| I <sub>lim</sub>   | Current limitation             | V <sub>CC</sub> = 13V<br>5.5V < V <sub>CC</sub> < 36V | 6                    | 9                    | 15<br>15             | A<br>A |
| T <sub>TSD</sub>   | Thermal shut-down temperature  |                                                       | 150                  | 175                  | 200                  | °C     |
| T <sub>R</sub>     | Thermal reset temperature      |                                                       | 135                  |                      |                      | °C     |
| T <sub>HYST</sub>  | Thermal hysteresis             |                                                       | 7                    | 15                   |                      | °C     |
| V <sub>demag</sub> | Turn-off output voltage clamp  | I <sub>OUT</sub> = 2A; V <sub>IN</sub> = 0V; L = 6mH  | V <sub>CC</sub> - 41 | V <sub>CC</sub> - 48 | V <sub>CC</sub> - 55 | V      |
| V <sub>ON</sub>    | Output voltage drop limitation | I <sub>OUT</sub> = 10mA                               |                      | 50                   |                      | mV     |

Note: 2. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

**Table 7. Switching** (Per each channel) (V<sub>CC</sub> = 13V)

| Symbol                                 | Parameter              | Test Conditions                                                                     | Min | Typ  | Max | Unit |
|----------------------------------------|------------------------|-------------------------------------------------------------------------------------|-----|------|-----|------|
| t <sub>d(on)</sub>                     | Turn-on Delay Time     | R <sub>L</sub> = 6.5Ω from V <sub>IN</sub> rising edge to V <sub>OUT</sub> = 1.3V   |     | 30   |     | μs   |
| t <sub>d(off)</sub>                    | Turn-off Delay Time    | R <sub>L</sub> = 6.5Ω from V <sub>IN</sub> falling edge to V <sub>OUT</sub> = 11.7V |     | 30   |     | μs   |
| dV <sub>OUT</sub> /dt <sub>(on)</sub>  | Turn-on Voltage Slope  | R <sub>L</sub> = 6.5Ω from V <sub>OUT</sub> = 1.3V to V <sub>OUT</sub> = 10.4V      |     | 0.40 |     | V/μs |
| dV <sub>OUT</sub> /dt <sub>(off)</sub> | Turn-off Voltage Slope | R <sub>L</sub> = 6.5Ω from V <sub>OUT</sub> = 11.7V to V <sub>OUT</sub> = 1.3V      |     | 0.40 |     | V/μs |

## ELECTRICAL CHARACTERISTICS (continued)

Table 8.  $V_{CC}$  - Output Diode (Per each channel)

| Symbol | Parameter          | Test Conditions                      | Min | Typ | Max | Unit |
|--------|--------------------|--------------------------------------|-----|-----|-----|------|
| $V_F$  | Forward on Voltage | $-I_{OUT}=1.3A$ ; $T_J=150^{\circ}C$ |     |     | 0.6 | V    |

Table 9. Logic Input (Per each channel)

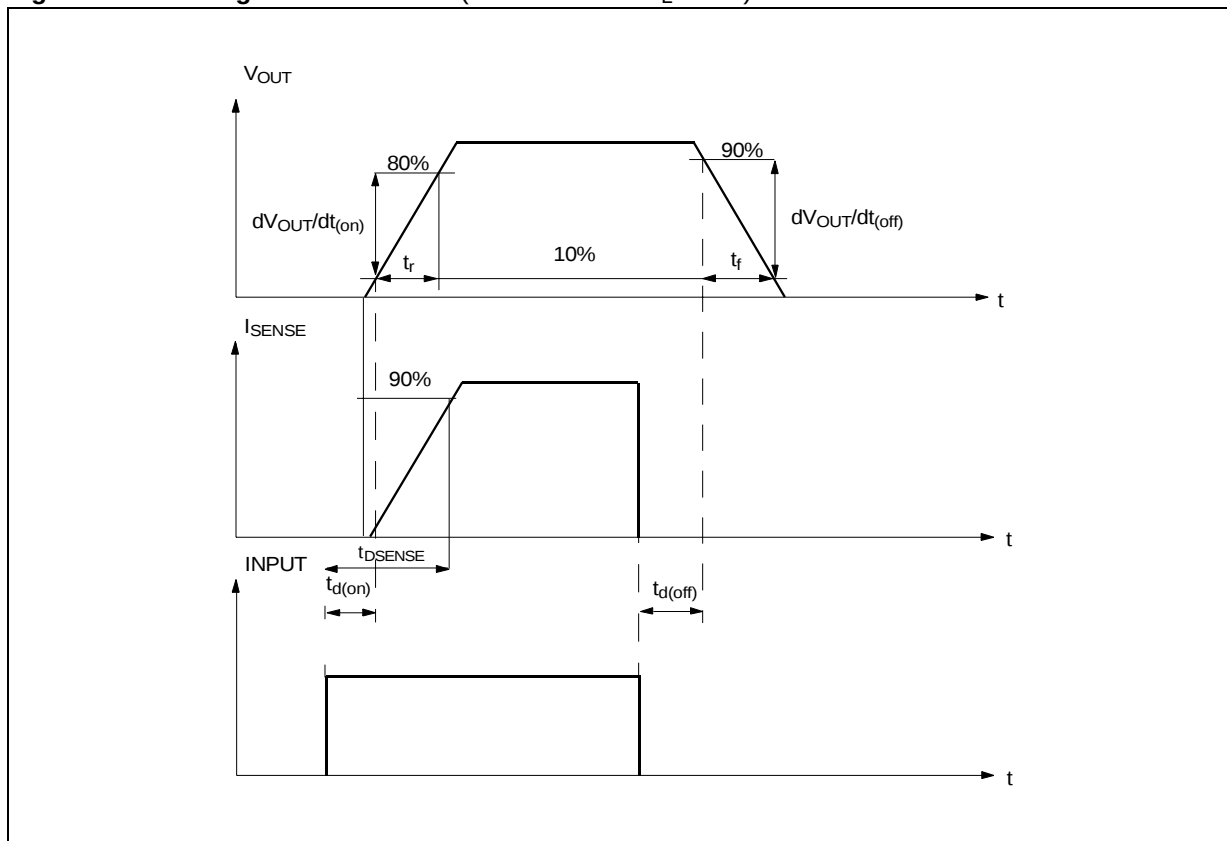
| Symbol        | Parameter                | Test Conditions | Min  | Typ  | Max  | Unit    |
|---------------|--------------------------|-----------------|------|------|------|---------|
| $V_{IL}$      | Input Low Level          |                 |      |      | 1.25 | V       |
| $I_{IL}$      | Low Level Input Current  | $V_{IN}=1.25V$  | 1    |      |      | $\mu A$ |
| $V_{IH}$      | Input High Level         |                 | 3.25 |      |      | V       |
| $I_{IH}$      | High Level Input Current | $V_{IN}=3.25V$  |      |      | 10   | $\mu A$ |
| $V_{I(hyst)}$ | Input Hysteresis Voltage |                 | 0.5  |      |      | V       |
| $V_{ICL}$     | Input Clamp Voltage      | $I_{IN}=1mA$    | 6    | 6.8  | 8    | V       |
|               |                          | $I_{IN}=-1mA$   |      | -0.7 |      | V       |

Table 10. Current Sense ( $9V \leq V_{CC} \leq 16V$ ) (See fig. 5)

| Symbol       | Parameter                                                | Test Conditions                                                                                                | Min  | Typ  | Max  | Unit     |
|--------------|----------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $K_1$        | $I_{OUT}/I_{SENSE}$                                      | $I_{OUT1,3}$ or $I_{OUT2,4}=0.25A$ ; $V_{SENSE}=0.5V$ ; other channels open; $T_J=-40^{\circ}C...150^{\circ}C$ | 1000 | 1400 | 1900 |          |
| $dK_1/K_1$   | Current Sense Ratio Drift                                | $I_{OUT1,3}$ or $I_{OUT2,4}=0.25A$ ; $V_{SENSE}=0.5V$ ; other channels open; $T_J=-40^{\circ}C...150^{\circ}C$ | -10  |      | +10  | %        |
| $K_2$        | $I_{OUT}/I_{SENSE}$                                      | $I_{OUT1,3}$ or $I_{OUT2,4}=1.6A$ ; $V_{SENSE}=4V$ ; other channels open; $T_J=-40^{\circ}C$                   | 1280 | 1500 | 1800 |          |
|              |                                                          | $T_J=25^{\circ}C...150^{\circ}C$                                                                               | 1300 | 1500 | 1780 |          |
| $dK_2/K_2$   | Current Sense Ratio Drift                                | $I_{OUT1,3}$ or $I_{OUT2,4}=1.6A$ ; $V_{SENSE}=4V$ ; other channels open; $T_J=-40^{\circ}C...150^{\circ}C$    | -6   |      | +6   | %        |
| $K_3$        | $I_{OUT}/I_{SENSE}$                                      | $I_{OUT1,3}$ or $I_{OUT2,4}=2.5A$ ; $V_{SENSE}=4V$ ; other channels open; $T_J=-40^{\circ}C$                   | 1280 | 1500 | 1680 |          |
|              |                                                          | $T_J=25^{\circ}C...150^{\circ}C$                                                                               | 1340 | 1500 | 1600 |          |
| $dK_3/K_3$   | Current Sense Ratio Drift                                | $I_{OUT1,3}$ or $I_{OUT2,4}=2.5A$ ; $V_{SENSE}=4V$ ; other channels open; $T_J=-40^{\circ}C...150^{\circ}C$    | -6   |      | +6   | %        |
| $I_{SENSE}$  | Analog Sense Leakage Current                             | $V_{IN}=0V$ ; $I_{OUT}=0A$ ; $V_{SENSE}=0V$ ; $T_J=-40^{\circ}C...150^{\circ}C$                                | 0    |      | 5    | $\mu A$  |
|              |                                                          | $V_{IN}=5V$ ; $I_{OUT}=0A$ ; $V_{SENSE}=0V$ ; $T_J=-40^{\circ}C...150^{\circ}C$                                | 0    |      | 10   | $\mu A$  |
| $V_{SENSE}$  | Max analog sense output voltage                          | $V_{CC}=5.5V$ ; $I_{OUT}=1.3A$ ; $R_{SENSE}=10k\Omega$                                                         | 2    |      |      | V        |
|              |                                                          | $V_{CC}>8V$ ; $I_{OUT}=2.5A$ ; $R_{SENSE}=10k\Omega$                                                           | 4    |      |      | V        |
| $V_{SENSEH}$ | Analog sense output voltage in overtemperature condition | $V_{CC}=13V$ ; $R_{SENSE}=3.9k\Omega$                                                                          |      | 5.5  |      | V        |
| $R_{SENSE}$  | Intrinsic sense pin resistance                           | $V_{CC}=13V$ ; $T_J>T_{TSD}$ ; All Channels Open                                                               |      | 400  |      | $\Omega$ |
| $t_{DSENSE}$ | Current sense delay response                             | to 90% $I_{SENSE}$ (see note 3)                                                                                |      |      | 500  | $\mu s$  |

Note: 3. Current sense signal delay after positive input slope.

Note: 4. Sense pin doesn't have to be left floating.

**Figure 5. Switching Characteristics** (Resistive load  $R_L=6.5\Omega$ )**Table 11. Truth Table** (per channel)

| CONDITIONS                    | INPUT | OUTPUT | SENSE                          |
|-------------------------------|-------|--------|--------------------------------|
| Normal operation              | L     | L      | 0                              |
|                               | H     | H      | Nominal                        |
| Overtemperature               | L     | L      | 0                              |
|                               | H     | L      | $V_{SENSEH}$                   |
| Undervoltage                  | L     | L      | 0                              |
|                               | H     | L      | 0                              |
| Overvoltage                   | L     | L      | 0                              |
|                               | H     | L      | 0                              |
| Short circuit to GND          | L     | L      | 0                              |
|                               | H     | L      | $(T_j < T_{TSD})$ 0            |
|                               | H     | L      | $(T_j > T_{TSD})$ $V_{SENSEH}$ |
| Short circuit to $V_{CC}$     | L     | H      | 0                              |
|                               | H     | H      | < Nominal                      |
| Negative output voltage clamp | L     | L      | 0                              |

Table 12. Electrical Transient Requirements

| ISO T/R 7637/1<br>Test Pulse | TEST LEVELS |         |         |         |                         |
|------------------------------|-------------|---------|---------|---------|-------------------------|
|                              | I           | II      | III     | IV      | Delays and Impedance    |
| 1                            | -25 V       | -50 V   | -75 V   | -100 V  | 2 ms 10 $\Omega$        |
| 2                            | +25 V       | +50 V   | +75 V   | +100 V  | 0.2 ms 10 $\Omega$      |
| 3a                           | -25 V       | -50 V   | -100 V  | -150 V  | 0.1 $\mu$ s 50 $\Omega$ |
| 3b                           | +25 V       | +50 V   | +75 V   | +100 V  | 0.1 $\mu$ s 50 $\Omega$ |
| 4                            | -4 V        | -5 V    | -6 V    | -7 V    | 100 ms, 0.01 $\Omega$   |
| 5                            | +26.5 V     | +46.5 V | +66.5 V | +86.5 V | 400 ms, 2 $\Omega$      |

| ISO T/R 7637/1<br>Test Pulse | TEST LEVELS RESULTS |    |     |    |
|------------------------------|---------------------|----|-----|----|
|                              | I                   | II | III | IV |
| 1                            | C                   | C  | C   | C  |
| 2                            | C                   | C  | C   | C  |
| 3a                           | C                   | C  | C   | C  |
| 3b                           | C                   | C  | C   | C  |
| 4                            | C                   | C  | C   | C  |
| 5                            | C                   | E  | E   | E  |

| CLASS | CONTENTS                                                                                                                                                                |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C     | All functions of the device are performed as designed after exposure to disturbance.                                                                                    |
| E     | One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

Figure 6. Waveforms

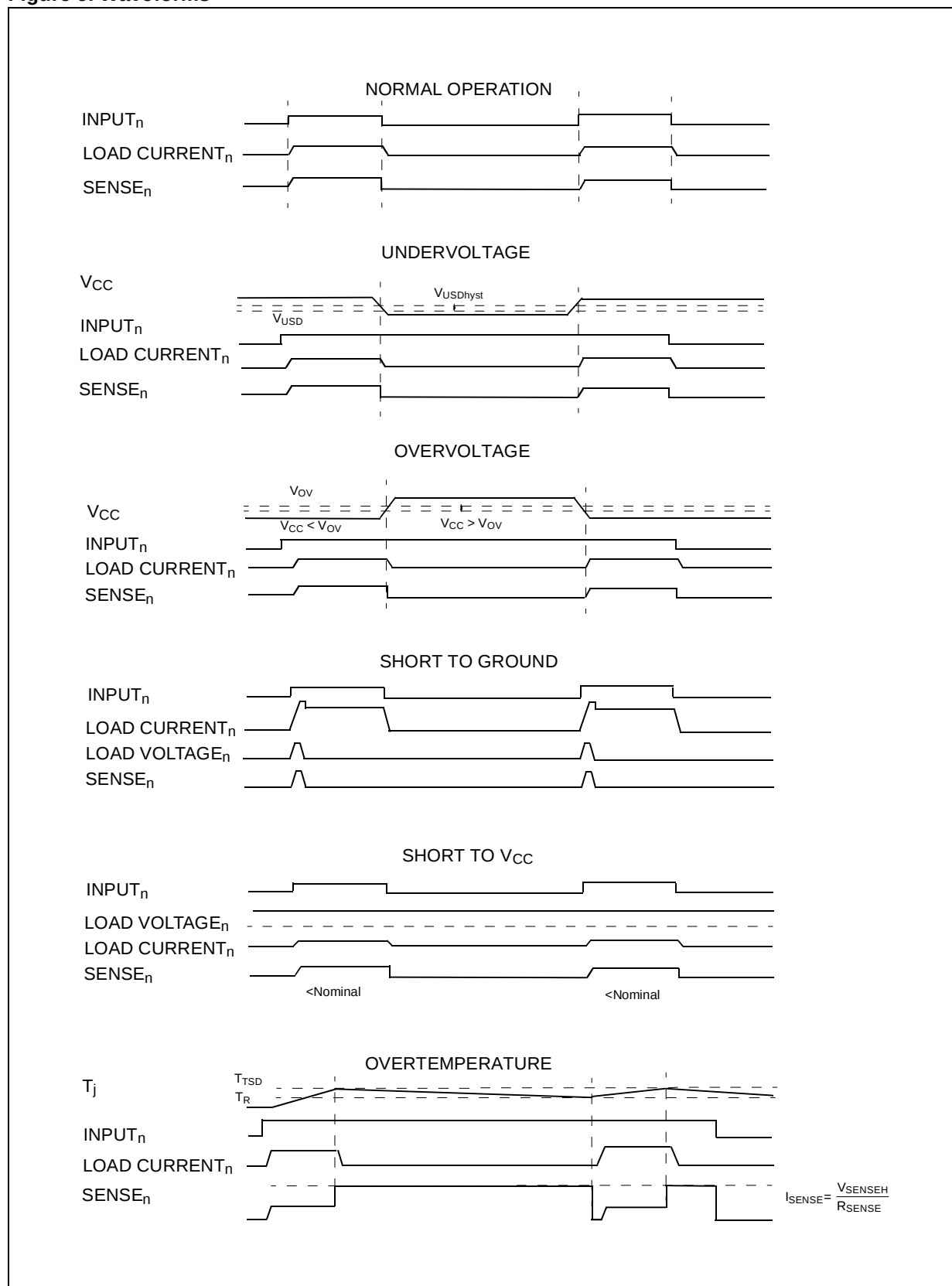
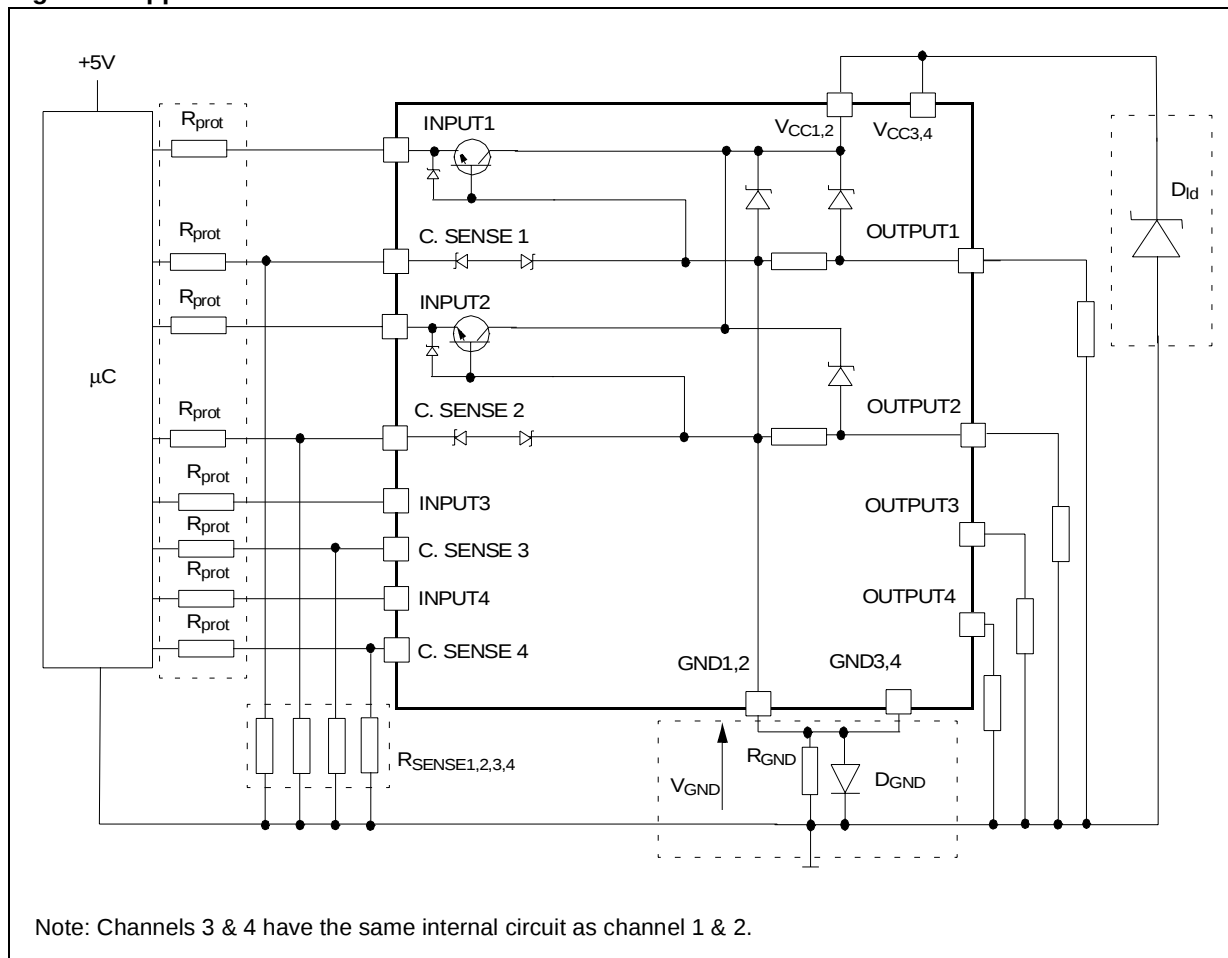


Figure 7. Application Schematic



### GND PROTECTION NETWORK AGAINST REVERSE BATTERY

**Solution 1:** Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600\text{mV} / 2(I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

**Solution 2:** A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1\text{k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600\text{mV}$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT line is also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT pin is to leave it unconnected, while unused SENSE pin has to be connected to Ground pin.

### LOAD DUMP PROTECTION

$D_{id}$  is necessary (Transil or MOV) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

**.μC I/Os PROTECTION:**

If a ground protection network is used and negative transients are present on the V<sub>CC</sub> line, the control pins will be pulled negative. ST suggests to insert a resistor (R<sub>prot</sub>) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V<sub>CCpeak</sub> = - 100V and I<sub>latchup</sub> ≥ 20mA; V<sub>OHμC</sub> ≥ 4.5V

$$5k\Omega \leq R_{prot} \leq 65k\Omega.$$

Recommended R<sub>prot</sub> value is 10kΩ

SO-28 Double Island Thermal Data

Figure 8. SO-28 Double Island PC Board

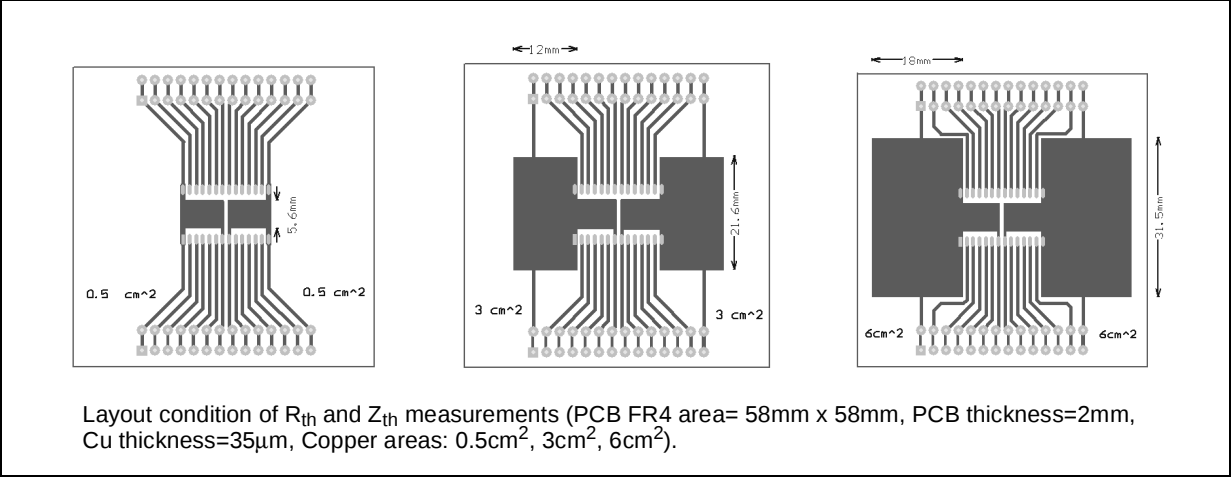


Table 13. Thermal Calculation According To The Pcb Heatsink Area

| Chip 1 | Chip 2 | $T_{jchip1}$                                                        | $T_{jchip2}$                                                        | Note                         |
|--------|--------|---------------------------------------------------------------------|---------------------------------------------------------------------|------------------------------|
| ON     | OFF    | $R_{thA} \times P_{dchip1} + T_{amb}$                               | $R_{thC} \times P_{dchip1} + T_{amb}$                               |                              |
| OFF    | ON     | $R_{thC} \times P_{dchip2} + T_{amb}$                               | $R_{thA} \times P_{dchip2} + T_{amb}$                               |                              |
| ON     | ON     | $R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$                | $R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$                | $P_{dchip1}=P_{dchip2}$      |
| ON     | ON     | $(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$ | $(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$ | $P_{dchip1} \neq P_{dchip2}$ |

$R_{thA}$  = Thermal resistance Junction to Ambient with one chip ON  
 $R_{thB}$  = Thermal resistance Junction to Ambient with both chips ON and  $P_{dchip1}=P_{dchip2}$   
 $R_{thC}$  = Mutual thermal resistance

Figure 9.  $R_{thj-amb}$  Vs. PCB Copper Area In Open Box Free Air Condition

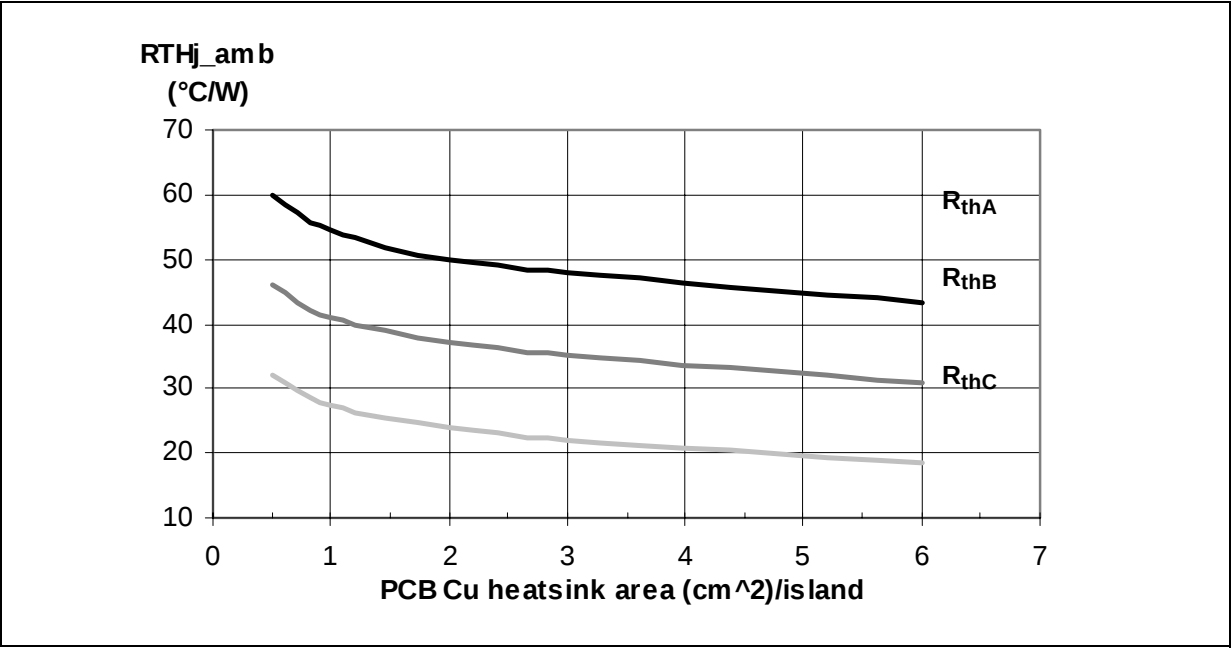


Figure 10. SO-28 Thermal Impedance Junction Ambient Single Pulse

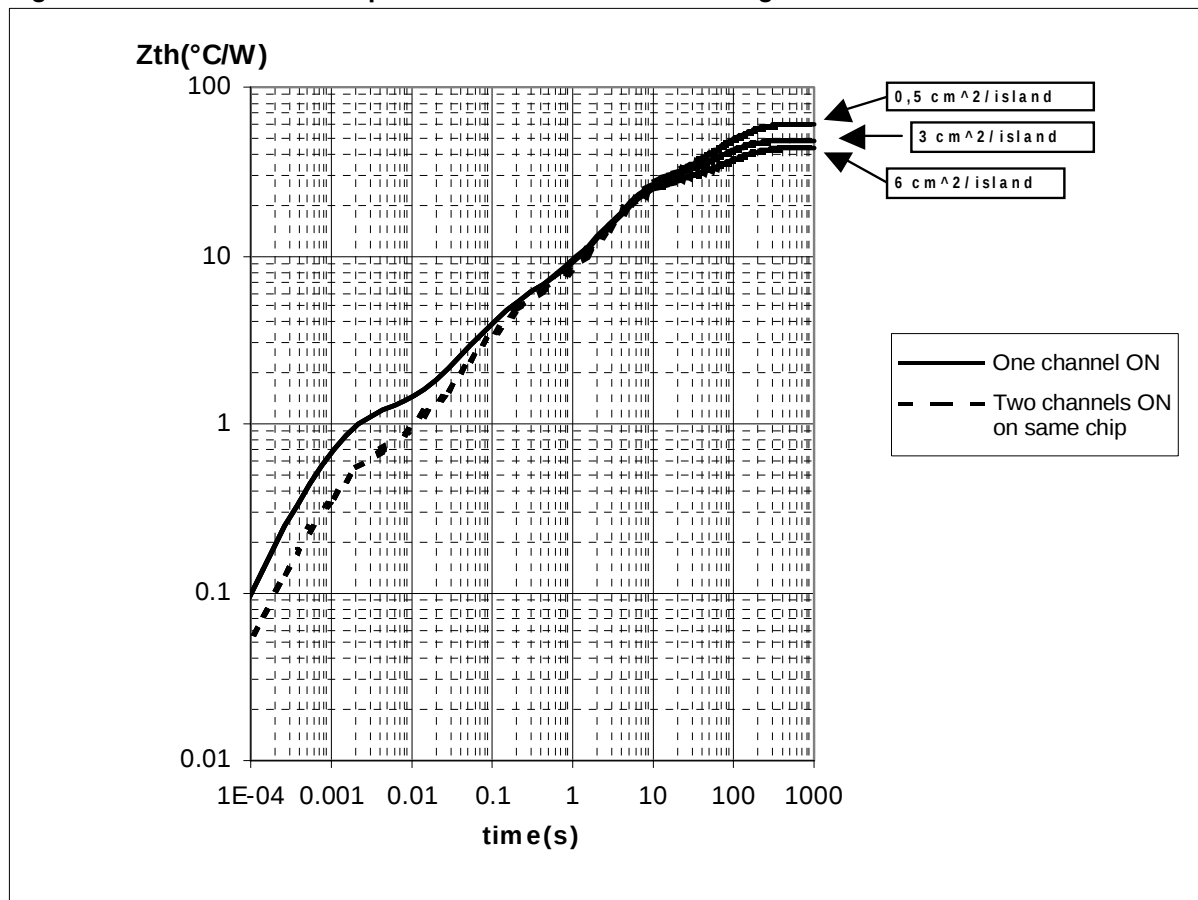
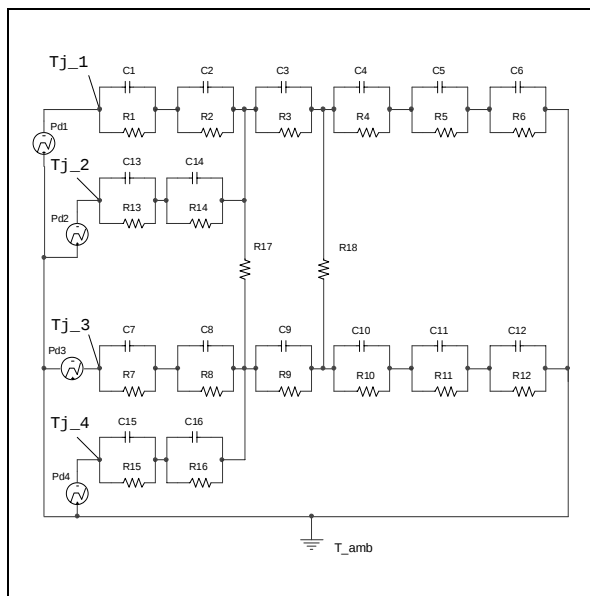


Figure 11. Thermal fitting model of a double channel HSD in SO-28



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Table 14. Thermal Parameter

| Area/island (cm <sup>2</sup> ) | 0.5      | 6  |
|--------------------------------|----------|----|
| R1=R7=R13=R15 (°C/W)           | 0.05     |    |
| R2=R8=R14=R16 (°C/W)           | 0.3      |    |
| R3=R9 (°C/W)                   | 3.4      |    |
| R4=R10 (°C/W)                  | 11       |    |
| R5=R11 (°C/W)                  | 15       |    |
| R6=R12 (°C/W)                  | 30       | 13 |
| C1=C7=C13=C15 (W.s/°C)         | 0.001    |    |
| C2=C8=C14=C16 (W.s/°C)         | 5.00E-03 |    |
| C3=C9 (W.s/°C)                 | 1.00E-02 |    |
| C4=C10 (W.s/°C)                | 0.2      |    |
| C5=C11 (W.s/°C)                | 1.5      |    |
| C6=C12 (W.s/°C)                | 5        | 8  |
| R17=R18 (°C/W)                 | 150      |    |

PACKAGE MECHANICAL

Table 15. SO-28 Mechanical Data

| Symbol | millimeters |            |       |
|--------|-------------|------------|-------|
|        | Min         | Typ        | Max   |
| A      |             |            | 2.65  |
| a1     | 0.10        |            | 0.30  |
| b      | 0.35        |            | 0.49  |
| b1     | 0.23        |            | 0.32  |
| C      |             | 0.50       |       |
| c1     |             | 45° (typ.) |       |
| D      | 17.7        |            | 18.1  |
| E      | 10.00       |            | 10.65 |
| e      |             | 1.27       |       |
| e3     |             | 16.51      |       |
| F      | 7.40        |            | 7.60  |
| L      | 0.40        |            | 1.27  |
| S      |             | 8° (max.)  |       |

Figure 12. SO-28 Package Dimensions

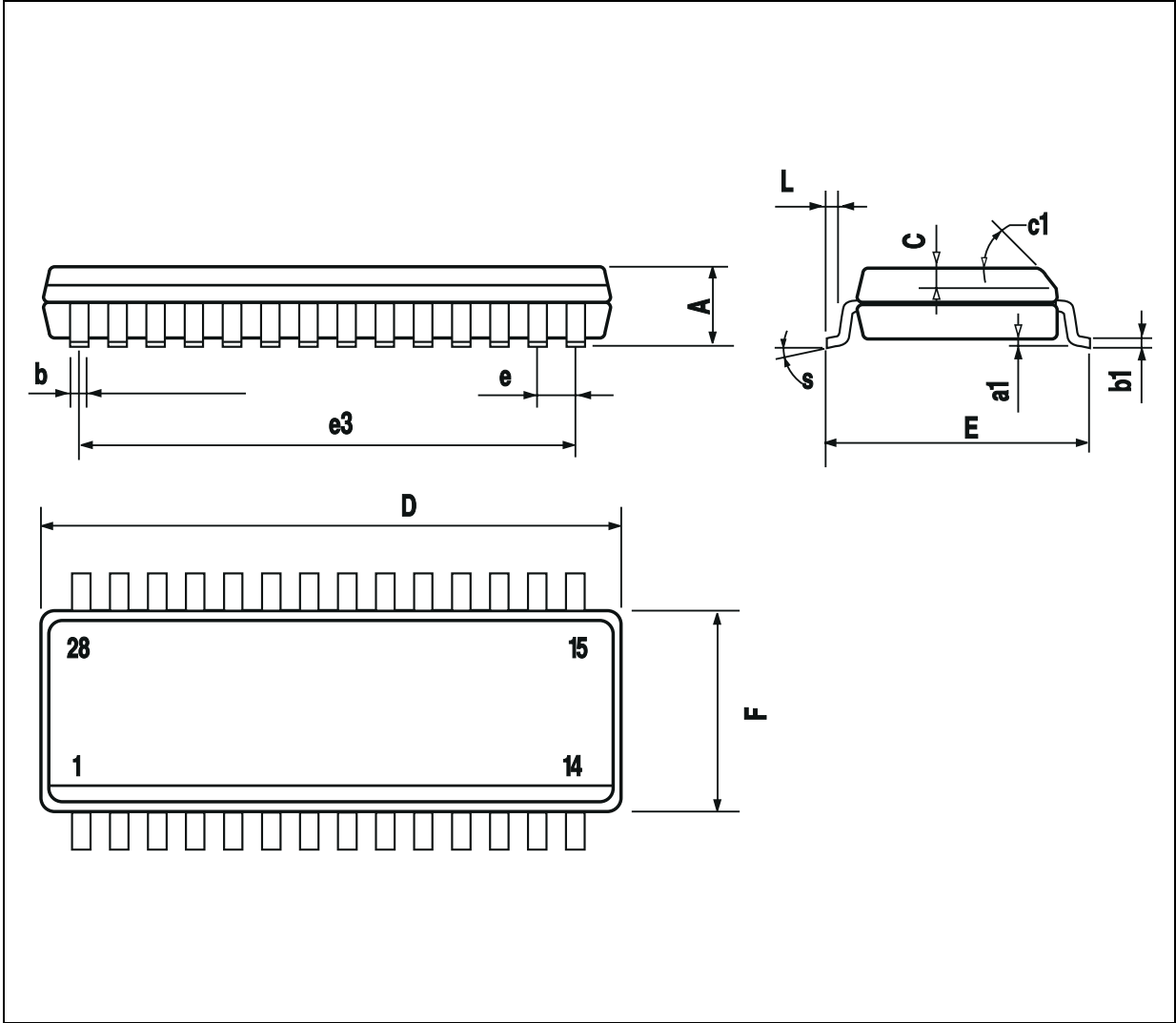


Figure 13. SO-28 Tube Shipment (No Suffix)

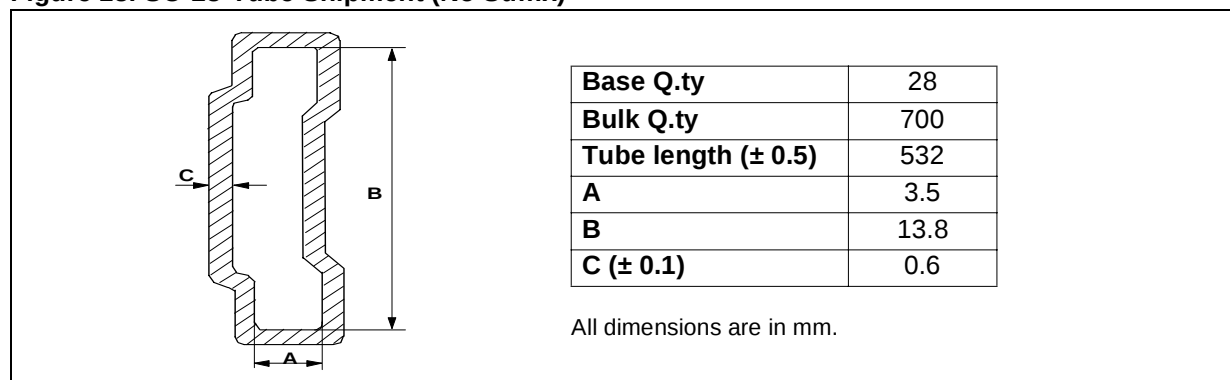
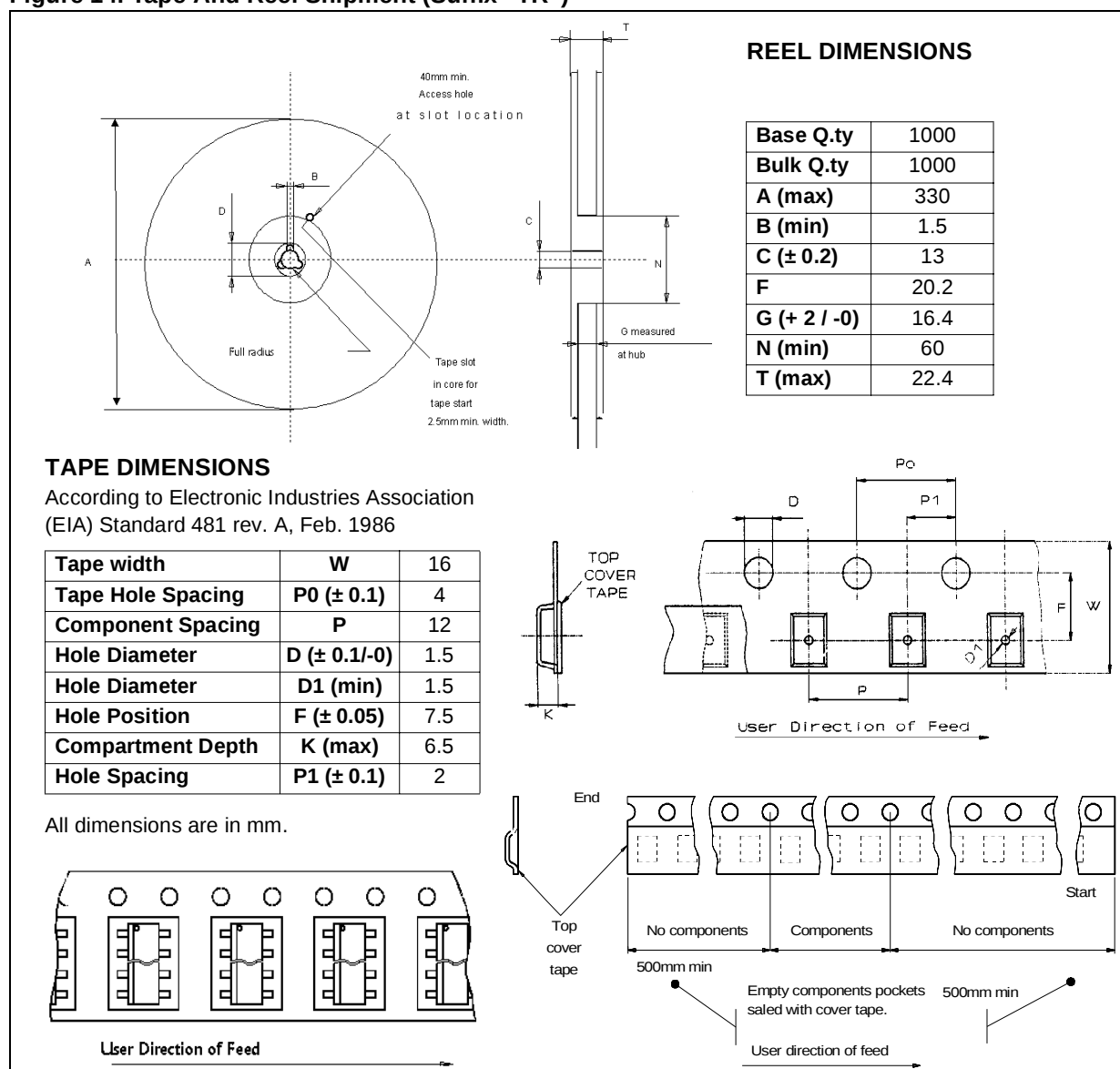


Figure 14. Tape And Reel Shipment (Suffix "TR")



**REVISION HISTORY**

| <b>Date</b> | <b>Revision</b> | <b>Description of Changes</b> |
|-------------|-----------------|-------------------------------|
| Sept. 2004  | 1               | - First Issue                 |

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