



VNQ830P-E

QUAD CHANNEL HIGH SIDE DRIVER

TARGET SPECIFICATION

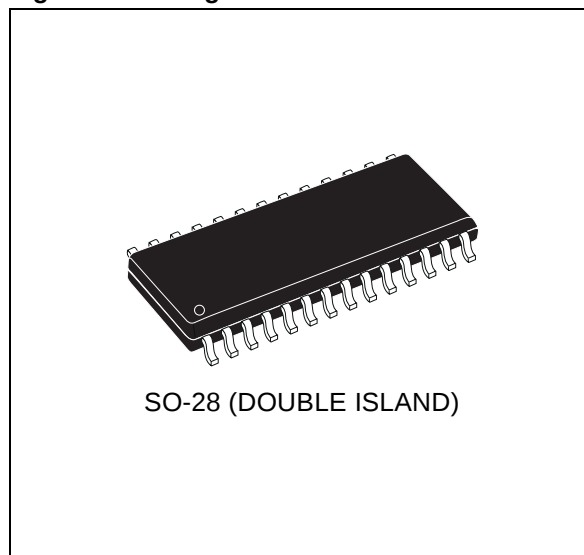
Table 1. General Features

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VNQ830P-E	65 m Ω (*)	6 A (*)	36 V

(*) Per each channel

- CMOS COMPATIBLE INPUTS
- OPEN DRAIN STATUS OUTPUTS
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (**)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package



DESCRIPTION

The VNQ830P-E is a quad HSD formed by assembling two VND830-E chips in the same SO-28 package. The VND830-E is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology. The VNQ830P-E is intended for driving any type of multiple loads with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the device against overload.

The device detects open load condition both in on and off state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
SO-28	VNQ830P-E	VNQ830PTR-E

Note: (**) See application schematic at page 11.

Figure 2. Block Diagram

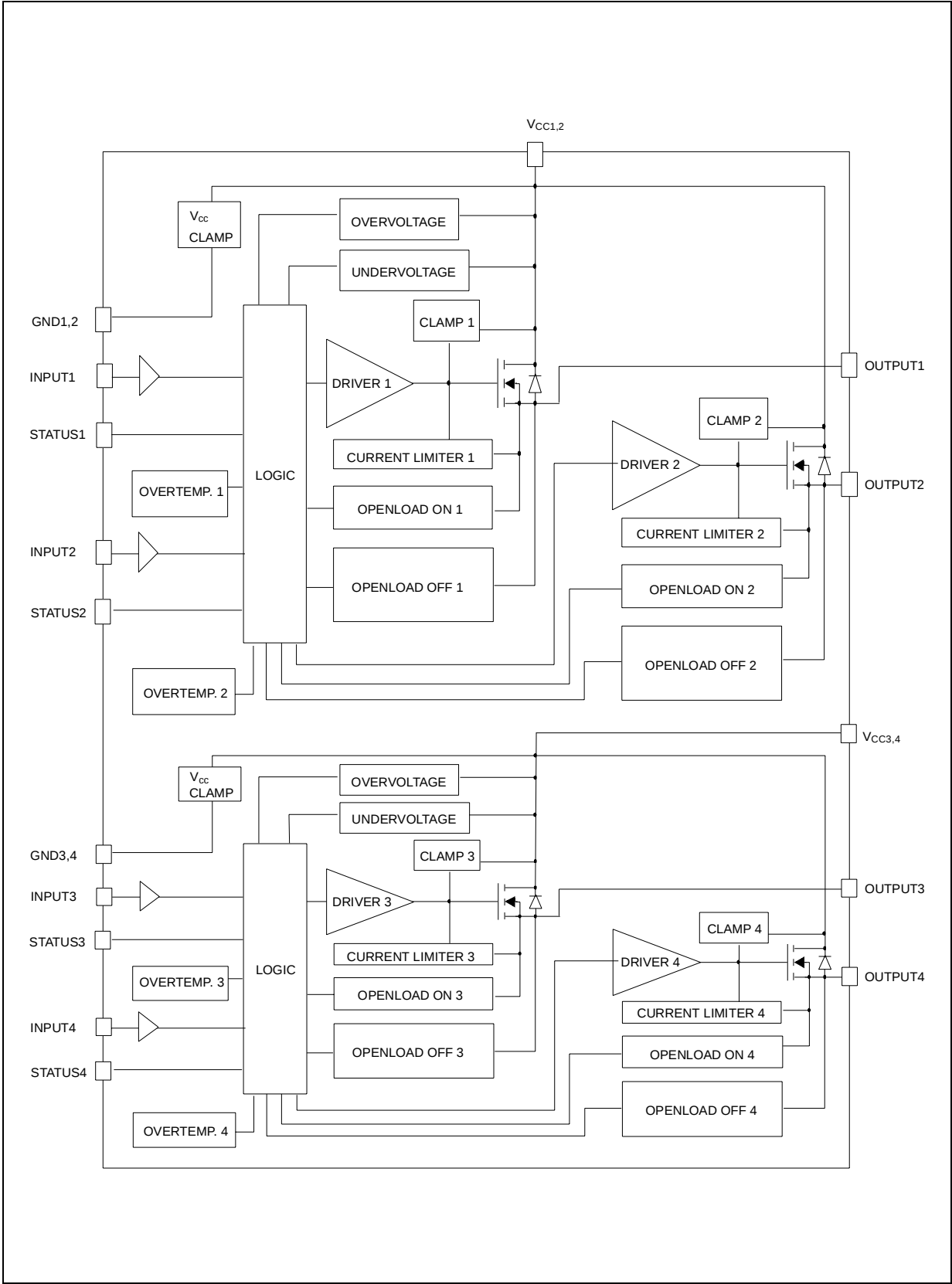


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	41	V
- V _{CC}	Reverse DC Supply Voltage	- 0.3	V
- I _{GND}	DC Reverse Ground Pin Current	- 200	mA
I _{OUT}	DC Output Current	Internally Limited	A
- I _{OUT}	Reverse DC Output Current	- 6	A
I _{IN}	DC Input Current	+/- 10	mA
I _{STAT}	DC Status Current	+/- 10	mA
V _{ESD}	Electrostatic Discharge (Human Body Model: R=1.5K Ω ; C=100pF)		
	- INPUT	4000	V
	- STATUS	4000	V
	- OUTPUT	5000	V
	- V _{CC}	5000	V
E _{MAX}	Maximum Switching Energy (L=1.5mH; R _L =0 Ω ; V _{bat} =13.5V; T _{jstart} =150°C; I _L =9A)	85	mJ
P _{tot}	Power dissipation (per island) at T _{lead} =25°C	6.25	W
T _j	Junction Operating Temperature	Internally Limited	°C
T _{stg}	Storage Temperature	- 55 to 150	°C

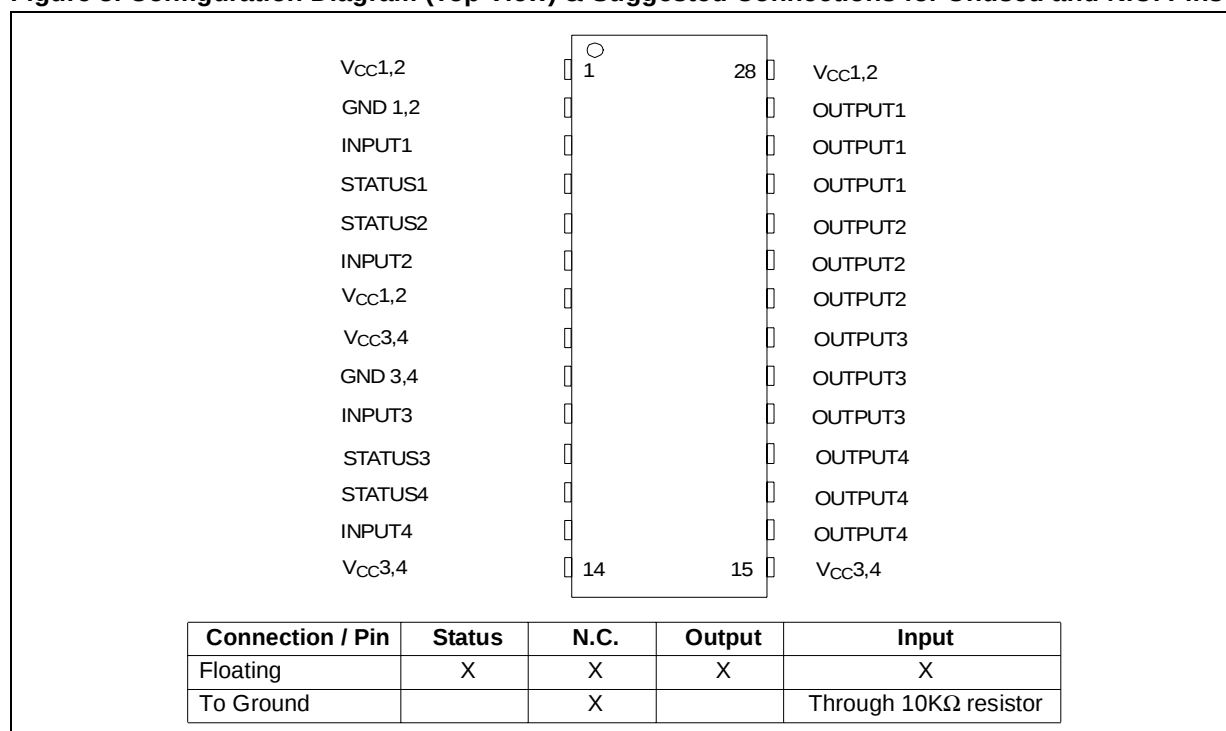
Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins

Figure 4. Current and Voltage Conventions

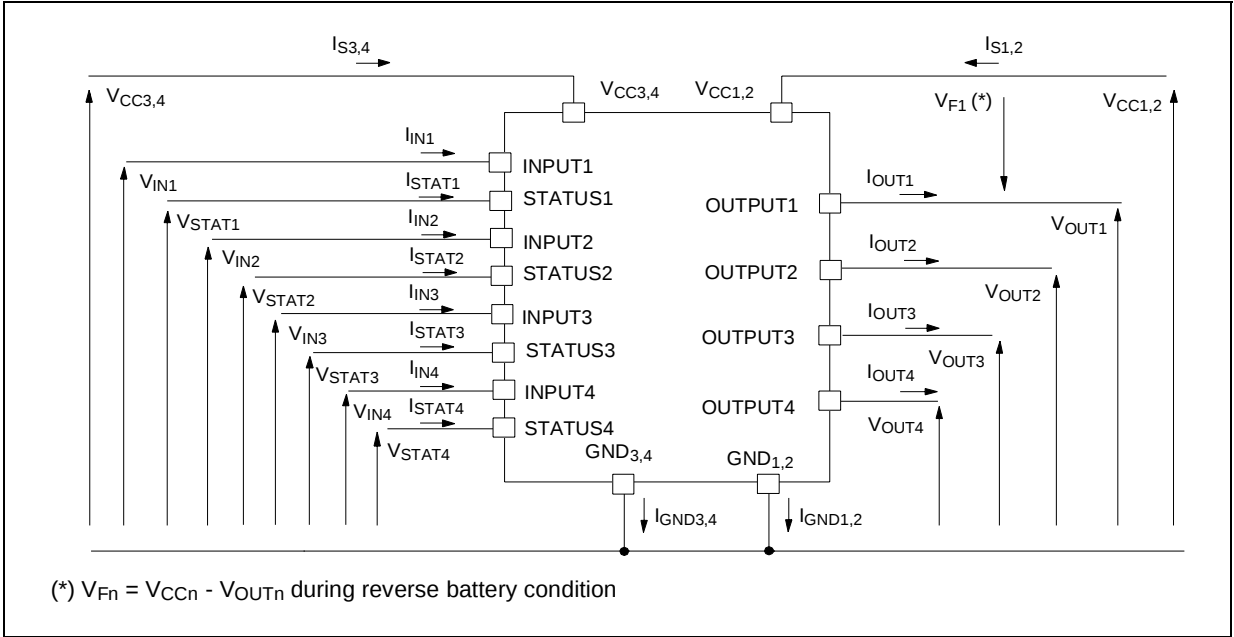


Table 4. Thermal Data (Per island)

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX)	15	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (one chip ON) (MAX)	60 ⁽¹⁾	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (two chips ON) (MAX)	46 ⁽¹⁾	°C/W

Note: 1. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

Note: 2. When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS ($8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$ unless otherwise specified)**Table 5. Power Outputs** (Per each channel)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CC}^{(**)}$	Operating Supply Voltage		5.5	13	36	V
$V_{USD}^{(**)}$	Undervoltage Shut-down		3	4	5.5	V
$V_{OV}^{(**)}$	Overvoltage Shut-down		36			V
R_{on}	On State Resistance	$I_{OUT}=2A$; $T_j=25^{\circ}C$ $I_{OUT}=2A$; $V_{CC}>8V$			65 130	$m\Omega$ $m\Omega$
$I_S^{(**)}$	Supply Current	Off State; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$ Off State; $V_{CC}=13V$; $V_{IN}=V_{OUT}=0V$; $T_j=25^{\circ}C$ On State; $V_{CC}=13V$; $V_{IN}=5V$; $I_{OUT}=0A$		12 12 5	40 25 7	μA μA mA
$I_{L(off1)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$	0		50	μA
$I_{L(off2)}$	Off State Output Current	$V_{IN}=0V$; $V_{OUT}=3.5V$	-75		0	μA
$I_{L(off3)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=125^{\circ}C$			5	μA
$I_{L(off4)}$	Off State Output Current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=25^{\circ}C$			3	μA

Note: (**) Per island.

Table 6. Switching (Per each channel) ($V_{CC}=13V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$R_L=6.5\Omega$ from V_{IN} rising edge to $V_{OUT}=1.3V$		30		μs
$t_{d(off)}$	Turn-off Delay Time	$R_L=6.5\Omega$ from V_{IN} falling edge to $V_{OUT}=11.7V$		30		μs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	$R_L=6.5\Omega$ from $V_{OUT}=1.3V$ to $V_{OUT}=10.4V$		See relative diagram		V/ μs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	$R_L=6.5\Omega$ from $V_{OUT}=11.7V$ to $V_{OUT}=1.3V$		See relative diagram		V/ μs

Table 7. V_{CC} - Output Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward on Voltage	$-I_{OUT}=1.2A$; $T_j=150^{\circ}C$			0.6	V

ELECTRICAL CHARACTERISTICS (continued)**Table 8. Logic Input** (Per each channel)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	$V_{IN}=1.25V$	1			μA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	$V_{IN}=3.25V$			10	μA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	$I_{IN}=1mA$	6	6.8	8	V
		$I_{IN}=-1mA$		-0.7		V

Table 9. Status Pin (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	$I_{STAT}=1.6mA$			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; $V_{STAT}=5V$			10	μA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; $V_{STAT}=5V$			100	pF
V_{SCL}	Status Clamp Voltage	$I_{STAT}=1mA$	6	6.8	8	V
		$I_{STAT}=-1mA$		-0.7		V

Table 10. Protections (Per each channel) (See note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^{\circ}C$
T_R	Reset Temperature		135			$^{\circ}C$
T_{hyst}	Thermal Hysteresis		7	15		$^{\circ}C$
t_{SDL}	Status Delay in Overload Conditions	$T_J > T_{TSD}$			20	μs
I_{lim}	Current limitation	$5.5V < V_{CC} < 36V$	6	9	15	A
					15	A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT}=2A$; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V

Note: 3. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 11. Openload Detection (Per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	$V_{IN}=5V$	50	100	200	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT}=0A$			200	μs
V_{OL}	Openload OFF State Voltage Detection Threshold	$V_{IN}=0V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	μs

Figure 5.

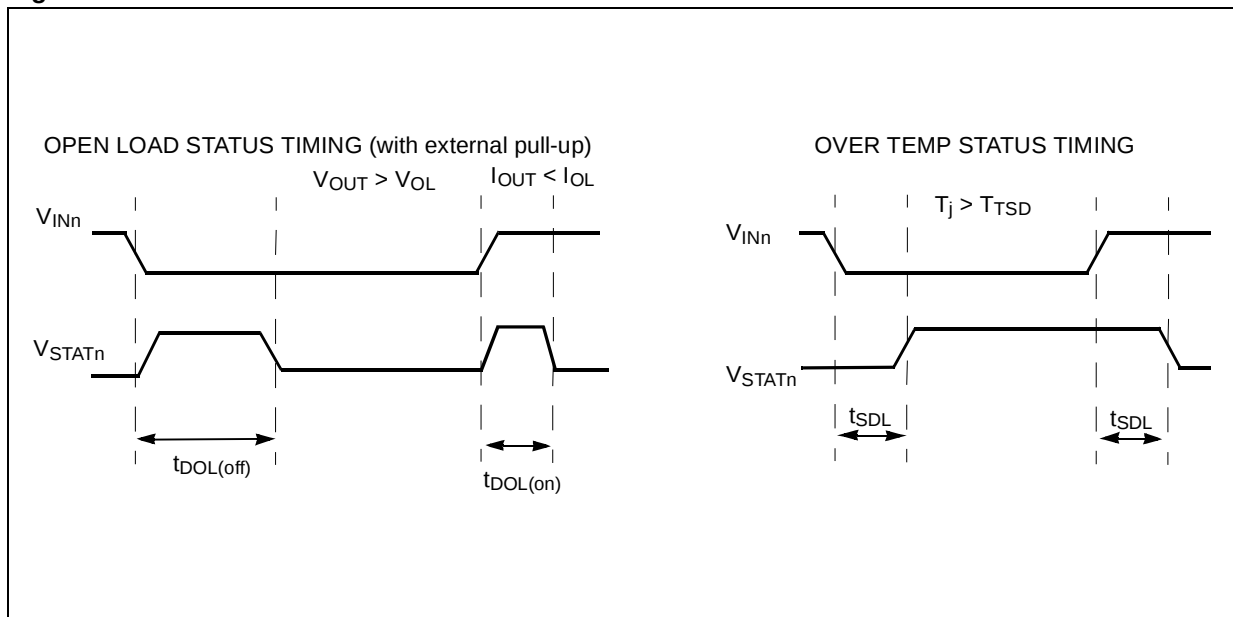


Figure 6. Switching time Waveforms

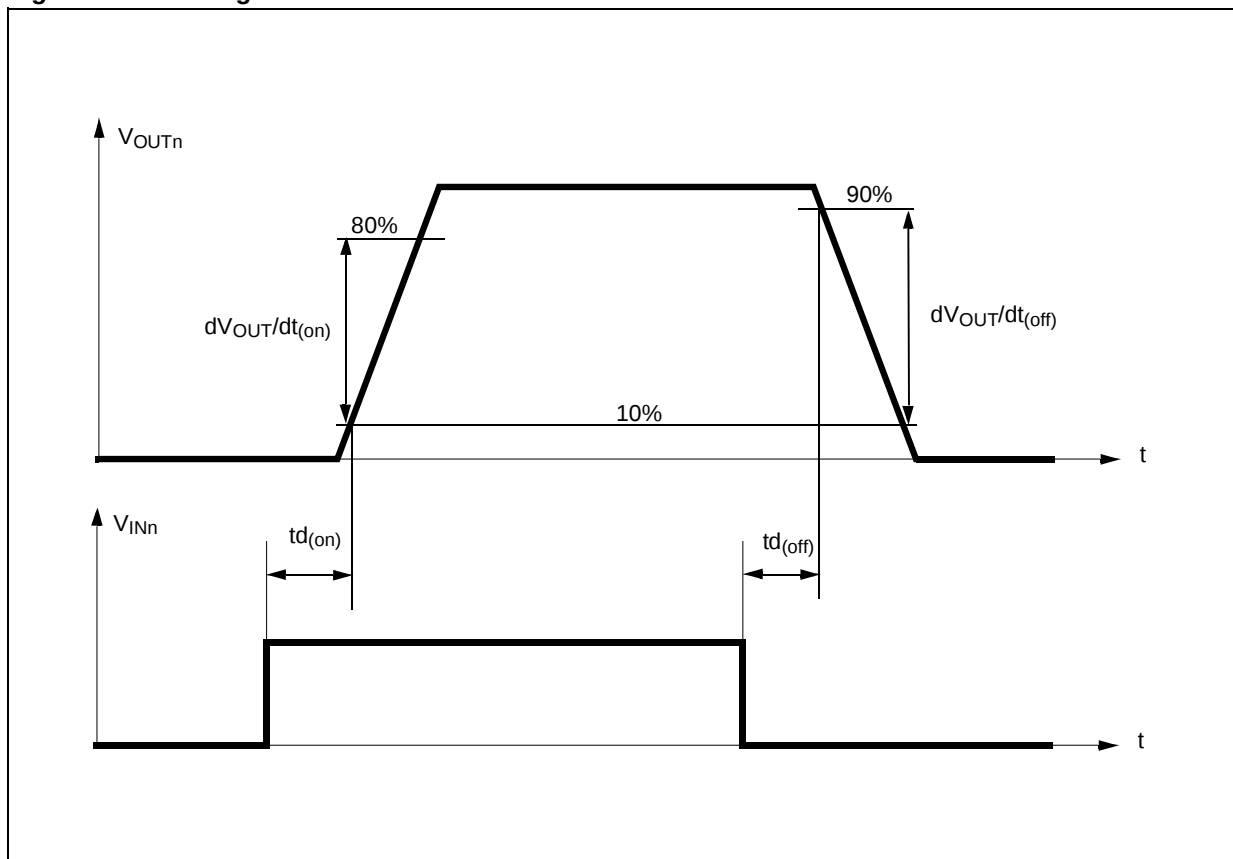


Table 12. Truth Table

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > V_{OL}	L H	H H	L H
Output Current < I_{OL}	L H	L H	H L

Table 13. Electrical Transient Requirements on V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

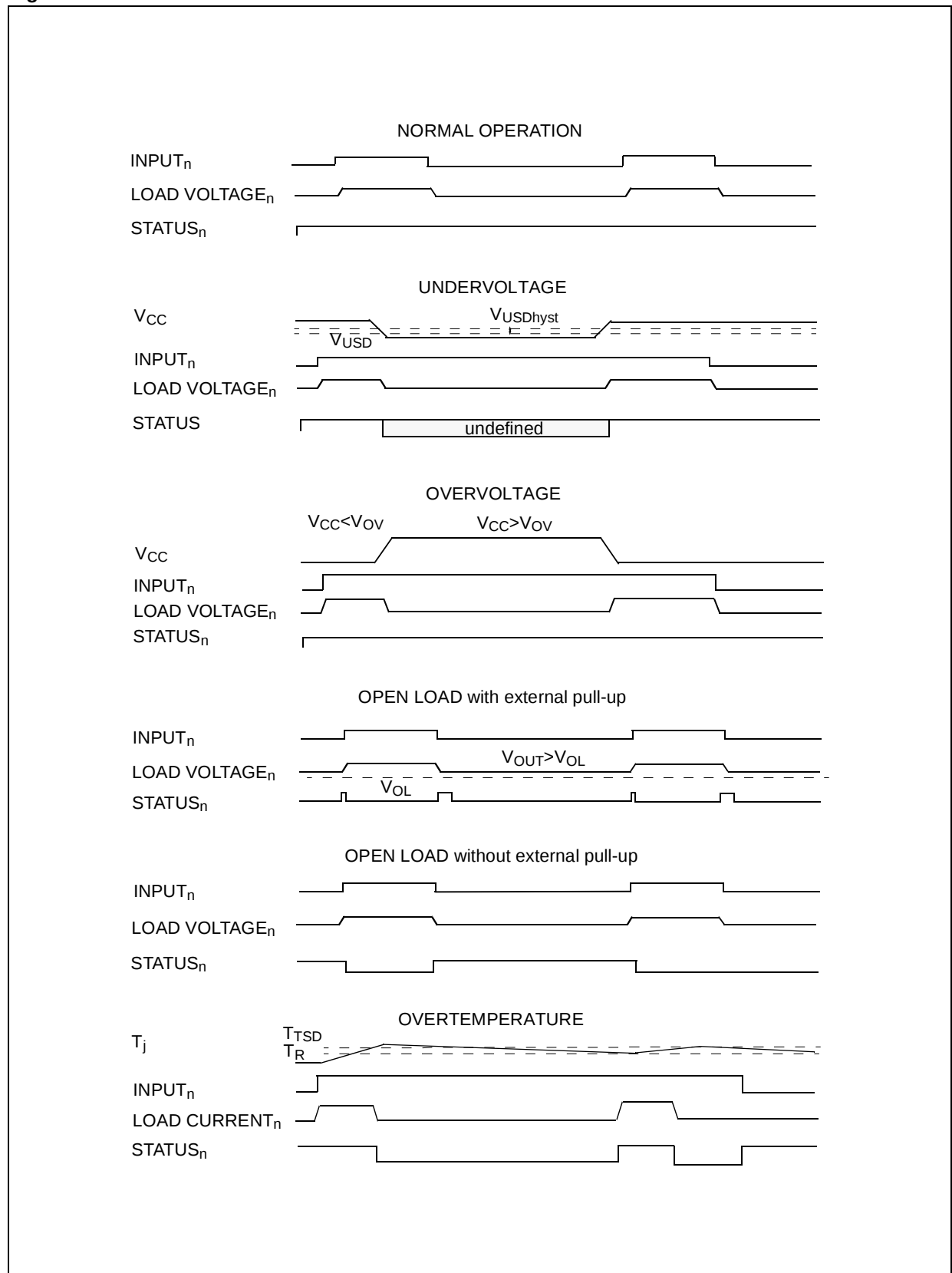
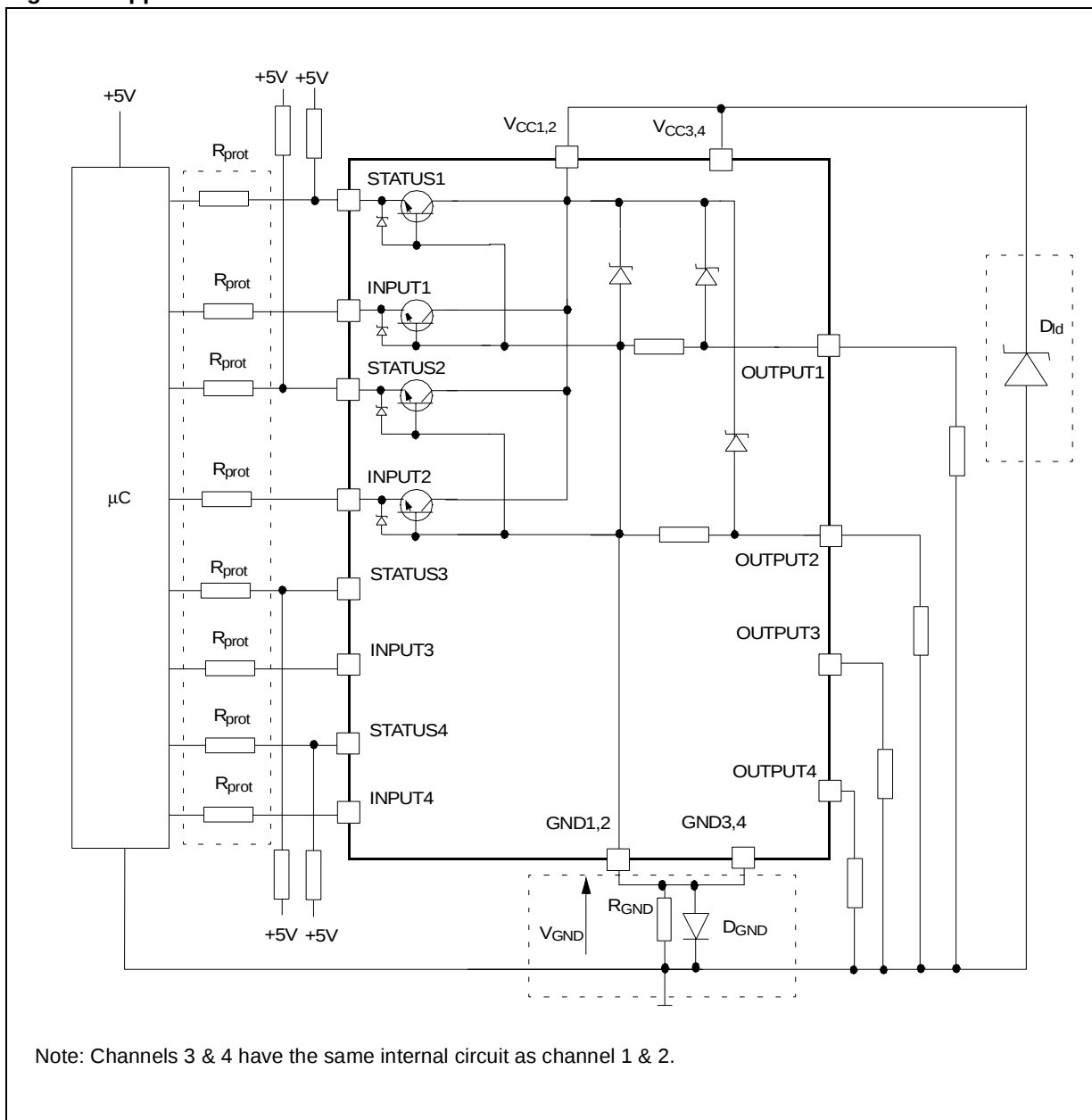


Figure 8. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / 2(I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2.

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -100V and I_{latchup} ≥ 20mA; V_{OHμC} ≥ 4.5V
5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended R_{prot} value is 10kΩ.

OPEN LOAD DETECTION IN OFF STATE

Off state open load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

- 1) no false open load indication when load is connected:
in this case we have to avoid V_{OUT} to be higher than V_{OLmin}; this results in the following condition
 $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$.
- 2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$.

Because I_{S(OFF)} may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

The values of V_{OLmin}, V_{OLmax} and I_{L(off2)} are available in the Electrical Characteristics section.

Figure 9. Open Load detection in off state

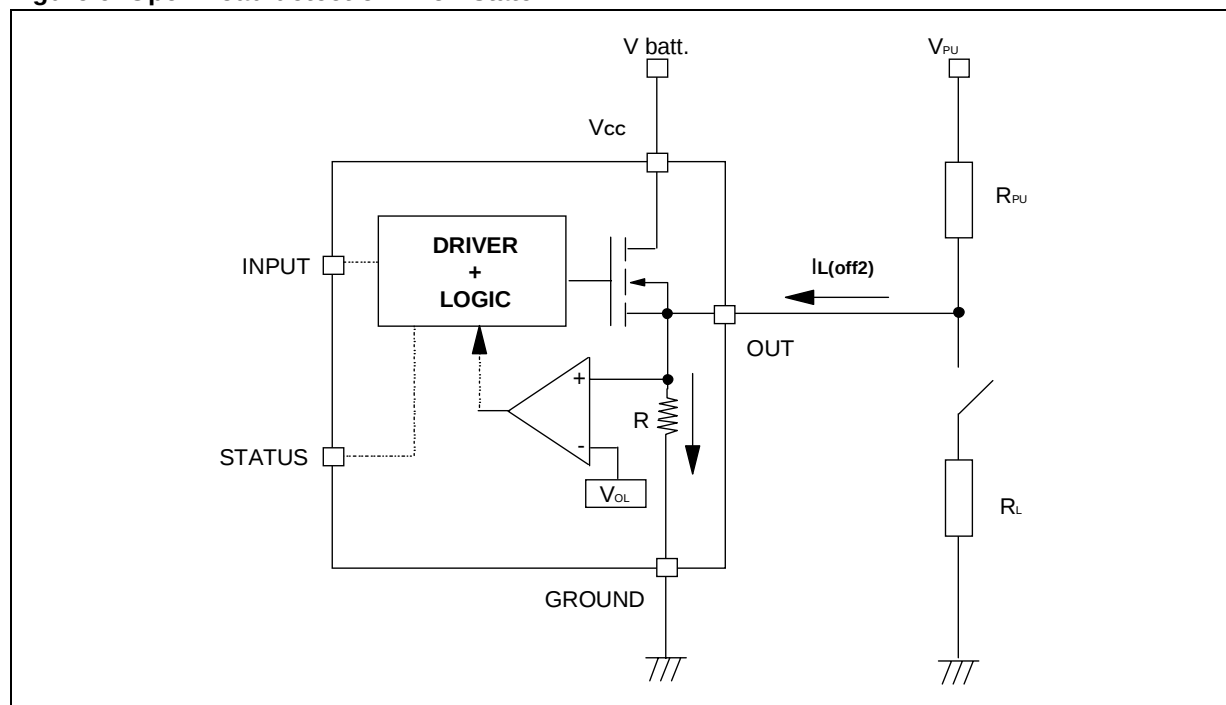


Figure 10. Off State Output Current

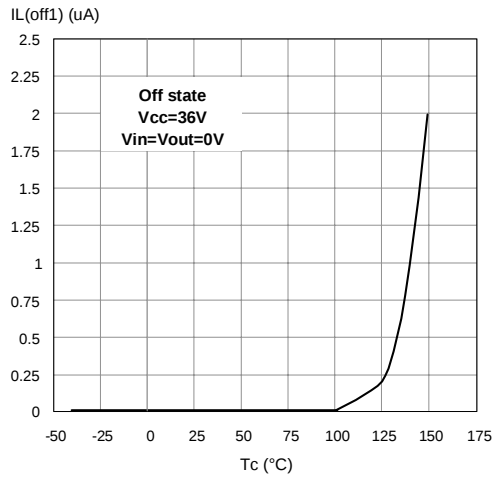


Figure 11. High Level Input Current

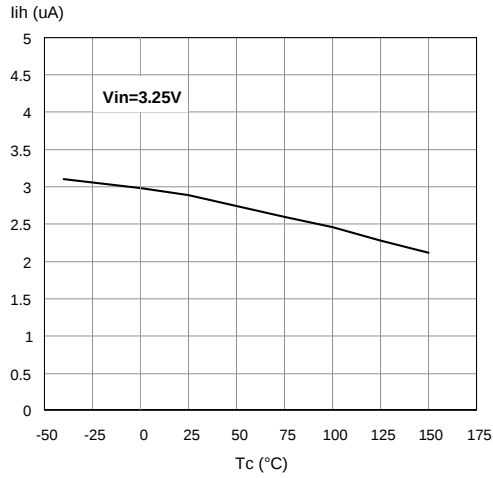


Figure 12. Input Clamp Voltage

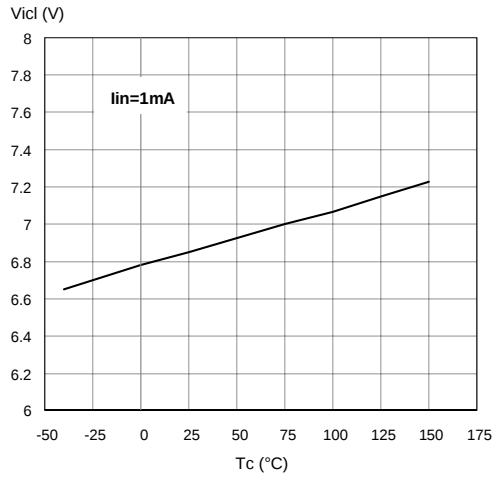


Figure 14. Status Level Voltage

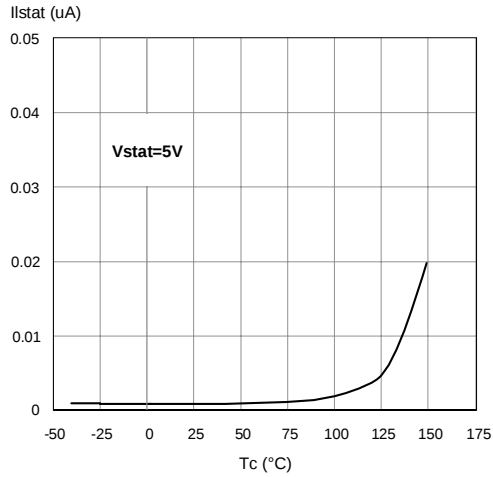


Figure 13. Status Low Output Voltage

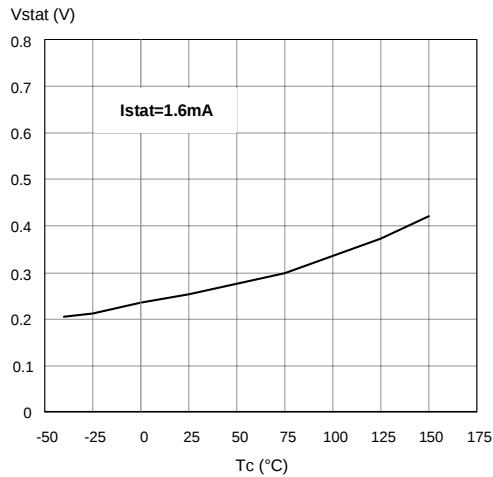


Figure 15. Status Clamp Voltage

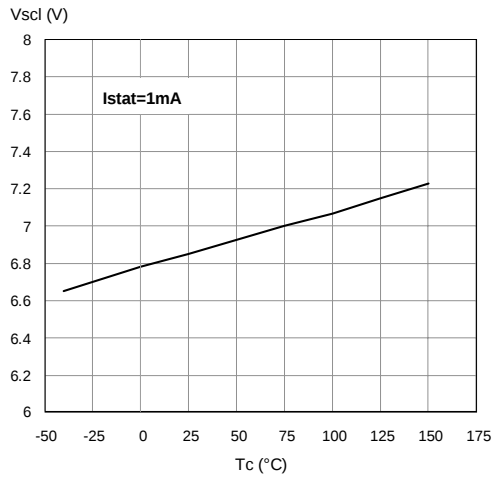


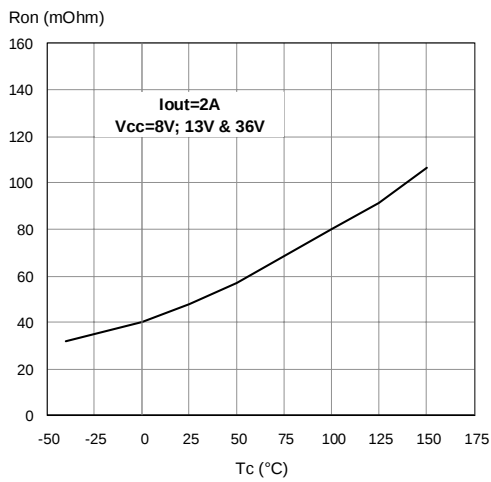
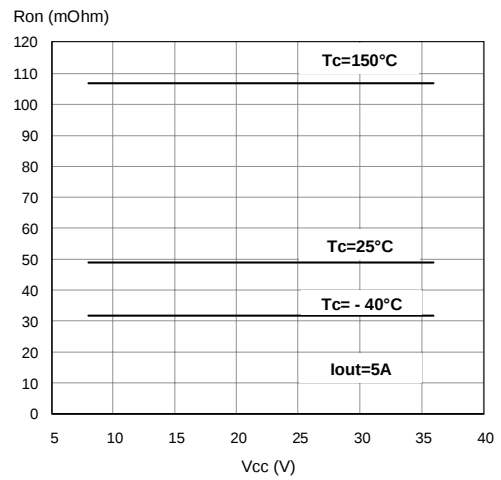
Figure 16. On State Resistance Vs T_{case} Figure 17. On State Resistance Vs V_{CC} 

Figure 18. Openload On State Detection Threshold

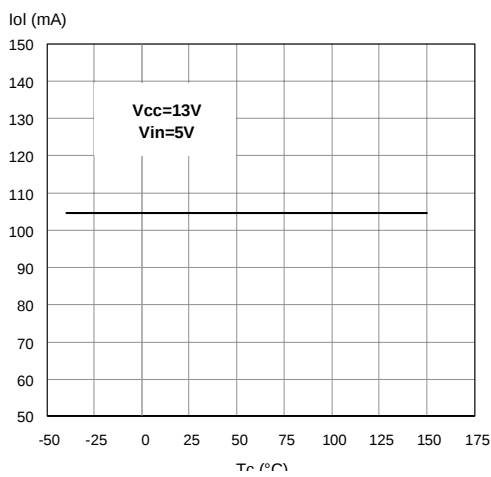


Figure 20. Openload Off State Voltage Detection Threshold

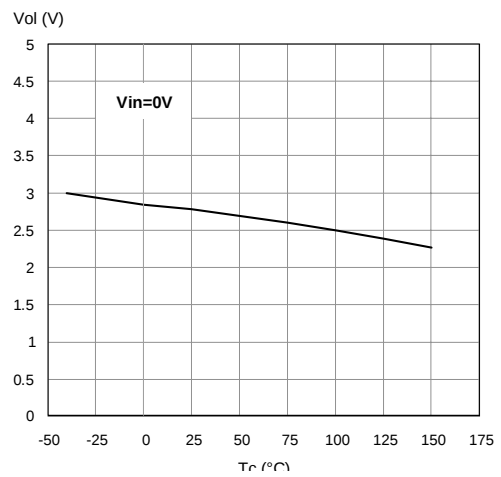


Figure 19. Input High Level

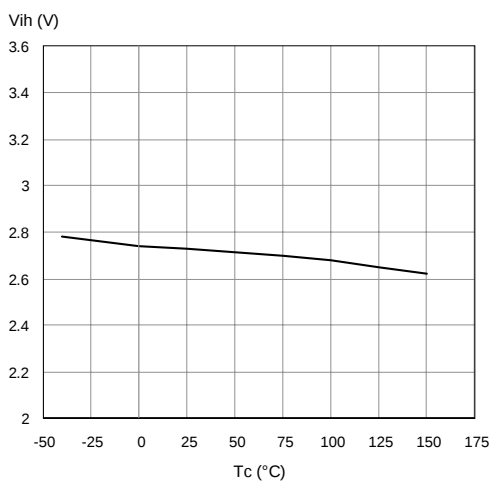


Figure 21. Input Low Level

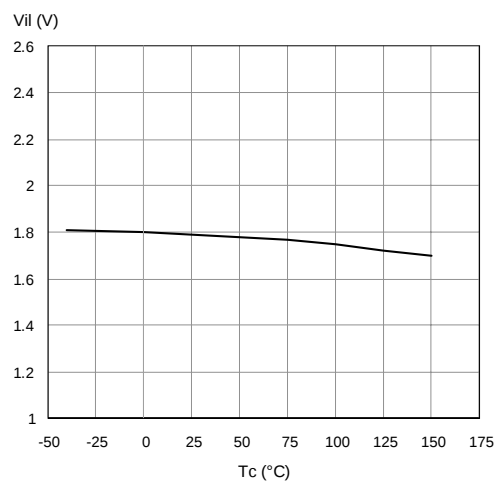


Figure 22. Turn-on Voltage Slope

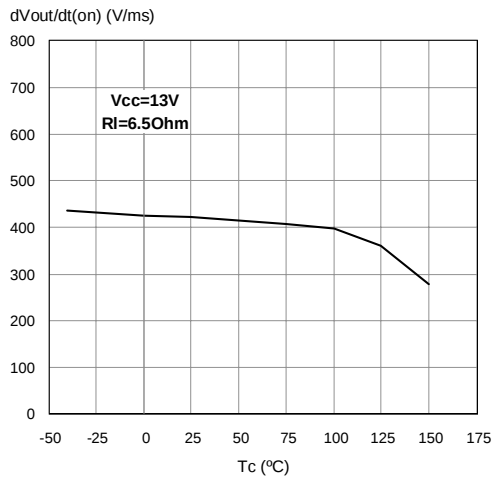


Figure 25. Turn-off Voltage Slope

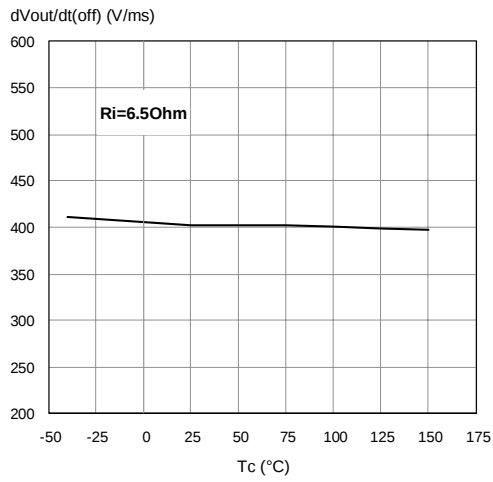


Figure 23. Overvoltage Shutdown

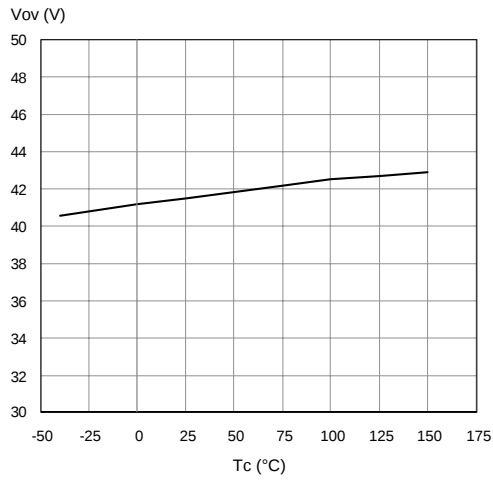


Figure 26. I_{LIM} Vs T_{case}

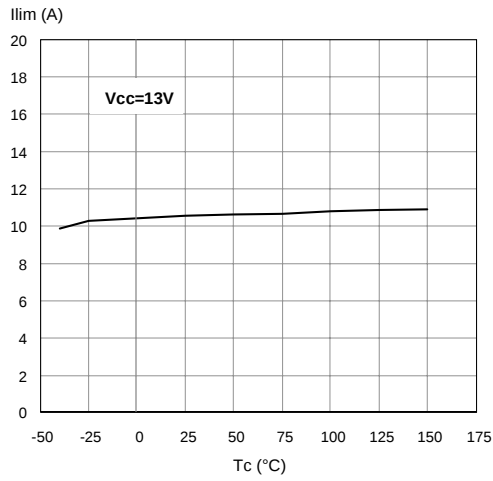


Figure 24. Input Hysteresis Voltage

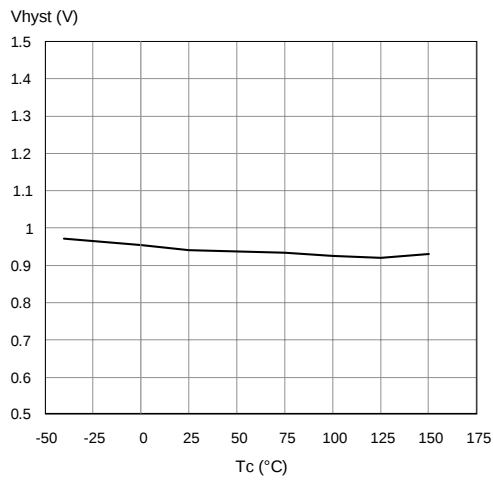
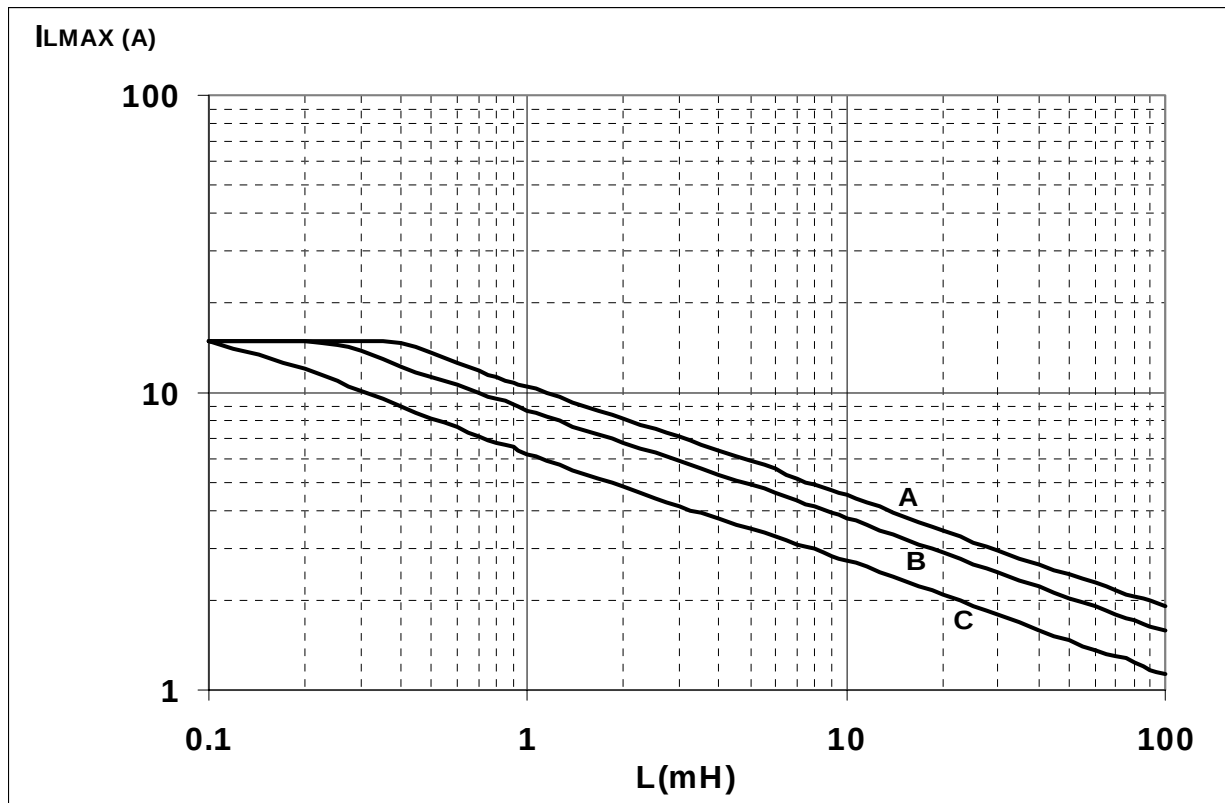


Figure 27. Maximum turn off current versus load inductance



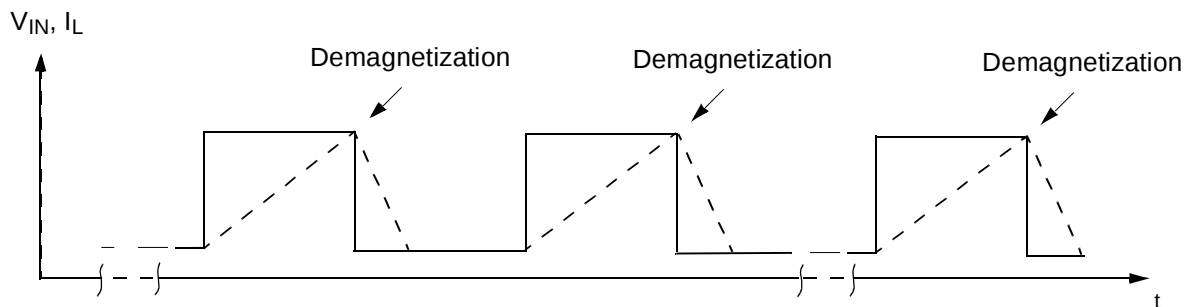
A = Single Pulse at $T_{Jstart}=150^{\circ}C$
 B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
 C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$



SO-28 Thermal Data

Figure 28. SO-28 DOUBLE ISLAND PC Board

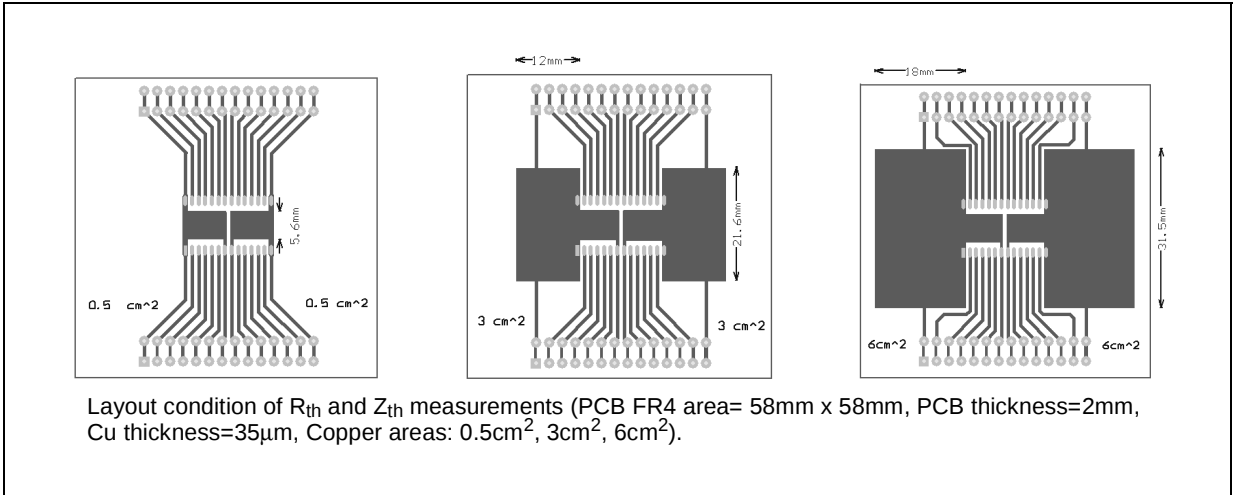


Table 14. Thermal calculation according to the PCB heatsink area

Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1}=P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

Note: R_{thA} = Thermal resistance Junction to Ambient with one chip ON

Note: R_{thB} = Thermal resistance Junction to Ambient with both chips ON and $P_{dchip1}=P_{dchip2}$

Note: R_{thC} = Mutual thermal resistance

Figure 29. $R_{thj-amb}$ Vs PCB copper area in open box free air condition

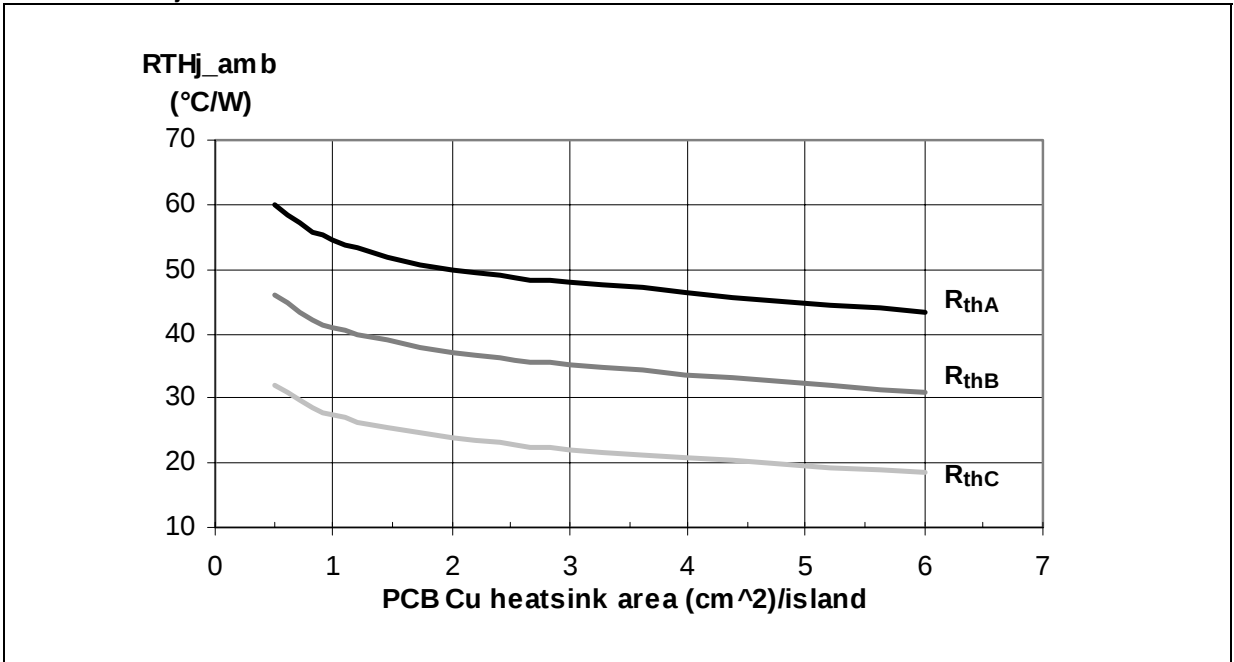


Figure 30. SO-28 Thermal Impedance Junction Ambient Single Pulse

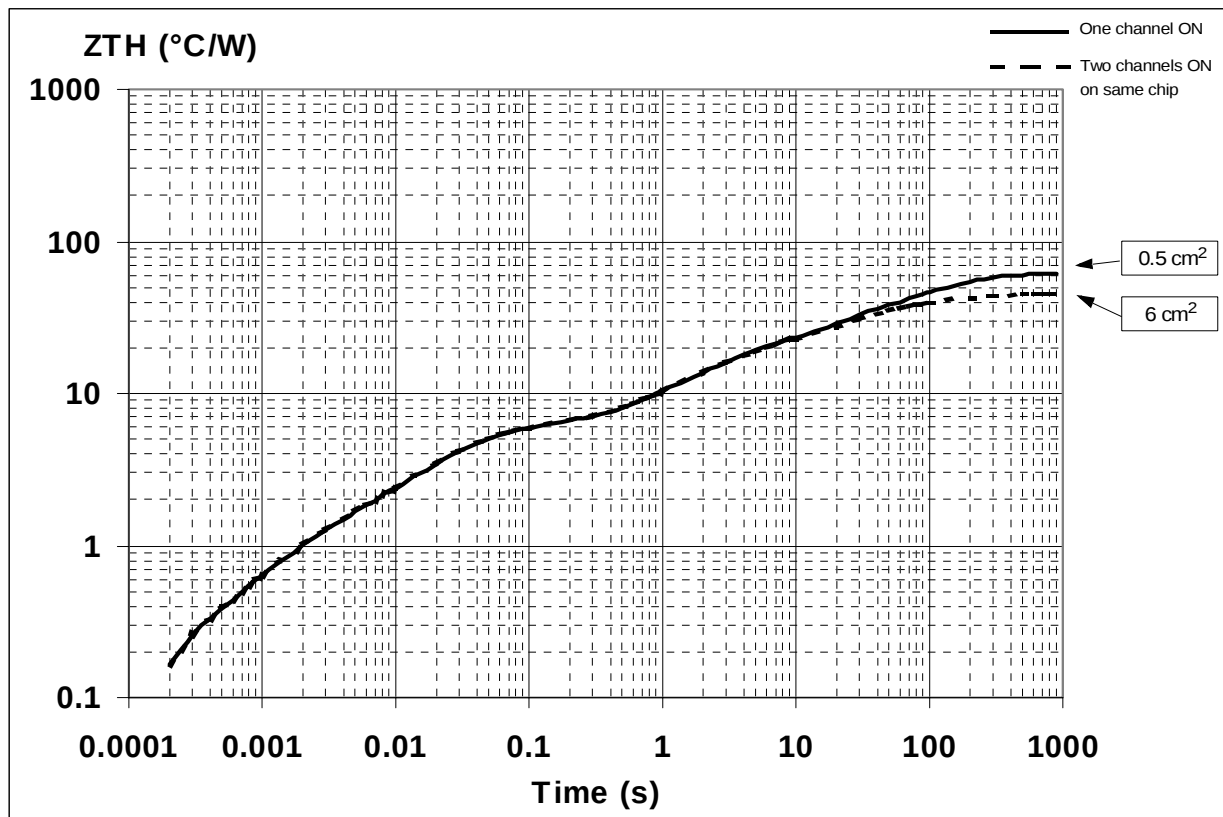
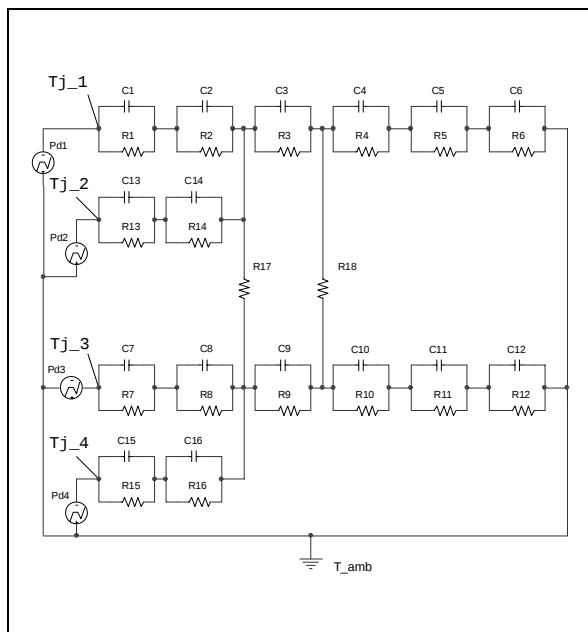


Figure 31. Thermal fitting model of a quad channels HSD in SO-28



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

$$\text{where } \delta = t_p / T$$

Table 15. Thermal Parameter

Area/island (cm²)	0.5	6
R1=R7=R13=R15 (°C/W)	0.15	
R2=R8=R14=R16 (°C/W)	0.8	
R3=R9 (°C/W)	4.5	
R4=R10 (°C/W)	11	
R5=R11 (°C/W)	15	
R6=R12 (°C/W)	5	13
C1=C7=C13=C15 (W.s/°C)	0.0006	
C2=C8=C14=C16 (W.s/°C)	2.10E-03	
C3=C9 (W.s/°C)	6.00E-03	
C4=C10 (W.s/°C)	0.2	
C5=C11 (W.s/°C)	1.5	
C6=C12 (W.s/°C)	5	8
R17=R18 (°C/W)	150	

PACKAGE MECHANICAL

Table 16. SO-28 Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A			2.65
a1	0.10		0.30
b	0.35		0.49
b1	0.23		0.32
C		0.50	
c1	45 (typ.)		
D	17.7		18.1
E	10.00		10.65
e		1.27	
e3		16.51	
F	7.40		7.60
L	0.40		1.27
S	8 (max.)		

Figure 32. SO-28 Package Dimensions

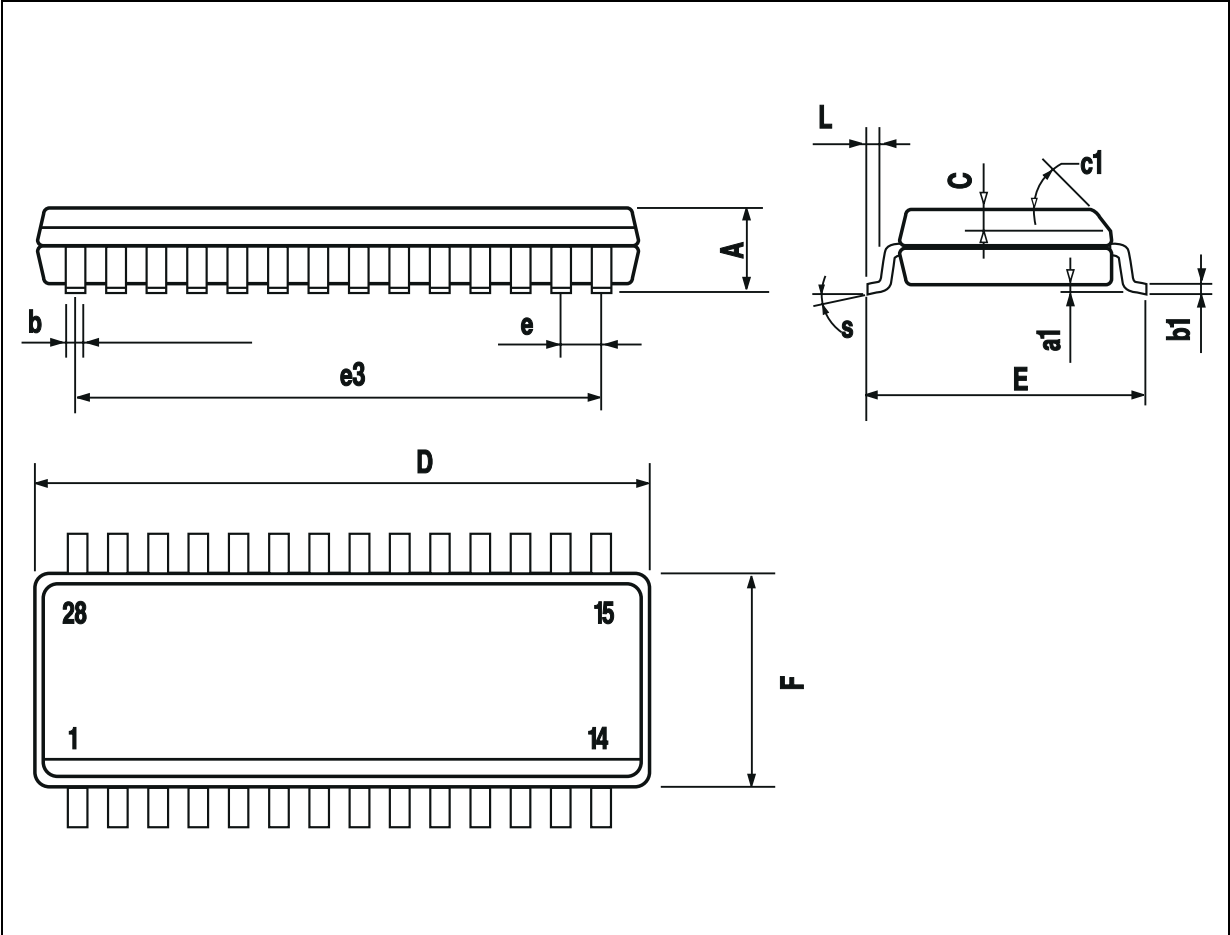


Figure 33. SO-28 TUBE SHIPMENT (no suffix)

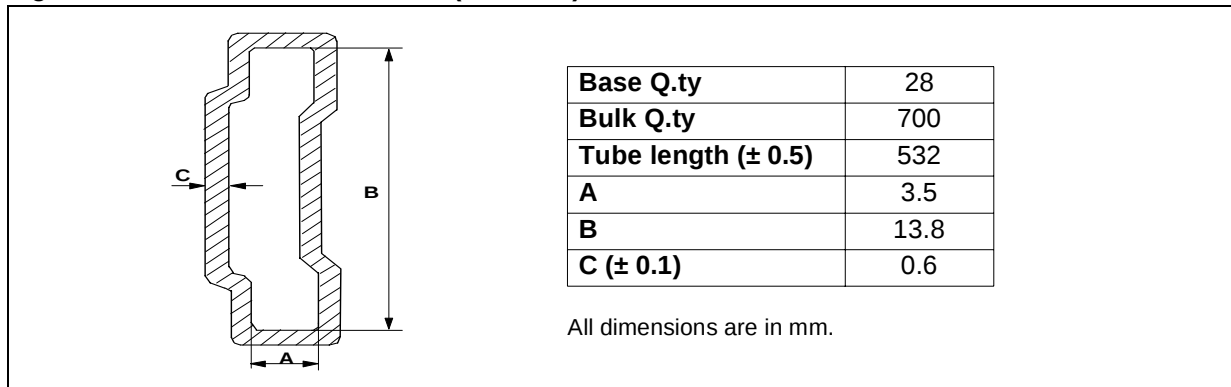
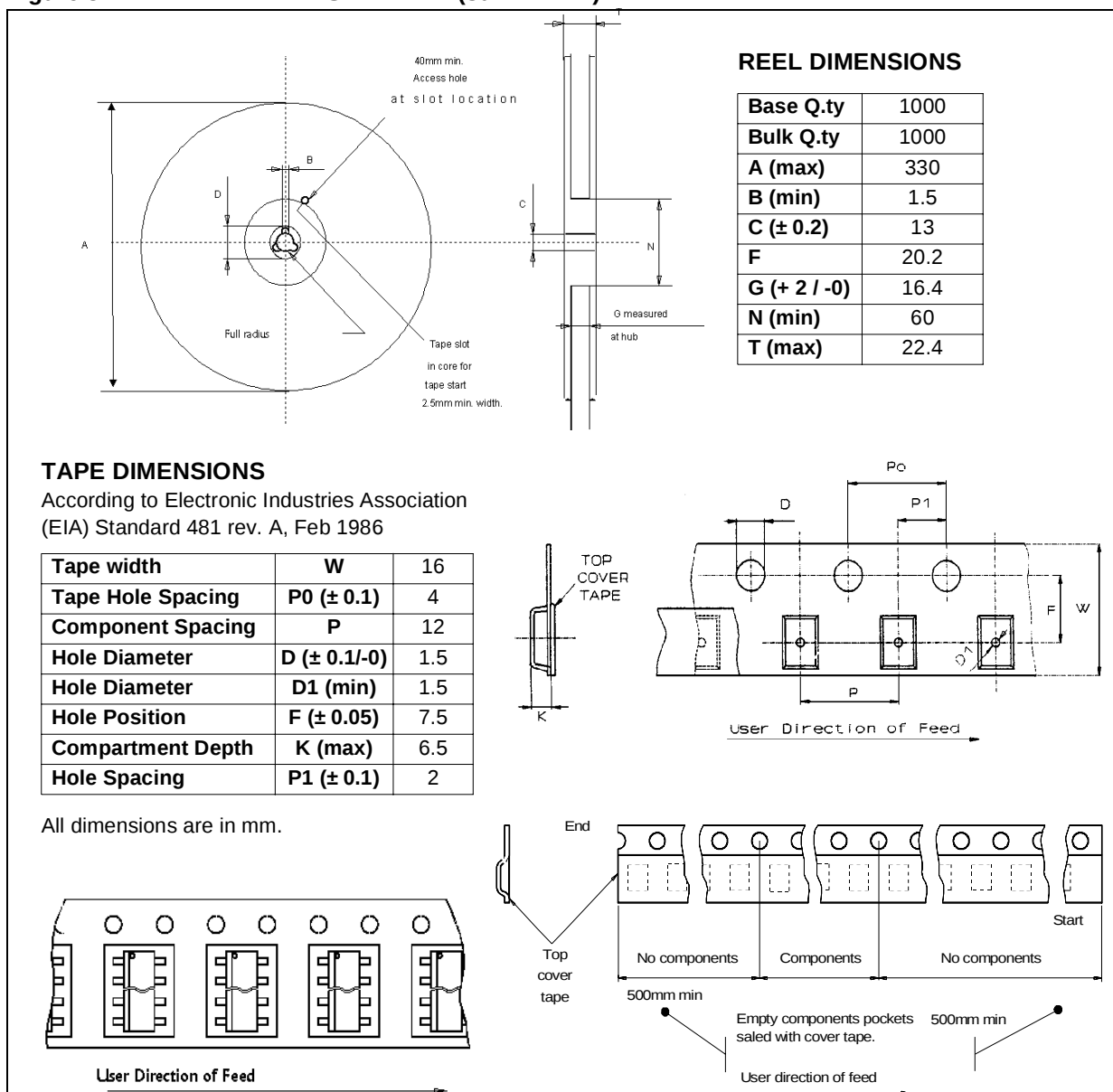


Figure 34. TAPE AND REEL SHIPMENT (suffix "TR")



REVISION HISTORY

Table 17. Revision History

Date	Revision	Description of Changes
Oct. 2004	1	First issue.

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