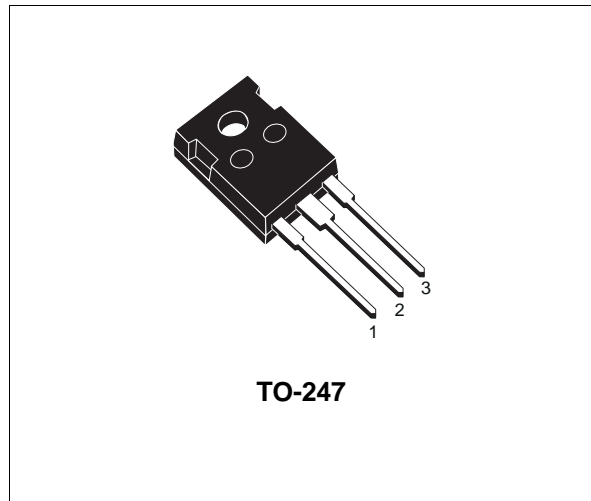


**"OMNIFET":
FULLY AUTOPROTECTED POWER MOSFET**

PRELIMINARY DATA

TYPE	V _{clamp}	R _{DS(on)}	I _{lim}
VNW100N04	42 V	0.012 Ω	100 A

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET
- STANDARD TO-247 PACKAGE



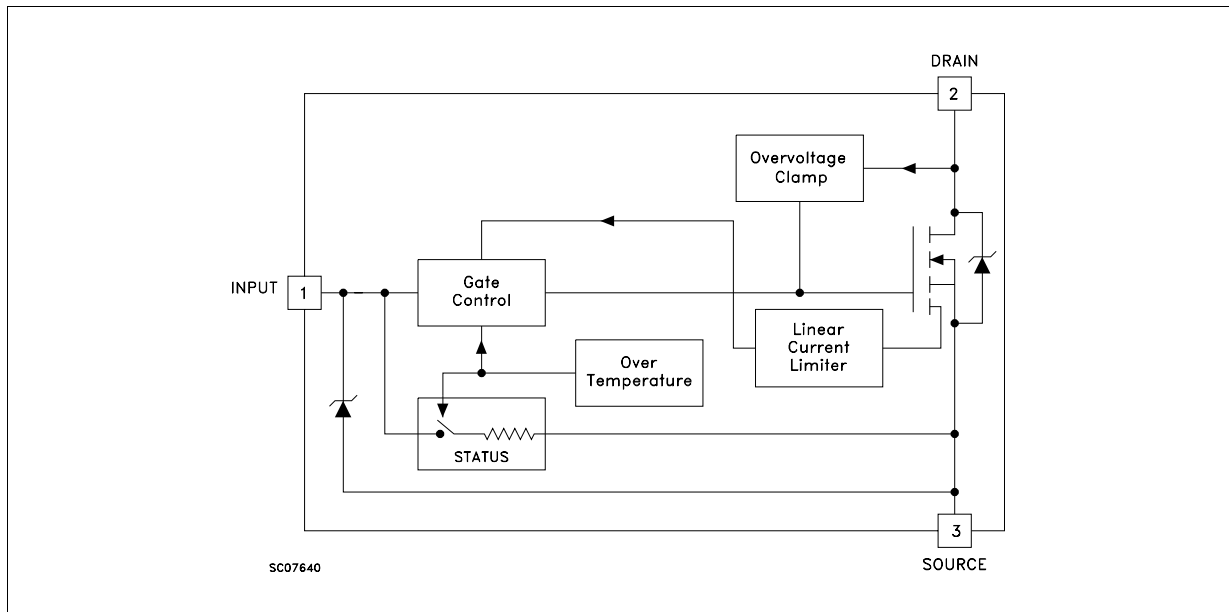
DESCRIPTION

The VNW100N04 is a monolithic device made using SGS-THOMSON Vertical Intelligent Power M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear

current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{in} = 0)	Internally Clamped	V
V _{in}	Input Voltage	18	V
I _D	Drain Current	Internally Limited	A
I _R	Reverse DC Output Current	-100	A
V _{esd}	Electrostatic Discharge (C= 100 pF, R=1.5 KΩ)	2000	V
P _{tot}	Total Dissipation at T _c = 25 °C	208	W
T _j	Operating Junction Temperature	Internally Limited	°C
T _c	Case Operating Temperature	Internally Limited	°C
T _{stg}	Storage Temperature	-55 to 150	°C

THERMAL DATA

R _{thj-case}	Thermal Resistance Junction-case	Max	0.6	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	30	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{CLAMP}	Drain-source Clamp Voltage	I _D = 50 A V _{in} = 0	36	42	48	V
V _{CLTH}	Drain-source Clamp Threshold Voltage	I _D = 2 mA V _{in} = 0	35			V
V _{INCL}	Input-Source Reverse Clamp Voltage	I _{in} = -1 mA	-1		-0.3	V
I _{DSS}	Zero Input Voltage Drain Current (V _{in} = 0)	V _{DS} = 13 V V _{in} = 0 V _{DS} = 25 V V _{in} = 0			50 200	μA μA
I _{ISS}	Supply Current from Input Pin	V _{DS} = 0 V V _{in} = 10 V		250	500	μA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{IN(th)}	Input Threshold Voltage	V _{DS} = V _{in} I _D + I _{in} = 1 mA	0.8		3	V
R _{DS(on)}	Static Drain-source On Resistance	V _{in} = 10 V I _D = 50 A V _{in} = 5 V I _D = 50 A			0.012 0.015	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 13 V I _D = 50 A	40	60		S
C _{oss}	Output Capacitance	V _{DS} = 13 V f = 1 MHz V _{in} = 0		2000	3000	pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING (**)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_d = 50\text{ A}$		110	250	ns
t_r	Rise Time	$V_{gen} = 10\text{ V}$ $R_{gen} = 10\ \Omega$		500	900	ns
$t_{d(off)}$	Turn-off Delay Time	(see figure 3)		1000	1800	ns
t_f	Fall Time			600	1000	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_d = 50\text{ A}$		2.2	3.5	μs
t_r	Rise Time	$V_{gen} = 10\text{ V}$ $R_{gen} = 1000\ \Omega$		3.5	6	μs
$t_{d(off)}$	Turn-off Delay Time	(see figure 3)		22	30	μs
t_f	Fall Time			12	18	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 15\text{ V}$ $I_D = 50\text{ A}$ $V_{in} = 10\text{ V}$ $R_{gen} = 10\ \Omega$		55		A/ μs
Q_i	Total Input Charge	$V_{DD} = 15\text{ V}$ $I_D = 50\text{ A}$ $V_{in} = 10\text{ V}$		190		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 50\text{ A}$ $V_{in} = 0$			1.6	V
$t_{rr} (**)$	Reverse Recovery Time	$I_{SD} = 50\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$		800		ns
$Q_{rr} (**)$	Reverse Recovery Charge	(see test circuit, figure 5)		5		μC
$I_{RRM} (**)$	Reverse Recovery Current			15		A

PROTECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain Current Limit	$V_{in} = 10\text{ V}$ $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$ $V_{DS} = 13\text{ V}$	35 35	50 50	65 65	A A
$t_{dim} (**)$	Step Response Current Limit	$V_{in} = 10\text{ V}$ $V_{in} = 5\text{ V}$		50 130	80 200	μs μs
$T_{jsh} (**)$	Overtemperature Shutdown		170			$^\circ\text{C}$
$T_{jrs} (**)$	Overtemperature Reset		155			$^\circ\text{C}$
$I_{gf} (**)$	Fault Sink Current	$V_{in} = 10\text{ V}$ $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$ $V_{DS} = 13\text{ V}$		50 20		mA mA
$E_{as} (**)$	Single Pulse Avalanche Energy	starting $T_j = 25\text{ }^\circ\text{C}$ $V_{DD} = 20\text{ V}$ $V_{in} = 10\text{ V}$ $R_{gen} = 1\text{ K}\Omega$ $L = 10\text{ mH}$	4			J

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(**) Parameters guaranteed by design/characterization

PROTECTION FEATURES

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current (I_{ISS}) flows into the Input pin in order to supply the internal circuitry.

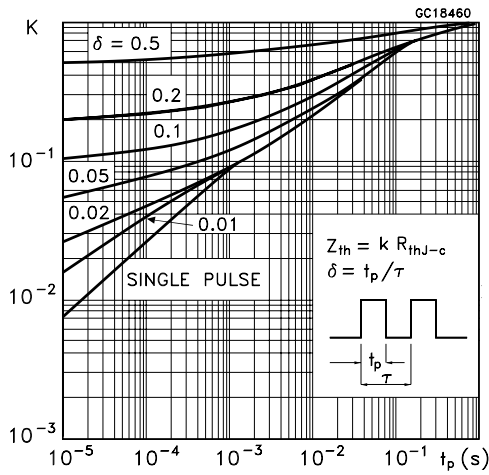
The device integrates:

- **OVERVOLTAGE CLAMP PROTECTION:** internally set at 42V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **LINEAR CURRENT LIMITER CIRCUIT:** limits the drain current I_d to I_{lim} whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

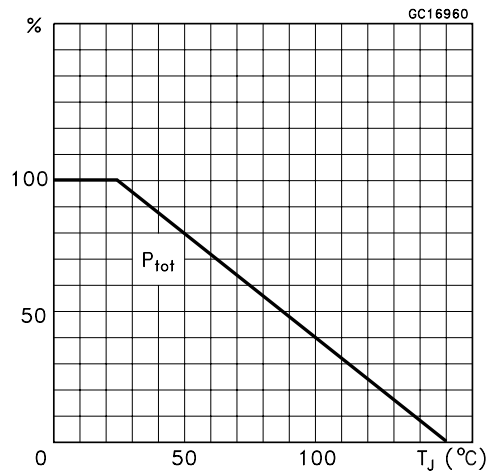
- **OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:** these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 170°C. The device is automatically restarted when the chip temperature falls below 155°C.
- **STATUS FEEDBACK:** In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω . The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

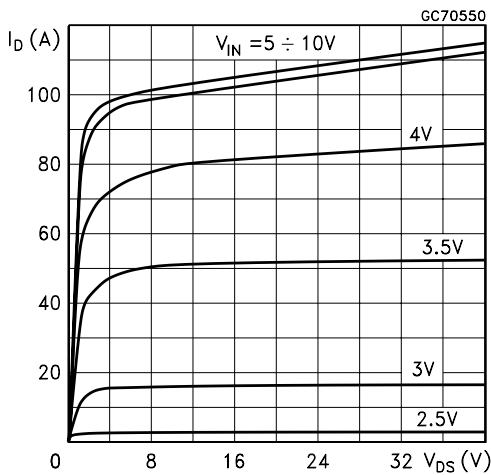
Thermal Impedance



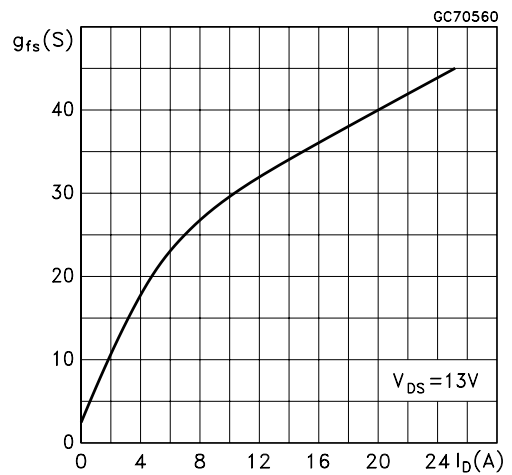
Derating Curve



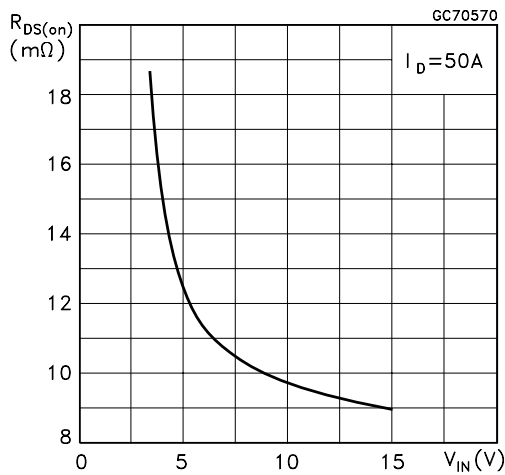
Output Characteristics



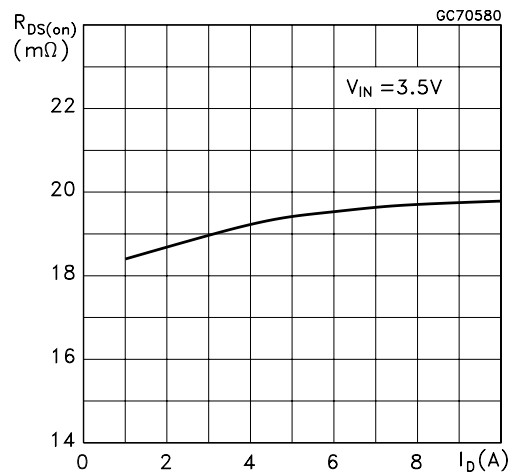
Transconductance



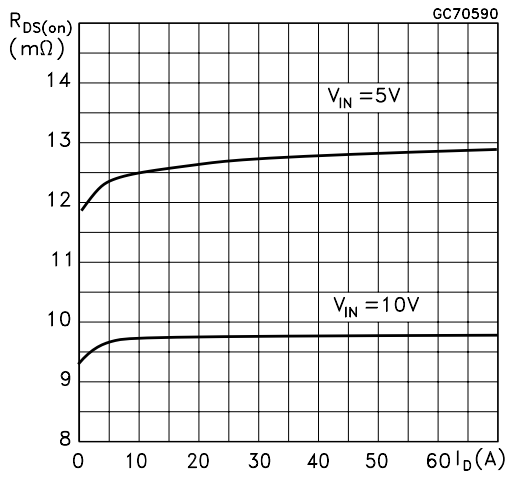
Static Drain-Source On Resistance vs Input Voltage



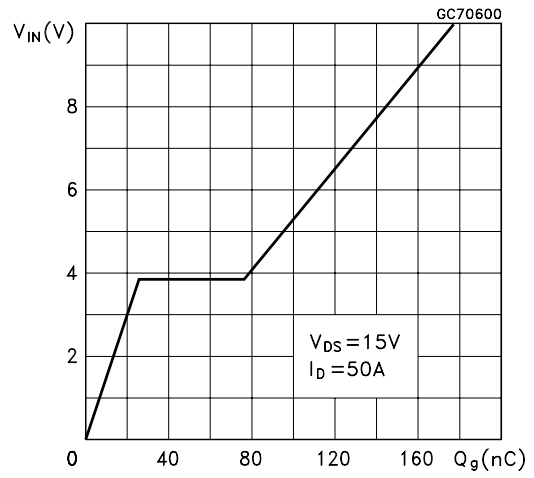
Static Drain-Source On Resistance



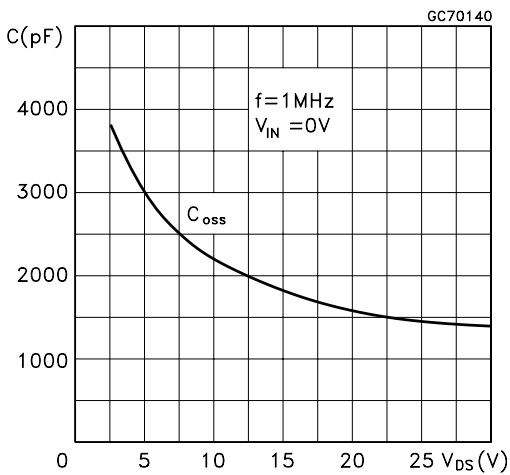
Static Drain-Source On Resistance



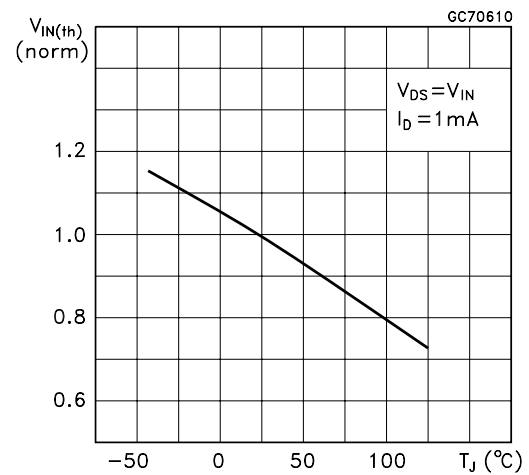
Input Charge vs Input Voltage



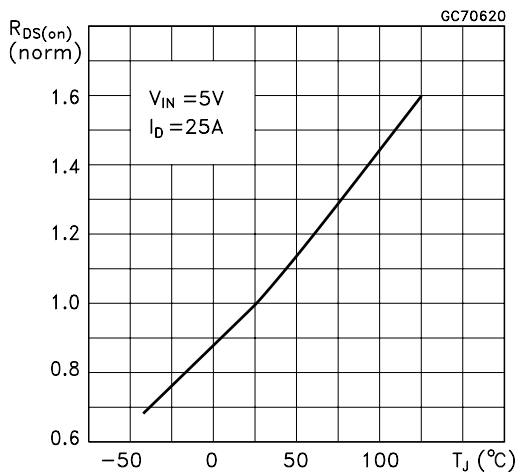
Capacitance Variations



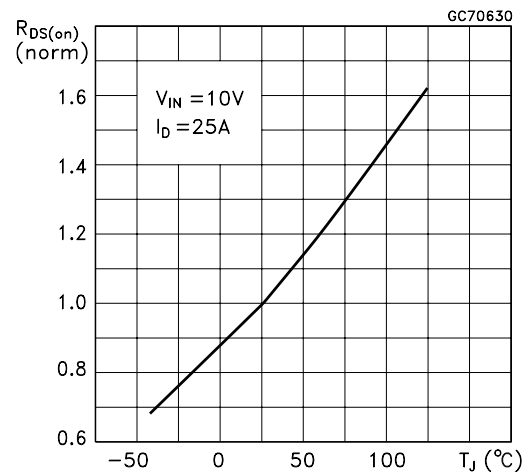
Normalized Input Threshold Voltage vs Temperature



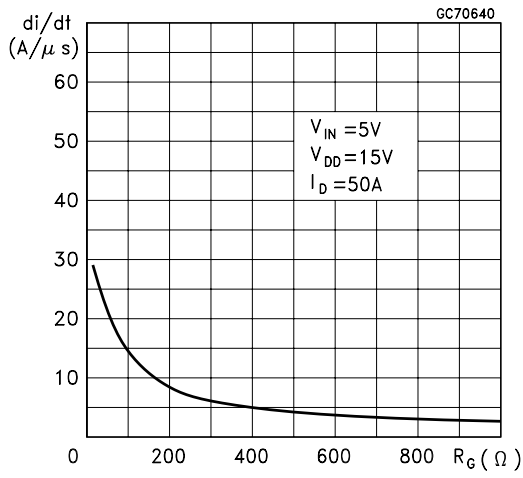
Normalized On Resistance vs Temperature



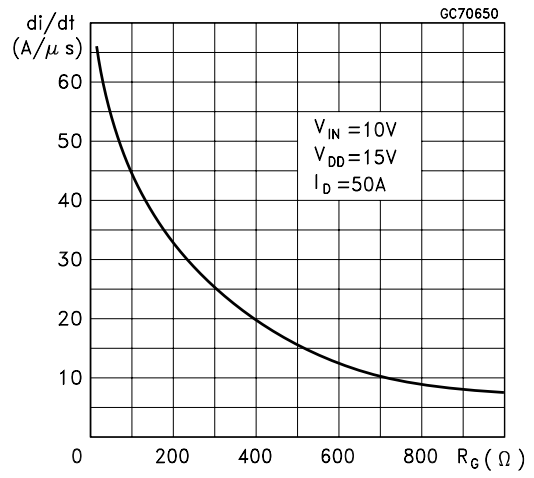
Normalized On Resistance vs Temperature



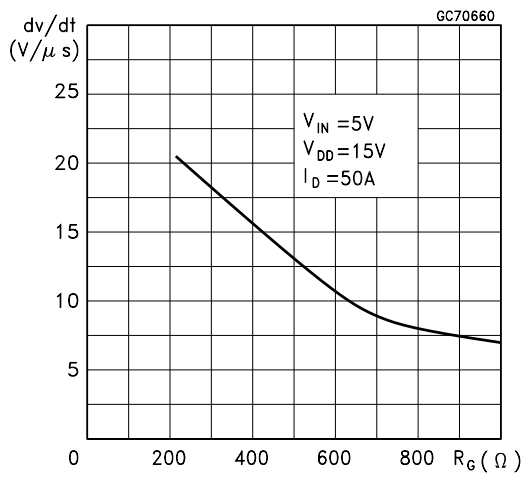
Turn-on Current Slope



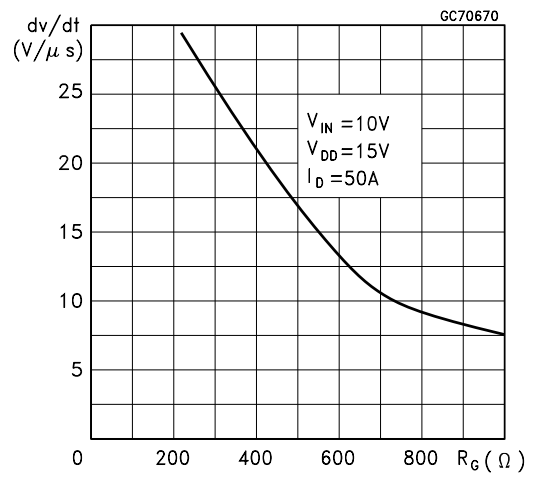
Turn-on Current Slope



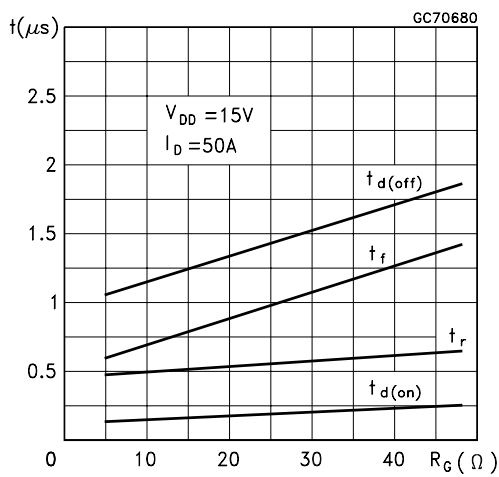
Turn-off Drain-Source Voltage Slope



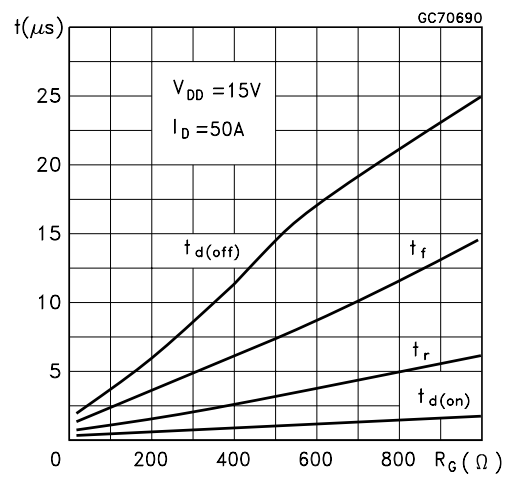
Turn-off Drain-Source Voltage Slope



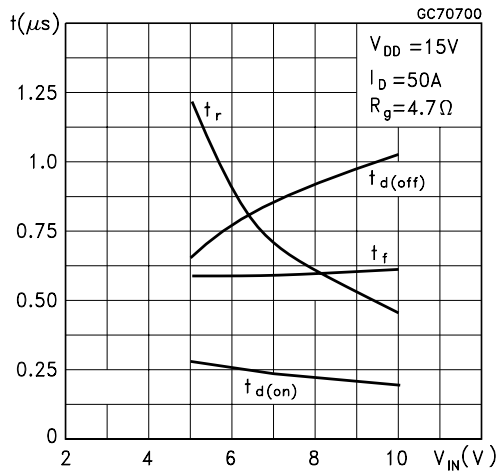
Switching Time Resistive Load



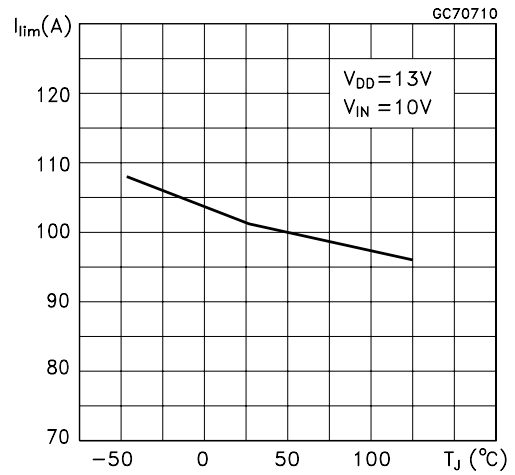
Switching Time Resistive Load



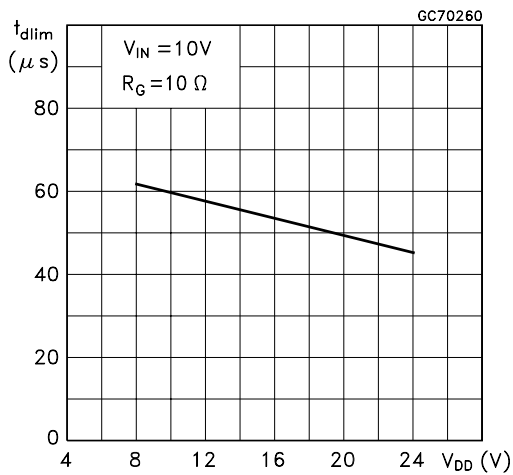
Switching Time Resistive Load



Current Limit vs Junction Temperature



Step Response Current Limit



Source Drain Diode Forward Characteristics

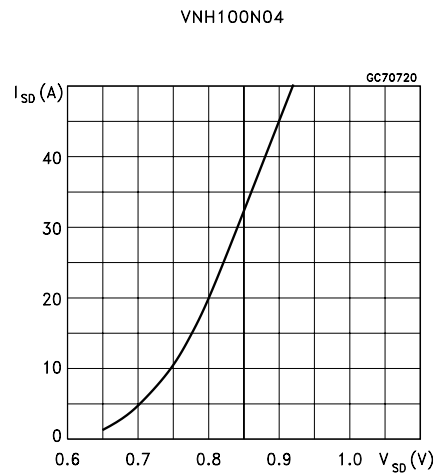


Fig. 1: Unclamped Inductive Load Test Circuits

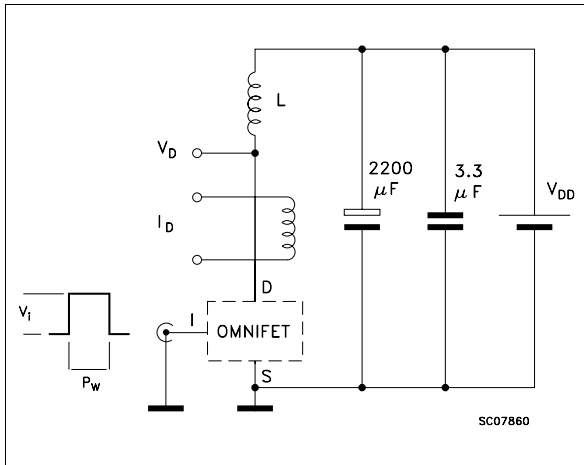


Fig. 2: Unclamped Inductive Waveforms

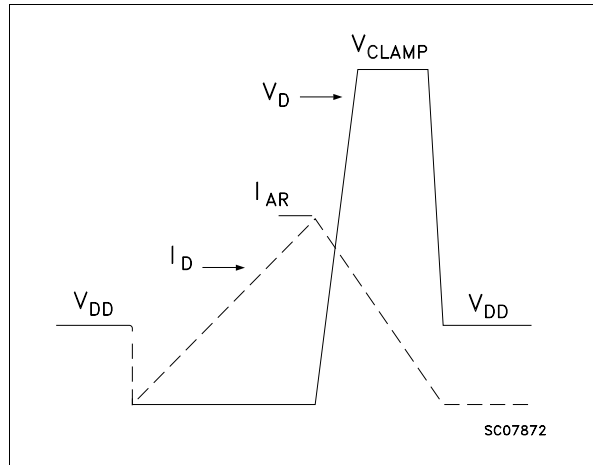


Fig. 3: Switching Times Test Circuits For Resistive Load

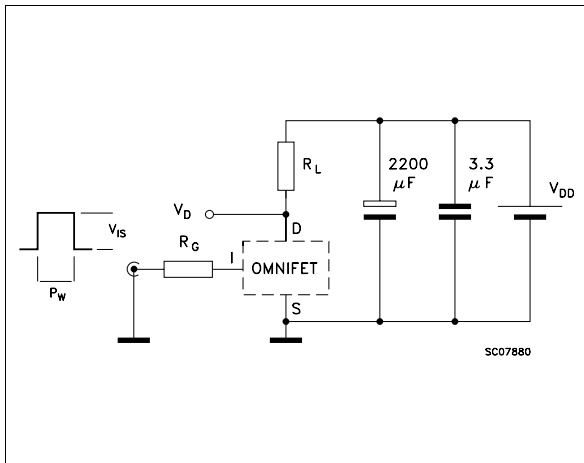


Fig. 4: Input Charge Test Circuit

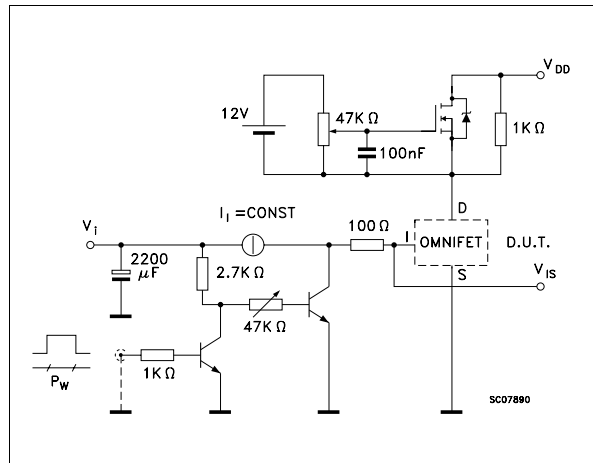


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

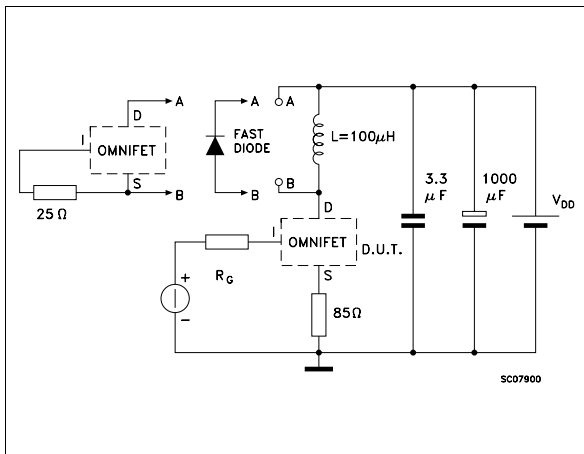
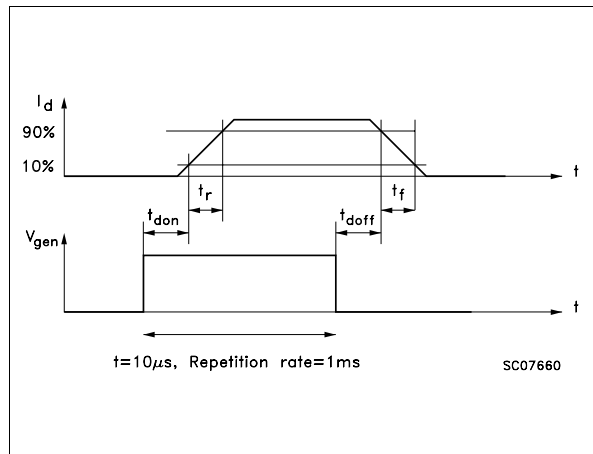


Fig. 6: Waveforms



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