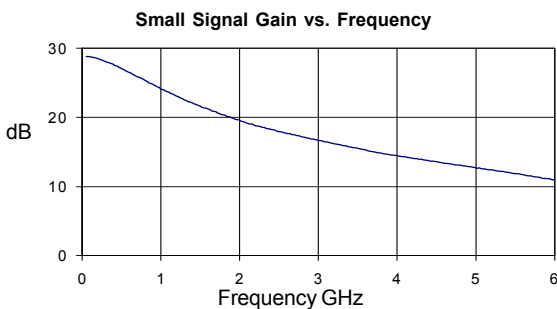


Product Description

Stanford Microdevices' SGA-3586 is a high performance cascadeable 50-ohm amplifier designed for operation at voltages as low as 3.5V. This RFIC uses the latest Silicon Germanium Heterostructure Bipolar Transistor (SiGe HBT) process featuring 1 micron emitters with F_T up to 50 GHz.

This circuit uses a darlington pair topology with resistive feedback for broadband performance as well as stability over its entire temperature range. Internally matched to 50 ohm impedance, the SGA-3586 requires only DC blocking and bypass capacitors for external components.



Electrical Specifications

Symbol	Parameters: Test Conditions: $Z_0 = 50 \text{ Ohms}$, $I_b = 35 \text{ mA}$, $T = 25^\circ\text{C}$	Units	Min.	Typ.	Max.
P_{1dB}	Output Power at 1dB Compression	f = 850 MHz f = 1950 MHz f = 2400 MHz	dBm dBm dBm		13.5 13.5 13.2
IP_3	Third Order Intercept Point Power out per tone = -5 dBm	f = 850 MHz f = 1950 MHz f = 2400 MHz	dBm dBm dBm		24.9 26.1 26.5
S_{21}	Small Signal Gain	f = 850 MHz f = 1950 MHz f = 2400 MHz	dB dB dB		25.0 19.7 18.3
Bandwidth	(Determined by S_{11} , S_{22} Values)		MHz		5000
S_{11}	Input VSWR	f = DC-5000 MHz	-		1.6:1
S_{22}	Output VSWR	f = DC-5000 MHz	-		1.25:1
S_{12}	Reverse Isolation	f = 850 MHz f = 1950 MHz f = 2400 MHz	dB dB dB		28.1 24.1 22.4
NF	Noise Figure, $Z_s = 50 \text{ Ohms}$	f = 1950 MHz	dB		2.5
V_D	Device Voltage		V		3.5
Rth,j-l	Thermal Resistance (junction - lead)		$^\circ\text{C/W}$		97

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SGA-3586

DC-5000 MHz Silicon Germanium Cascadeable Gain Block



Product Features

- DC-5000 MHz Operation
- Single Voltage Supply
- High Gain: 25 dB typ. at 850 MHz
- Low Current Draw: 35mA at 3.5V typ.
- Low Noise Figure: 2.5 dB typ. at 1950 MHz

Applications

- Oscillator Amplifiers
- PA for Low Power Applications
- IF/ RF Buffer Amplifier
- Drivers for CATV Amplifiers

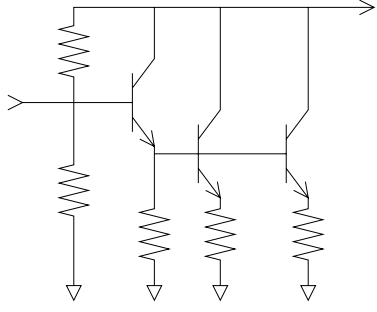
Absolute Maximum Ratings

Operation of this device above any one of these parameters may cause permanent damage.

Bias Conditions should also satisfy the following expression:
 $I_D V_D (\text{max}) < (T_J - T_{OP})/R_{th, j-l}$

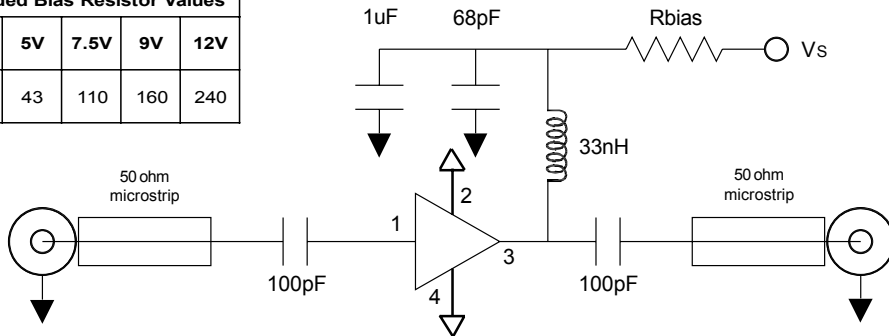
Parameter	Value	Unit
Supply Current	70	mA
Operating Temperature	-40 to +85	C
Maximum Input Power	0	dBm
Storage Temperature Range	-40 to +150	C
Operating Junction Temperature	+150	C

Parameter	Typical		Test Condition ($I_D = 35 \text{ mA}$, unless otherwise noted)
	25°C	Unit	
500 MHz			
Gain	27.1	dB	$Z_s = 50 \text{ Ohms}$ Tone spacing = 1 MHz, Pout per tone = -5 dBm
Noise Figure	2.4	dB	
Output IP3	23.5	dBm	
Output P1dB	13.3	dBm	
Input Return Loss	12.8	dB	
Isolation	29.0	dB	
850 MHz			
Gain	25.0	dB	$Z_s = 50 \text{ Ohms}$ Tone spacing = 1 MHz, Pout per tone = -5 dBm
Noise Figure	2.5	dB	
Output IP3	24.9	dBm	
Output P1dB	13.5	dBm	
Input Return Loss	10.7	dB	
Isolation	28.1	dB	
1950 MHz			
Gain	19.7	dB	$Z_s = 50 \text{ Ohms}$ Tone spacing = 1 MHz, Pout per tone = -5 dBm
Noise Figure	2.5	dB	
Output IP3	26.1	dBm	
Output P1dB	13.5	dBm	
Input Return Loss	10.5	dB	
Isolation	24.1	dB	
2400 MHz			
Gain	18.3	dB	$Z_s = 50 \text{ Ohms}$ Tone spacing = 1 MHz, Pout per tone = -5 dBm
Noise Figure	2.5	dB	
Output IP3	26.5	dBm	
Output P1dB	13.2	dBm	
Input Return Loss	11.1	dB	
Isolation	22.4	dB	

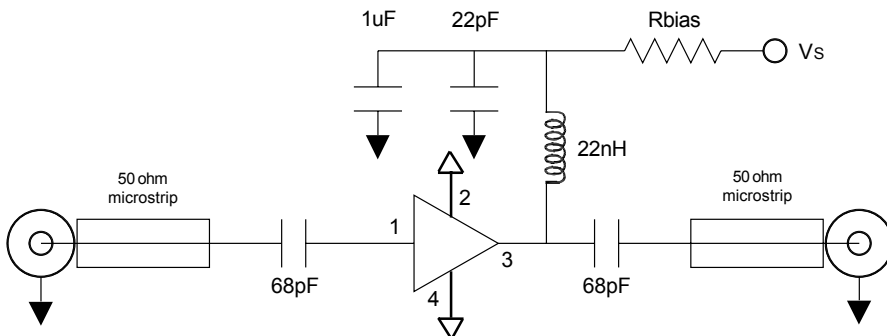
Pin #	Function	Description	Device Schematic
1	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.	
2	GND	Connection to ground. Use via holes for best performance to reduce lead inductance. Place vias as close to ground leads as possible.	
3	RF OUT/Vcc	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed.	
4	GND	Same as Pin 2.	

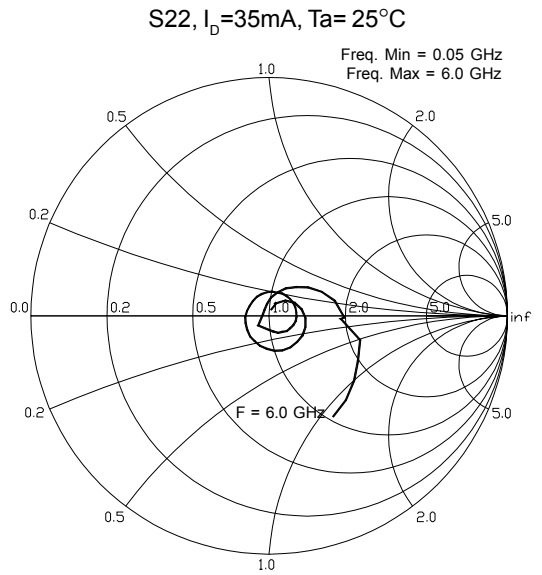
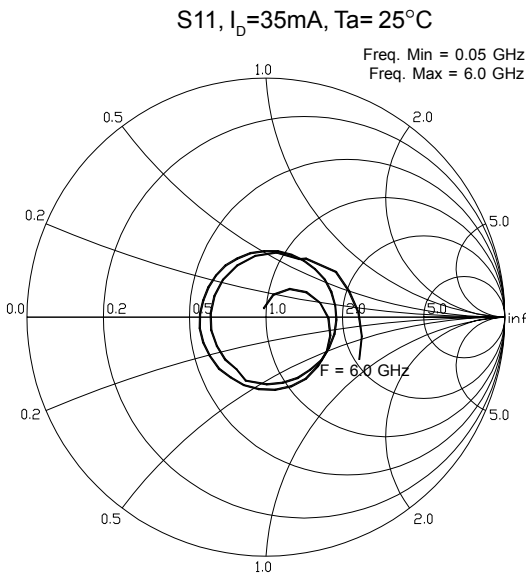
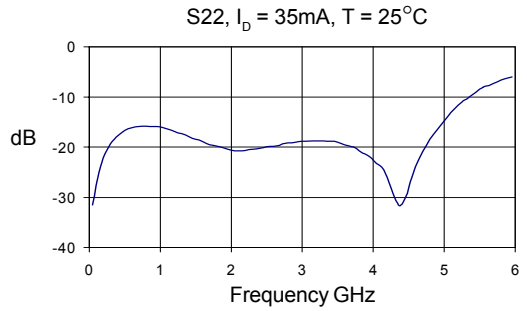
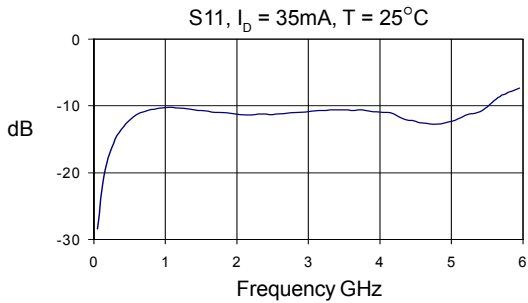
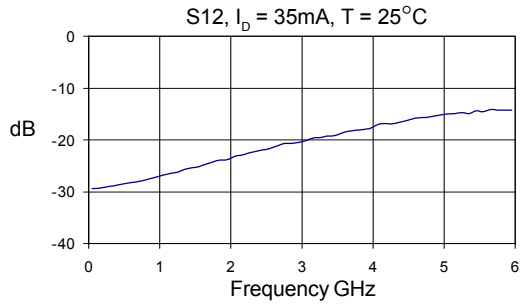
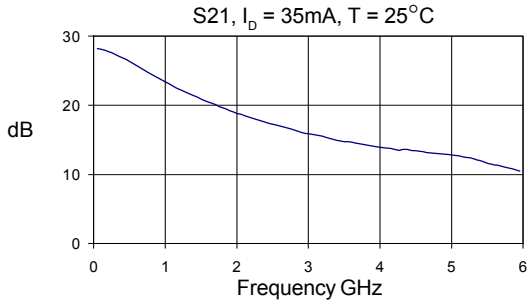
Application Schematic for Operation at 850 MHz

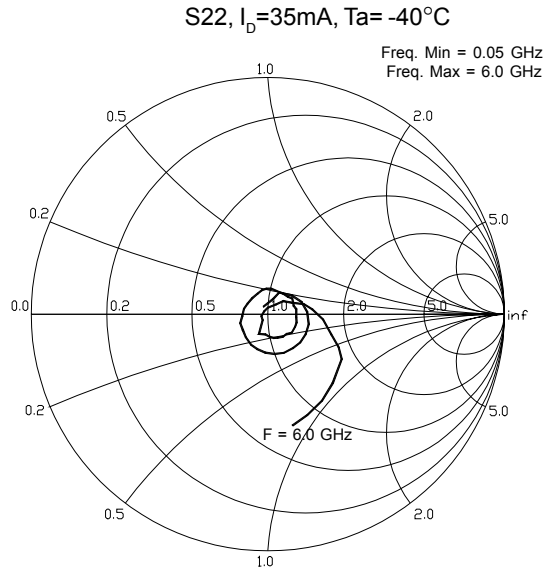
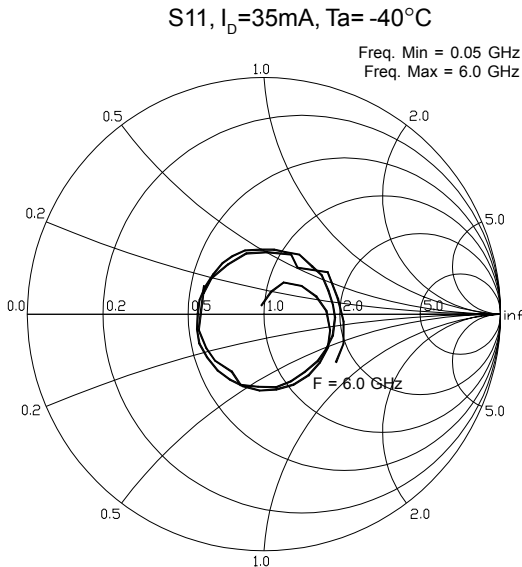
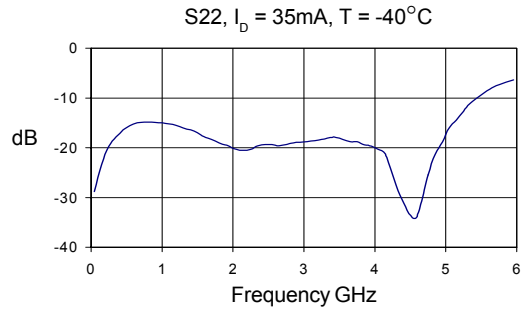
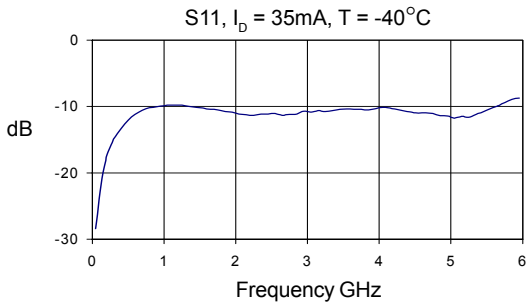
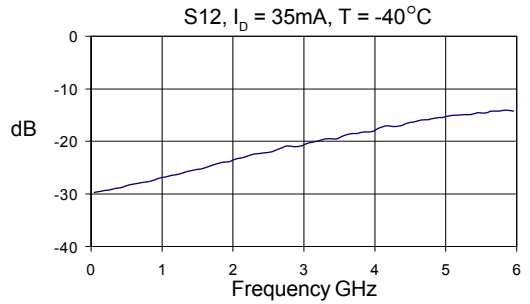
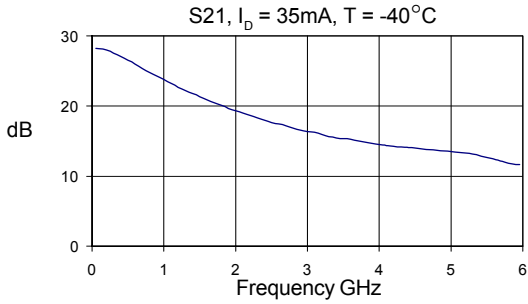
Recommended Bias Resistor Values				
Supply Voltage (Vs)	5V	7.5V	9V	12V
Rbias (Ohms)	43	110	160	240

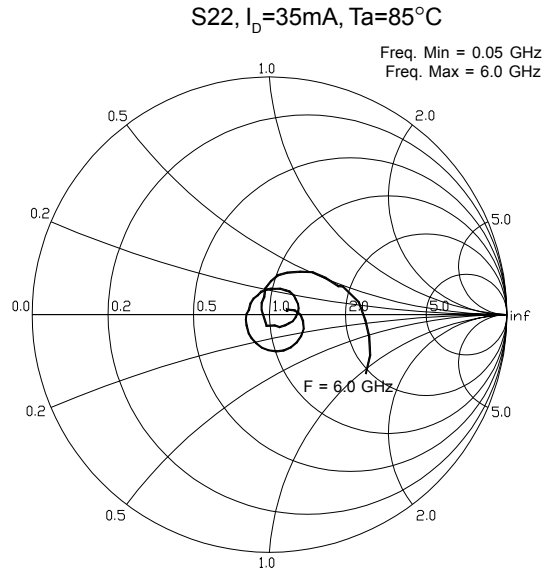
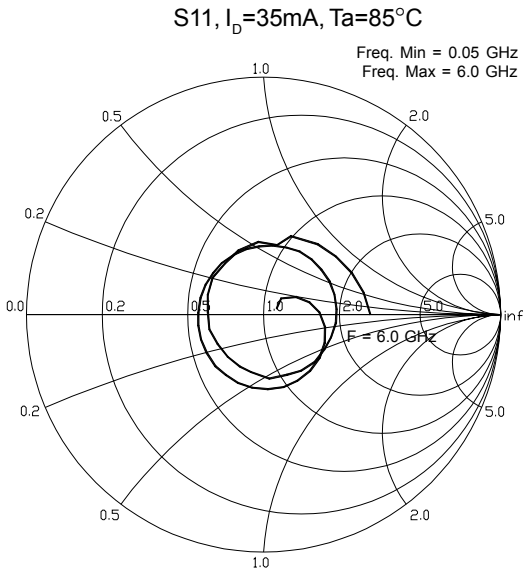
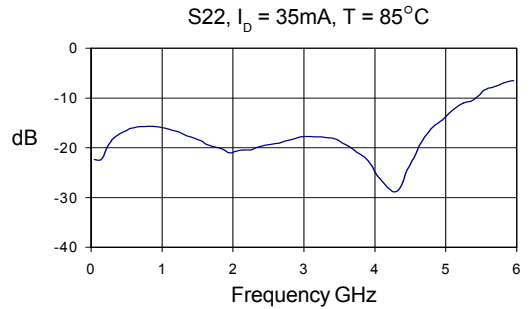
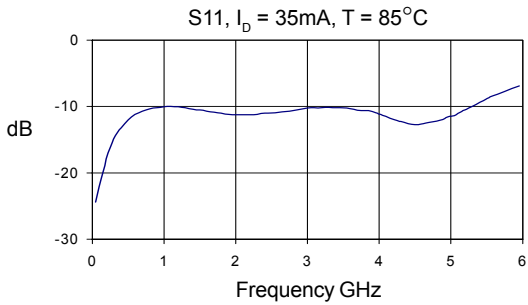
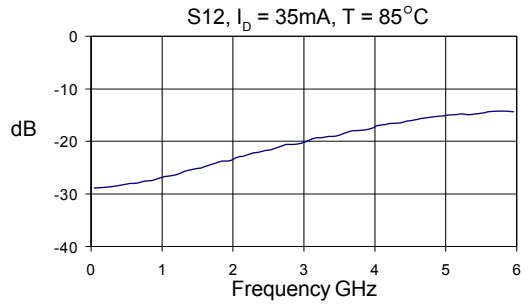
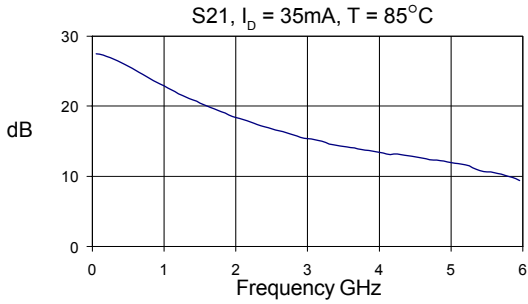


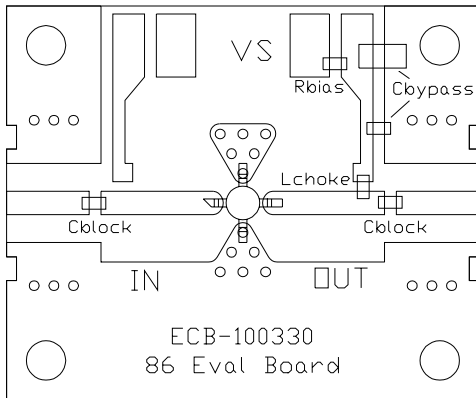
Application Schematic for Operation at 1950 MHz











Evaluation Board Layout

Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SGA-3586	13"	3000



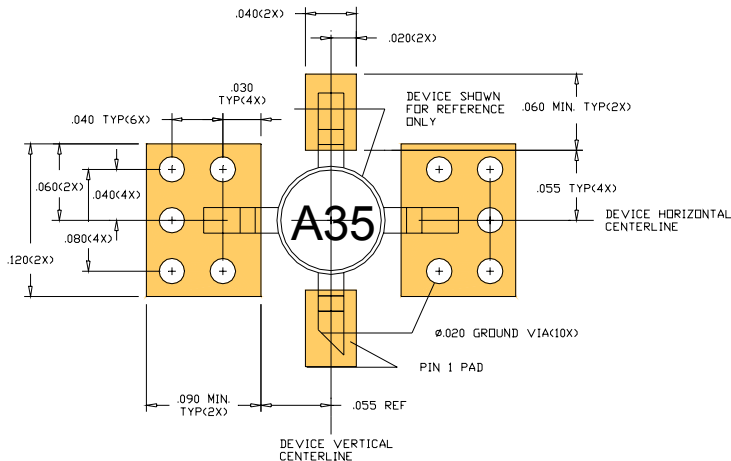
Caution ESD Sensitive:

Appropriate precautions in handling, packaging and testing devices must be observed.

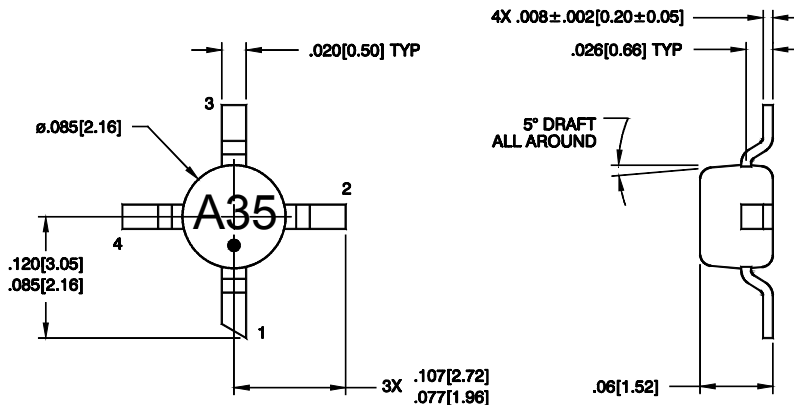
Part Symbolization

The part will be symbolized with an "A35" designator on the top surface of the package.

PCB Pad Layout



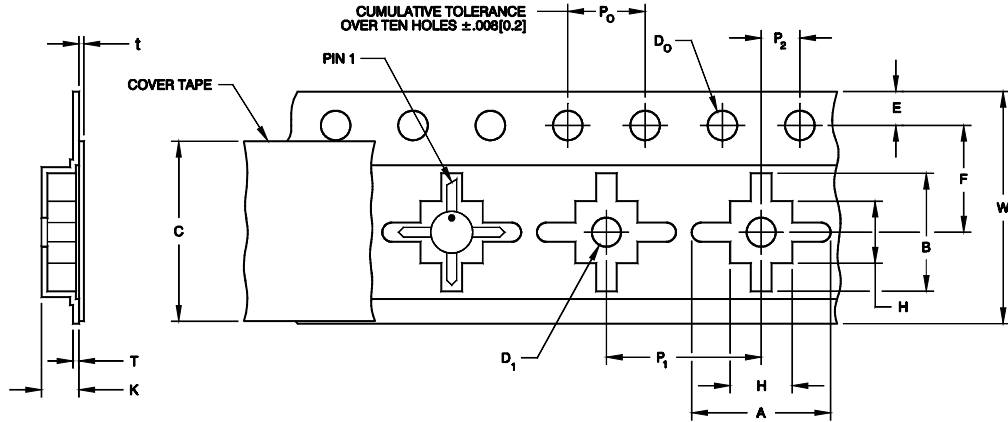
Package Dimensions



Component Tape and Reel Packaging

Tape Dimensions

For 86 Outline



DESCRIPTION		SYMBOL	SIZE (MM)
Cavity	Length	A	6.10 ± 0.10
	Width	B	6.20 ± 0.10
	Socket	H	3.10 ± 0.10
	Depth	K	2.00 ± 0.10
	Pitch	P	8.00 ± 0.10
	Bottom Hole diameter	D ₁	1.50 min.
Perforation	Diameter	D ₀	1.50 ± 0.10
	Pitch	P ₀	4.00 ± 0.10
	Position	E	1.75 ± 0.10
Cover Tape	Width	C	9.10 ± 0.25
	Tape Thickness	t	0.05 ± 0.01
Carrier Tape	Width	W	12.00 ± 0.30
	Tape Thickness	T	0.30 ± 0.05
Distance	Cavity to Perforation (Width Direction)	F	5.50 ± 0.05
	Cavity to Perforation (Length Direction)	P ₂	2.00 ± 0.05