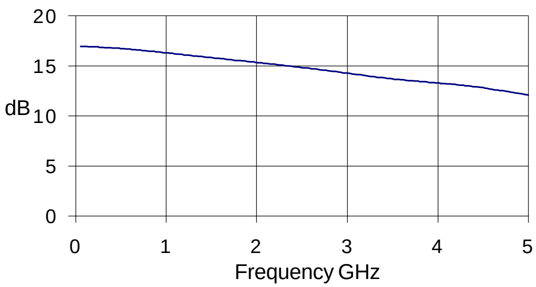
Product Description

Stanford Microdevices' SGA-5389 is a high performance cascadeable 50-ohm amplifier designed for operation at voltages as low as 3.6V. This RFIC uses the latest Silicon Germanium Heterostructure Bipolar Transistor (SiGe HBT) process featuring 1 micron emitters with F_T up to 50 GHz.

This circuit uses a darlington pair topology with resistive feedback for broadband performance as well as stability over its entire temperature range. Internally matched to 50 ohm impedance, the SGA-5389 requires only DC blocking and bypass capacitors for external components.

Small Signal Gain vs. Frequency



Preliminary

SGA-5389

DC-3200 MHz Silicon Germanium HBT Cascadeable Gain Block

Product Features

- **DC-3200 MHz Operation**
- **Single Voltage Supply**
- **High Output Intercept: +31.5 dBm typ. at 850 MHz**
- **Low Current Draw: 60mA at 3.6V typ.**
- **Low Noise Figure: 3.3 dB typ. at 850 MHz**

Applications

- **Oscillator Amplifiers**
- **PA for Low Power Applications**
- **IF/ RF Buffer Amplifier**
- **Drivers for CATV Amplifiers**

Symbol	Parameters: Test Conditions: Z_0 = 50 Ohms, I_D = 60 mA, T = 25°C		Units	Min.	Typ.	Max.
P_{1dB}	Output Power at 1dB Compression	f = 850 MHz f = 1950 MHz f = 2400 MHz	dBm dBm dBm		16.3 15.0 14.1	
IP_3	Third Order Intercept Point Power out per tone = 0 dBm	f = 850 MHz f = 1950 MHz f = 2400 MHz	dBm dBm dBm		31.5 28.1 26.6	
S_{21}	Small Signal Gain	f = 850 MHz f = 1950 MHz f = 2400 MHz	dB dB dB		16.9 15.8 15.4	
Bandwidth	3dB Bandwidth		MHz		3200	
S_{11}	Input VSWR	f = DC-5000 MHz	-		1.25:1	
S_{22}	Output VSWR	f = DC-5000 MHz	-		1.40:1	
S_{12}	Reverse Isolation	f = 850 MHz f = 1950 MHz f = 2400 MHz	dB dB dB		21.3 21.7 21.8	
NF	Noise Figure, Z_S = 50 Ohms	f = 1950 MHz	dB		2.8	
V_D	Device Voltage		V	3.1	3.5	4.1
Rth,j-l	Thermal Resistance (junction - lead)		°C/W		97	

Absolute Maximum Ratings

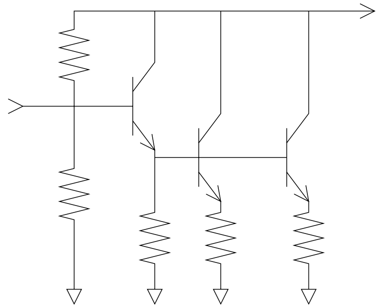
Operation of this device above any one of these parameters may cause permanent damage.

Bias Conditions should also satisfy the following expression:
$I_D V_D$ (max) < $(T_J - T_{OP})$/Rth, j-l

Parameter	Value	Unit
Supply Current	120	mA
Operating Temperature	-40 to +85	C
Maximum Input Power	+10	dBm
Storage Temperature Range	-40 to +150	C
Operating Junction Temperature	+150	C

Key parameters, at typical operating frequencies:

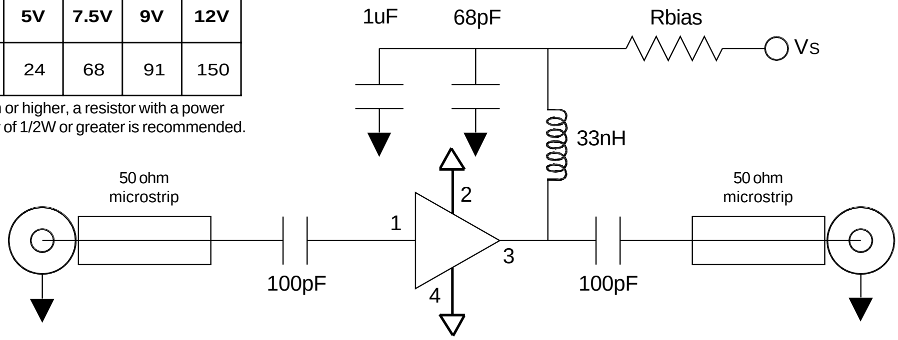
Parameter	Typical 25ºC	Unit	Test Condition (I_D = 60 mA, unless otherwise noted)
500 MHz			
Gain	17.1	dB	
Noise Figure	3.4	dB	Z_S = 50 Ohms
Output IP3	31.8	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	16.7	dBm	
Input Return Loss	23.3	dB	
Isolation	21.0	dB	
850 MHz			
Gain	16.9	dB	
Noise Figure	3.3	dB	Z_S = 50 Ohms
Output IP3	31.5	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	16.3	dBm	
Input Return Loss	20.8	dB	
Isolation	21.3	dB	
1950 MHz			
Gain	15.8	dB	
Noise Figure	2.8	dB	Z_S = 50 Ohms
Output IP3	28.1	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	15.0	dBm	
Input Return Loss	18.7	dB	
Isolation	21.7	dB	
2400 MHz			
Gain	15.4	dB	
Noise Figure	4.1	dB	Z_S = 50 Ohms
Output IP3	26.6	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	14.1	dBm	
Input Return Loss	19.4	dB	
Isolation	21.8	dB	

Pin #	Function	Description	Device Schematic
1	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.	
2	GND	Connection to ground. Use via holes for best performance to reduce lead inductance. Place vias as close to ground leads as possible.	
3	RF OUT/Vcc	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed.	
4	GND	Same as Pin 2.	

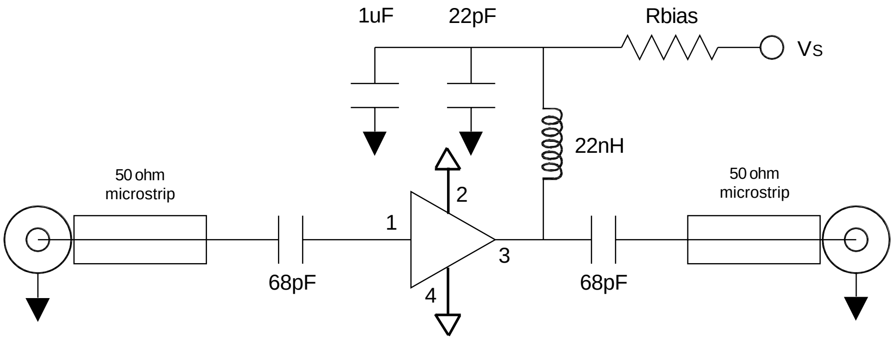
Application Schematic for Operation at 850 MHz

Recommended Bias Resistor Values				
Supply Voltage(Vs)	5V	7.5V	9V	12V
Rbias (Ohms)	24	68	91	150

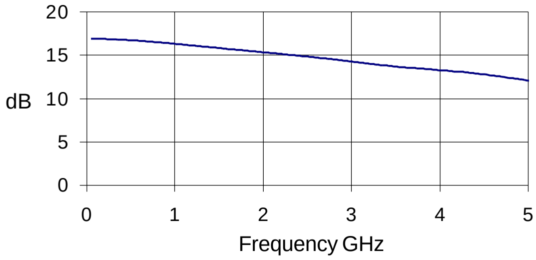
For 7.5V operation or higher, a resistor with a power handling capability of 1/2W or greater is recommended.



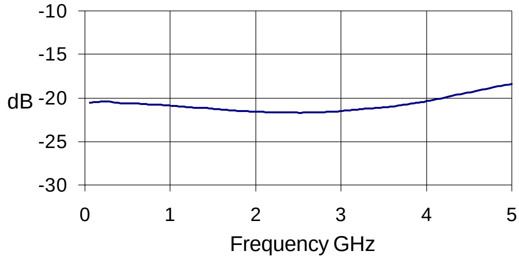
Application Schematic for Operation at 1950 MHz



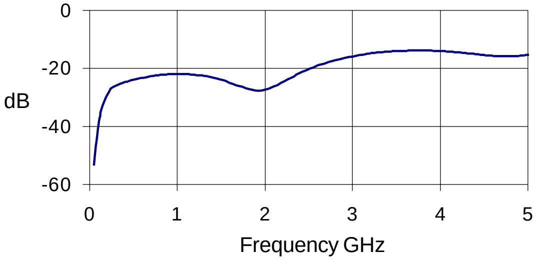
S21, I_D =60mA, T=+25C



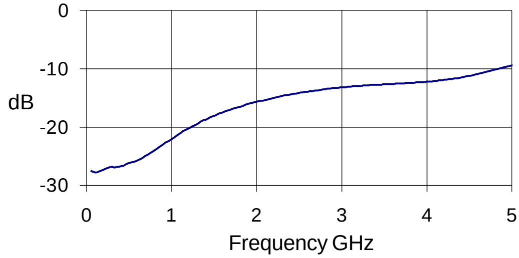
S12, I_D =60mA, T=+25C



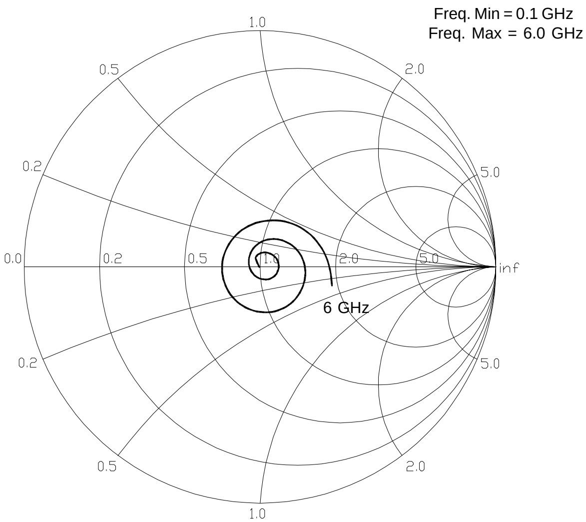
S11, I_D =60mA, T=+25C



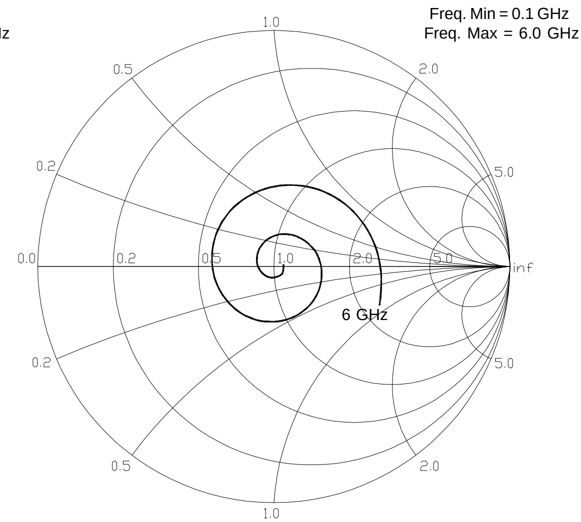
S22, I_D =60mA, T=+25C



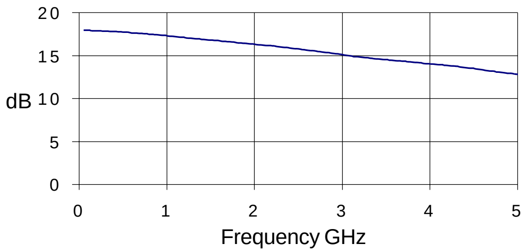
S11, I_D=60mA, Ta= +25C



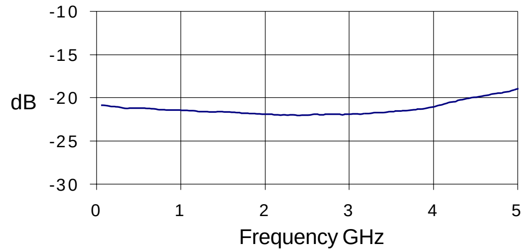
S22, I_D=60mA, Ta= +25C



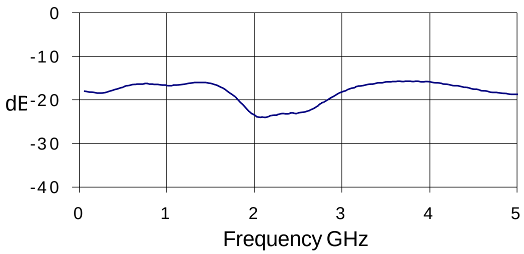
S21, I_D =60mA, T=-40C



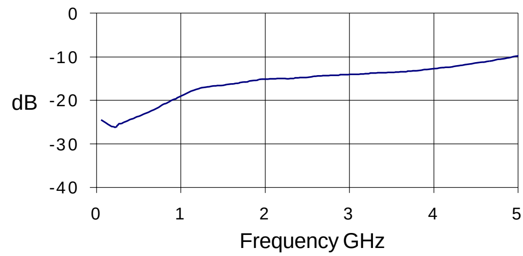
S12, I_D =60mA, T=-40C



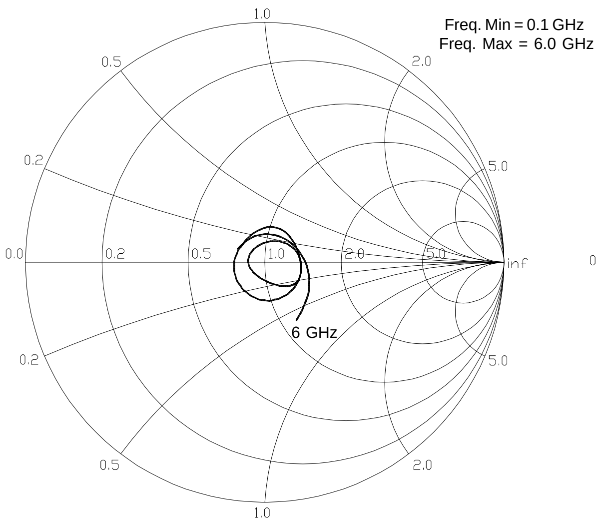
S11, I_D =60mA, T=-40C



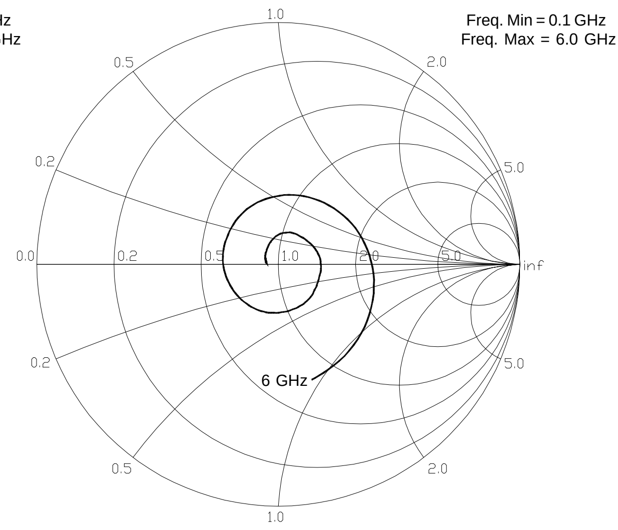
S22, I_D =60mA, T=-40C

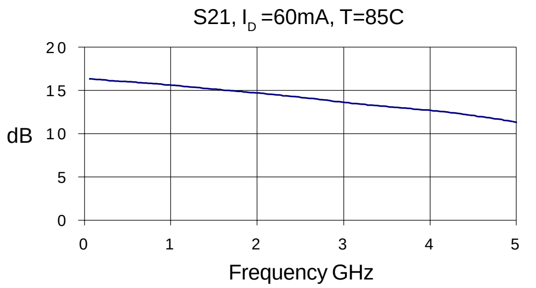


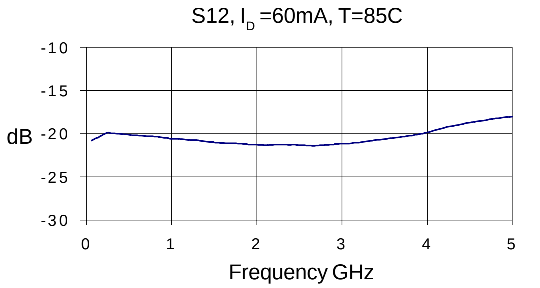
S11, I_D=60mA, Ta= -40C

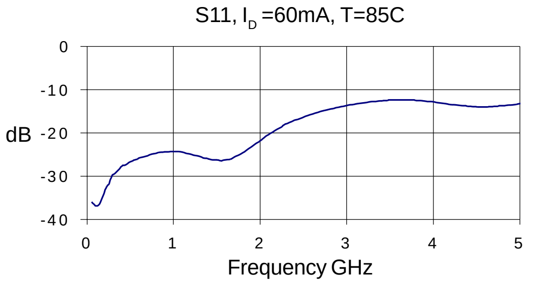


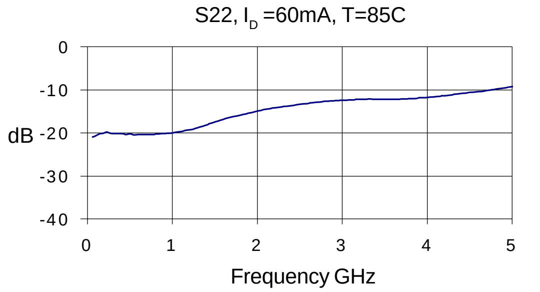
S22, I_D=60mA, Ta= -40C

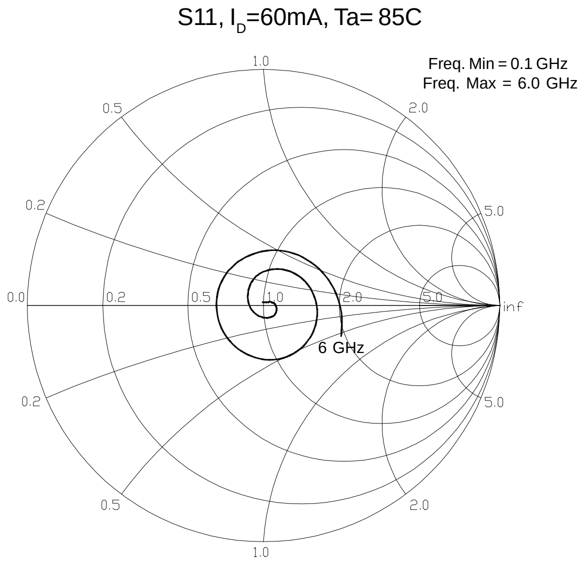


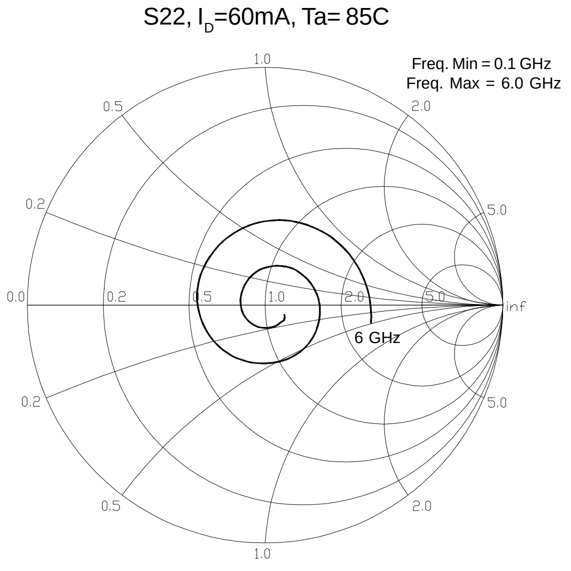

S21, I_D =60mA, T=85C
20
15
dB 10
5
0
0
1
2
3
4
5
Frequency GHz


S12, I_D =60mA, T=85C
-10
-15
dB -20
-25
-30
0
1
2
3
4
5
Frequency GHz


S11, I_D =60mA, T=85C
0
-10
dB -20
-30
-40
0
1
2
3
4
5
Frequency GHz


S22, I_D =60mA, T=85C
0
-10
dB -20
-30
-40
0
1
2
3
4
5
Frequency GHz


S11, I_D=60mA, Ta= 85C
Freq. Min = 0.1 GHz
Freq. Max = 6.0 GHz
6 GHz


S22, I_D=60mA, Ta= 85C
Freq. Min = 0.1 GHz
Freq. Max = 6.0 GHz
6 GHz

STANFORD MICRODEVICES

Preliminary

SGA-5389 DC-3200 MHz 3.5V SiGe Amplifier

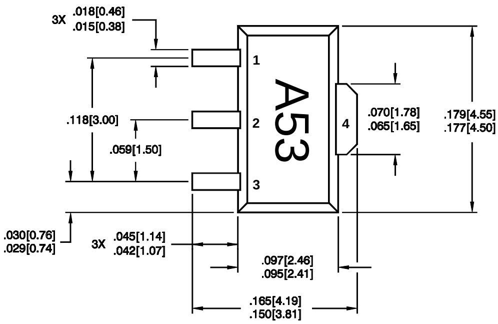
Caution ESD Sensitive:
Appropriate precautions in handling, packaging and testing devices must be observed.

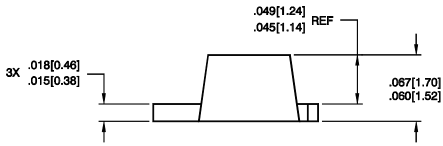
Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SGA-5389	13"	3000

Package Dimensions

Outline Drawing





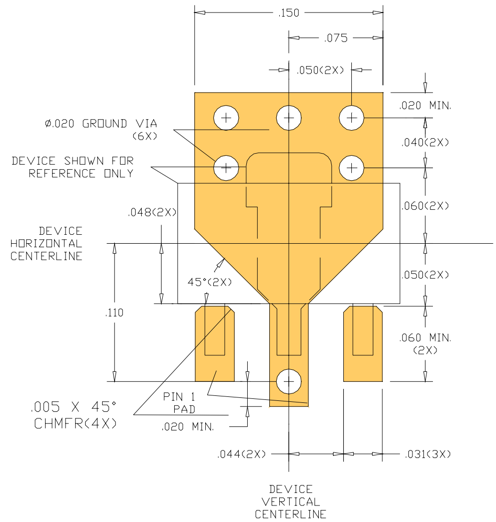
DIMENSIONS ARE IN INCHES [MM]

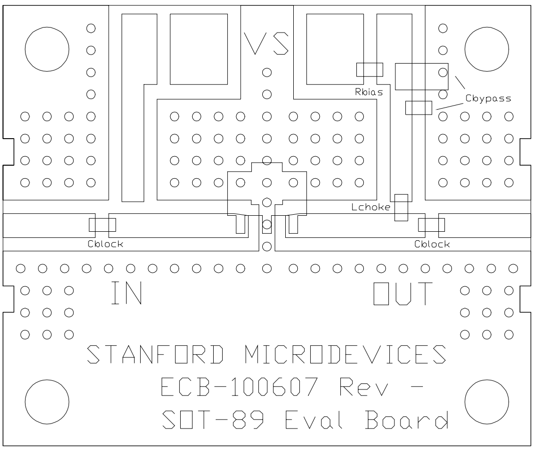
Pin assignments shown for reference only, not marked on part

Part Symbolization

The part will be symbolized with a “A53” designator on the top surface of the package.

PCB Pad Layout

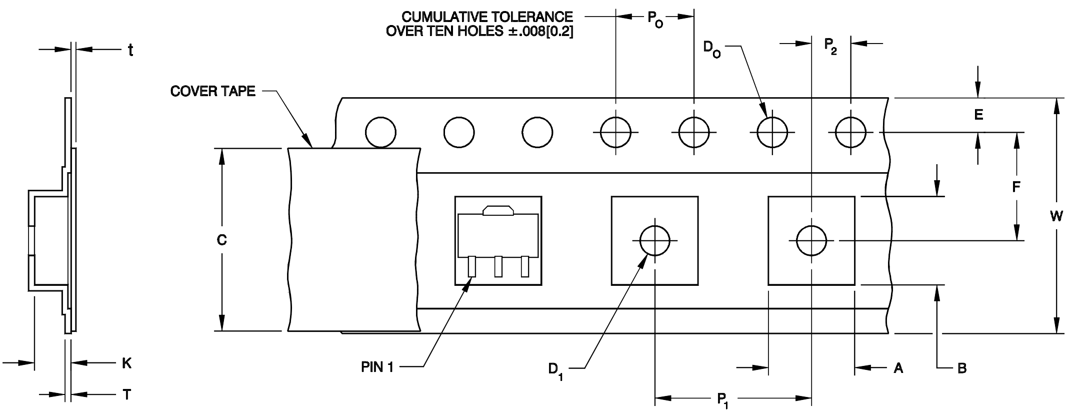




Component Tape and Reel Packaging

Tape Dimensions

For 89 Outline



DETAIL A

Description		Symbol	Size (mm)
Cavity	Length Width Depth Pitch Bottom Hole Diameter	A B K P_1 D_1	4.91 +/- 0.01 4.52 +/- 0.01 1.90 +/- 0.01 8.00 +/- 0.01 1.60 +/- 0.10
Perforation	Diameter Pitch Position	D_0 P_0 E	1.55 +/- 0.05 4.00 +/- 0.01 1.75 +/- 0.01
Cover Tape	Width Tape Thickness	C t	9.10 +/- 0.25 0.05 +/- 0.01
Carrier Tape	Width Thickness	W T	12.0 +/- 0.03 0.30 +/- 0.05
Distance	Cavity to Perforation (Width Direction) Cavity to Perforation (Length Direction)	F P_2	5.50 +/- 0.10 2.00 +/- 0.10