Preliminary

SGA-5586

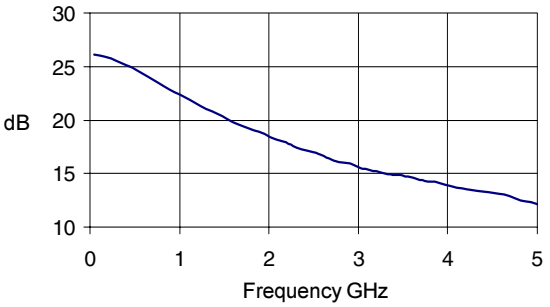
DC-4000 MHz Silicon Germanium HBT Cascadeable Gain Block

Product Description

Stanford Microdevices' SGA-5586 is a high performance cascadeable 50-ohm amplifier designed for operation at voltages as low as 3.9V. This RFIC uses the latest Silicon Germanium Heterostructure Bipolar Transistor (SiGe HBT) process featuring 1 micron emitters with F_T up to 50 GHz.

This circuit uses a darlington pair topology with resistive feedback for broadband performance as well as stability over its entire temperature range. Internally matched to 50 ohm impedance, the SGA-5586 requires only DC blocking and bypass capacitors for external components.

Small Signal Gain vs. Frequency



Product Features

- DC-4000 MHz Operation
- Single Voltage Supply
- High Output Intercept: +32 dBm typ. at 850 MHz
- Low Current Draw: 60mA at 3.9V typ.
- Low Noise Figure: 2.5dB typ. at 850 MHz

Applications

- Oscillator Amplifiers
- PA for Low Power Applications
- IF/ RF Buffer Amplifier
- Drivers for CATV Amplifiers

Symbol	Parameters: Test Conditions: Z_0 = 50 Ohms, I_D = 60 mA, T = 25°C		Units	Min.	Typ.	Max.
P_{1dB}	Output Power at 1dB Compression	f = 850 MHz f = 1950 MHz f = 2400 MHz	dBm dBm dBm		18.1 15.8 14.4	
IP_3	Third Order Intercept Point Power out per tone = 0 dBm	f = 850 MHz f = 1950 MHz f = 2400 MHz	dBm dBm dBm		31.6 28.8 27.1	
S_{21}	Small Signal Gain	f = 850 MHz f = 1950 MHz f = 2400 MHz	dB dB dB		23.4 19.1 17.8	
Bandwidth	(Determined by S_{11}, S_{22} Values)		MHz		4000	
S_{11}	Input VSWR	f = DC-4000 MHz	-		1.70:1	
S_{22}	Output VSWR	f = DC-4000 MHz	-		1.30:1	
S_{12}	Reverse Isolation	f = 850 MHz f = 1950 MHz f = 2400 MHz	dB dB dB		27.0 23.9 22.2	
NF	Noise Figure, Z_S = 50 Ohms	f = 1950 MHz	dB		2.6	
V_D	Device Voltage		V		3.9	
Rth,j-l	Thermal Resistance (junction - lead)		° C/W		97	

Absolute Maximum Ratings

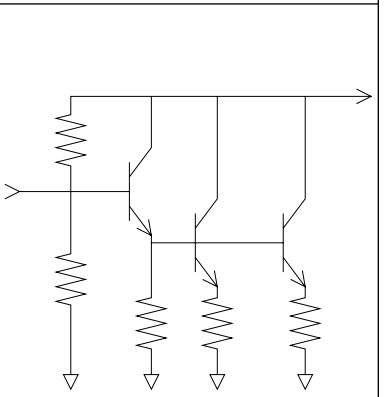
Operation of this device above any one of these parameters may cause permanent damage.

Bias Conditions should also satisfy the following expression:
$I_D V_D$ (max) < (T_J - T_{OP})/Rth, j-l

Parameter	Value	Unit
Supply Current	120	mA
Operating Temperature	-40 to +85	C
Maximum Input Power	+5	dBm
Storage Temperature Range	-40 to +150	C
Operating Junction Temperature	+150	C

Key parameters, at typical operating frequencies:

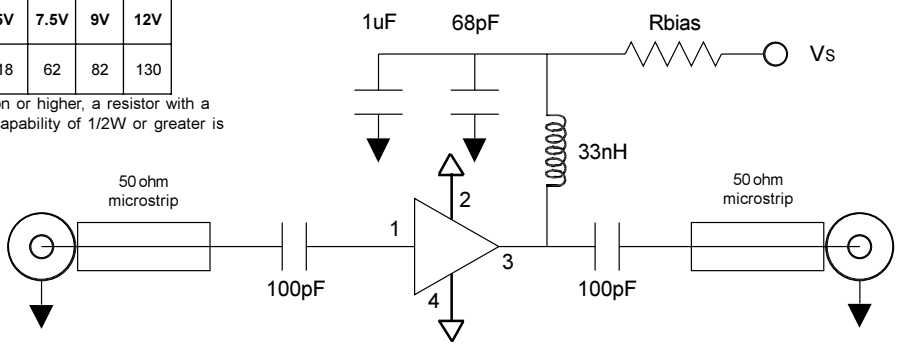
Parameter	Typical 25°C	Unit	Test Condition (I_D = 60 mA, unless otherwise noted)
500 MHz			
Gain	24.8	dB	
Noise Figure	2.5	dB	Z_S = 50 Ohms
Output IP3	31.5	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	18.3	dBm	
Input Return Loss	14.3	dB	
Isolation	27.4	dB	
850 MHz			
Gain	23.4	dB	
Noise Figure	2.5	dB	Z_S = 50 Ohms
Output IP3	31.6	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	18.1	dBm	
Input Return Loss	11.8	dB	
Isolation	27.0	dB	
1950 MHz			
Gain	19.1	dB	
Noise Figure	2.6	dB	Z_S = 50 Ohms
Output IP3	28.8	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	15.8	dBm	
Input Return Loss	10.7	dB	
Isolation	23.9	dB	
2400 MHz			
Gain	17.8	dB	
Noise Figure	3.0	dB	Z_S = 50 Ohms
Output IP3	27.1	dBm	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output P1dB	14.4	dBm	
Input Return Loss	11.0	dB	
Isolation	22.2	dB	

Pin #	Function	Description	Device Schematic
1	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.	
2	GND	Connection to ground. Use via holes for best performance to reduce lead inductance. Place vias as close to ground leads as possible.	
3	RF OUT/Vcc	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed.	
4	GND	Same as Pin 2.	

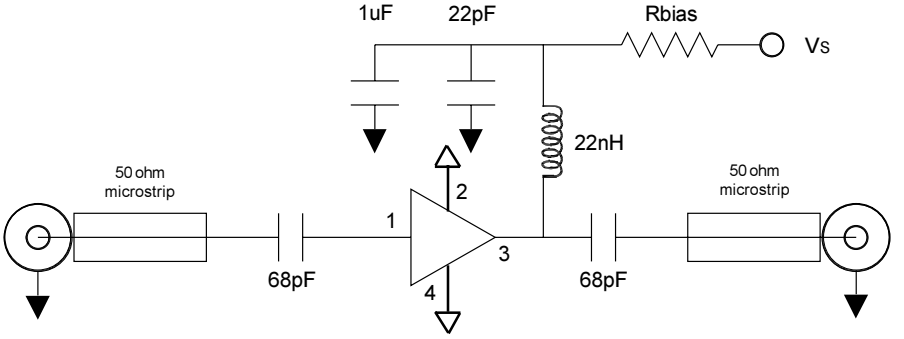
Application Schematic for Operation at 850 MHz

Recommended Bias Resistor Values				
Supply Voltage(Vs)	5V	7.5V	9V	12V
Rbias (Ohms)	18	62	82	130

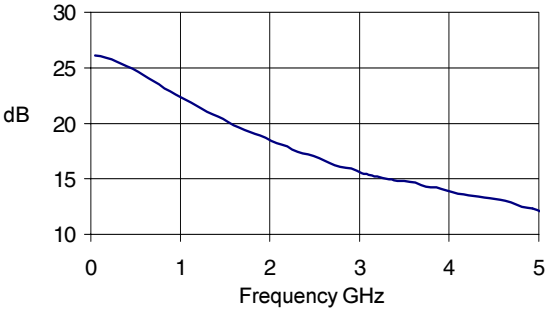
For 7.5V operation or higher, a resistor with a power handling capability of 1/2W or greater is recommended.



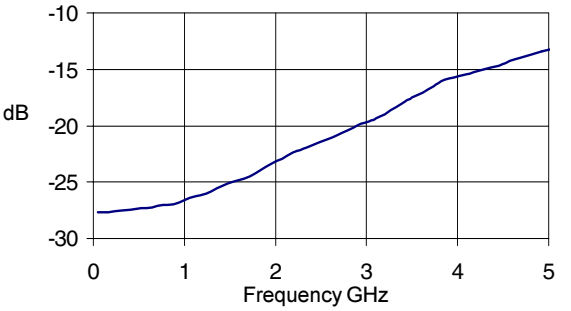
Application Schematic for Operation at 1950 MHz



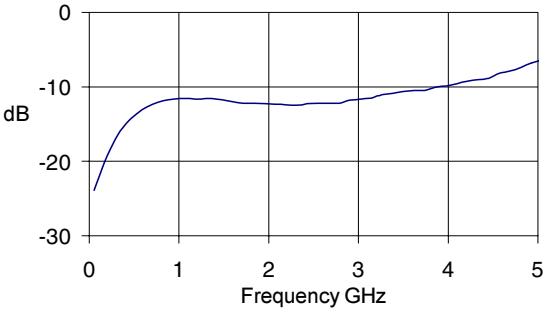
S21, I_D =60mA, T=+25C



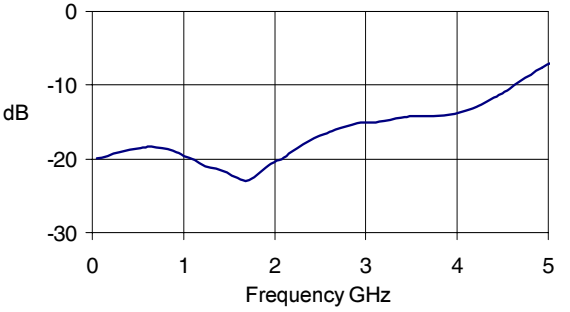
S12, I_D =60mA, T=+25C



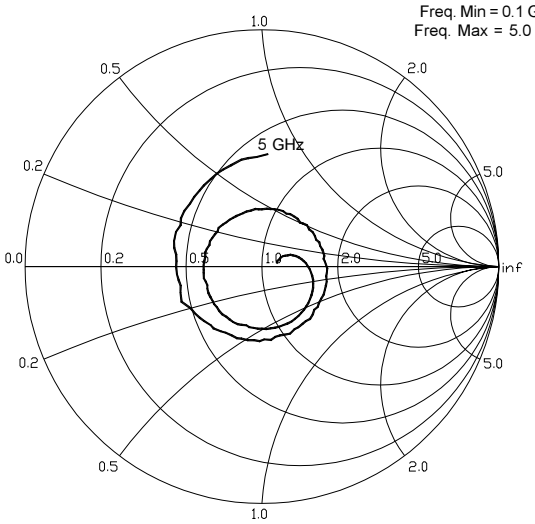
S11, I_D =60mA, T=+25C



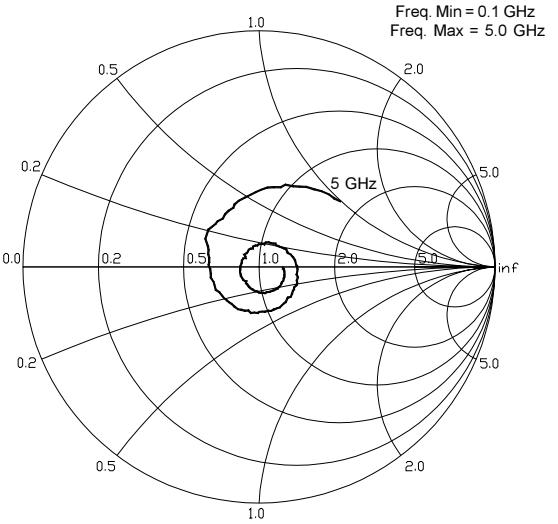
S22, I_D =60mA, T=+25C



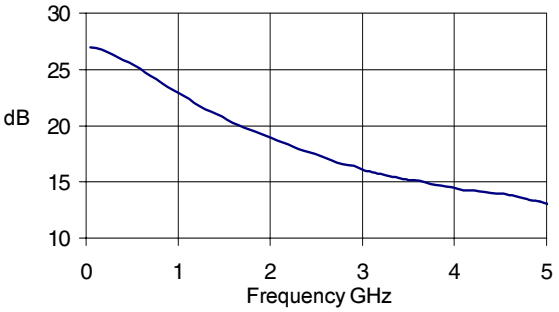
S11, I_D=60mA, Ta=25C



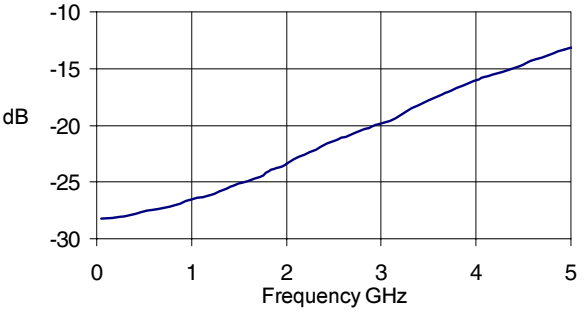
S22, I_D=60mA, Ta=25C



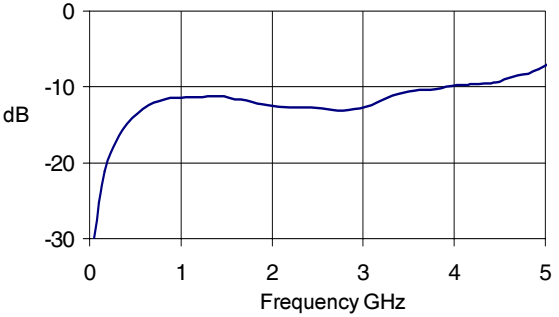
S21, I_D =60mA, T=-40C



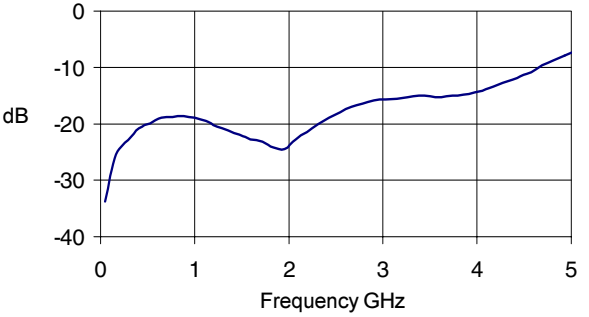
S12, I_D =60mA, T=-40C



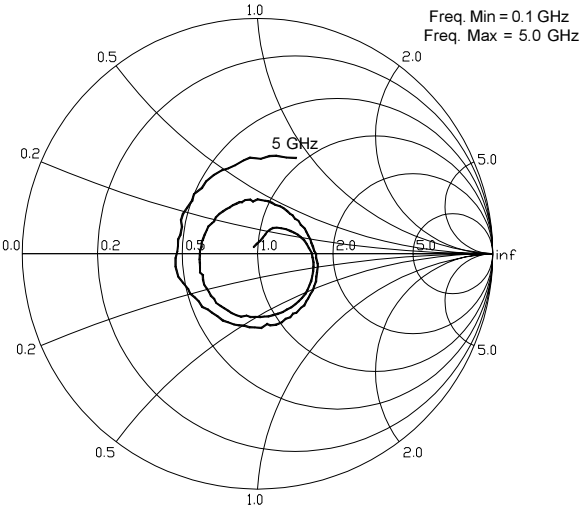
S11, I_D =60mA, T=-40C



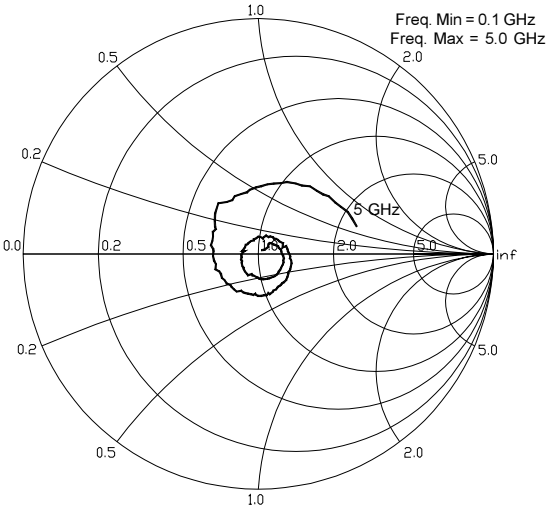
S22, I_D =60mA, T=-40C



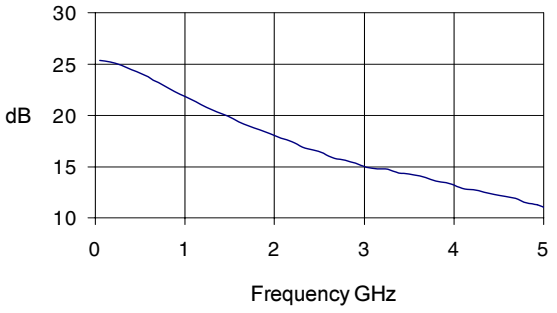
S11, I_D=60mA, Ta= -40C



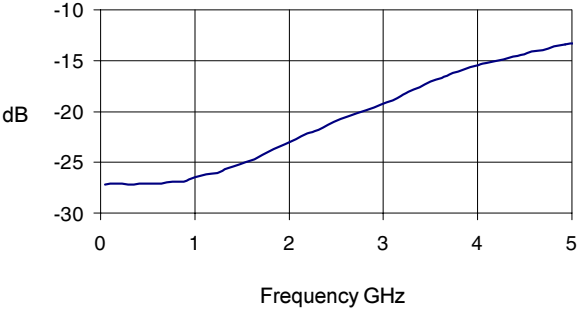
S22, I_D=60mA, Ta= -40C



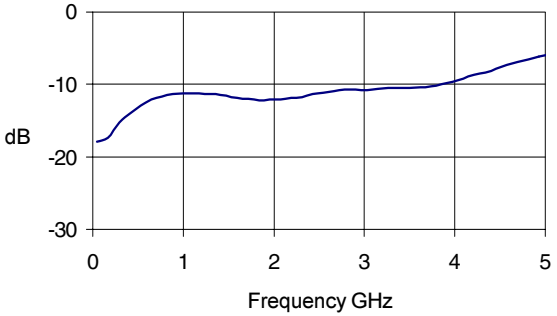
S21, I_D =60mA, T=85C



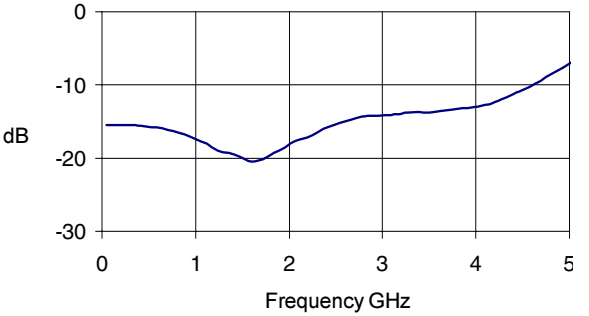
S12, I_D =60mA, T=85C



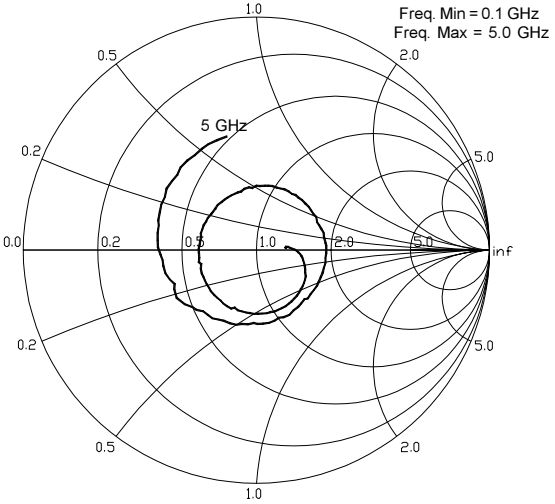
S11, I_D =60mA, T=85C



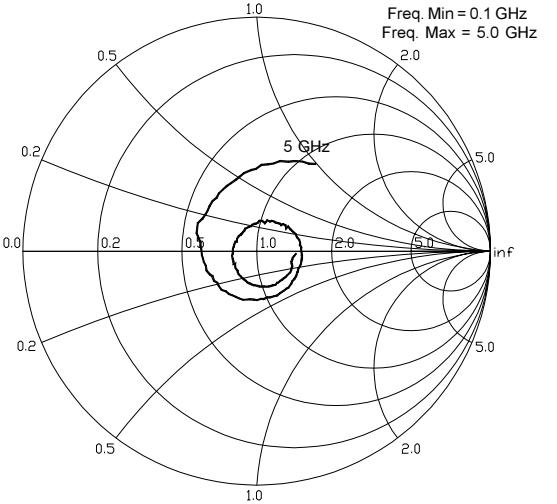
S22, I_D =60mA, T=85C



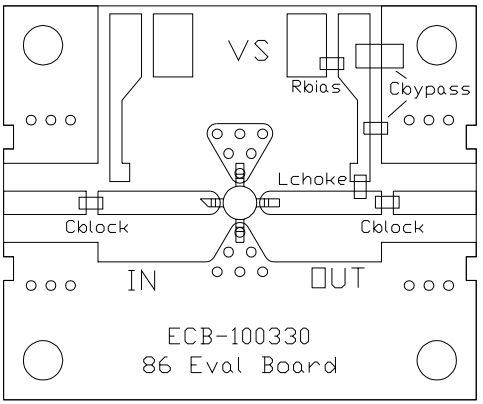
S11, I_D=60mA, Ta=85C



S22, I_D=60mA, Ta=85C



SGA-5586 DC-4000 MHz 3.9V SiGe Amplifier



Evaluation Board Layout

Part Number Ordering Information

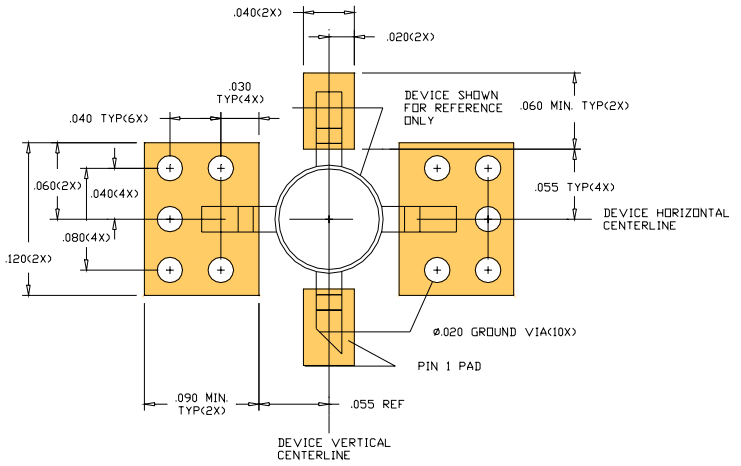
Part Number	Reel Size	Devices/Reel
SGA-5586	13"	3000

Caution ESD Sensitive:
Appropriate precautions in handling, packaging and testing devices must be observed.

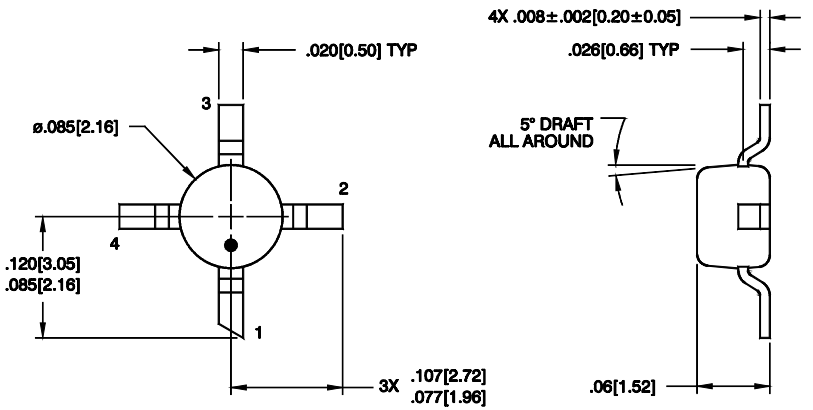
Part Symbolization

The part will be symbolized with an "A55" designator on the top surface of the package.

PCB Pad Layout



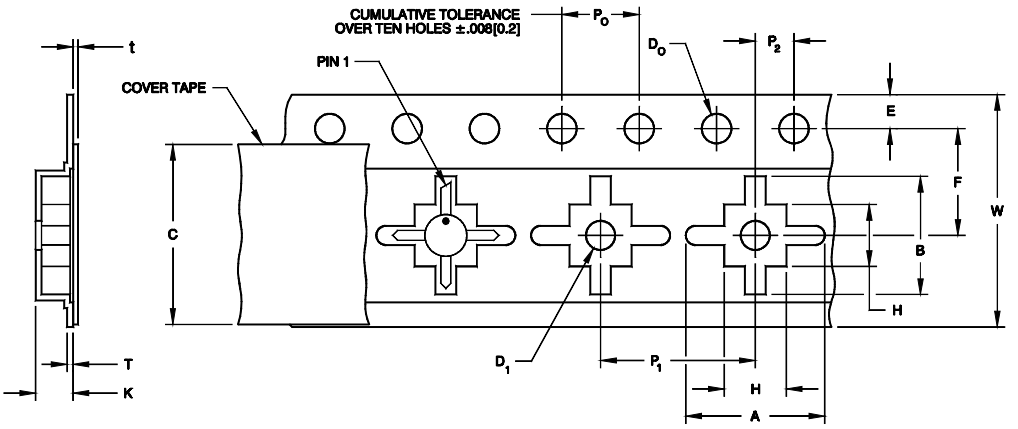
Package Dimensions



Component Tape and Reel Packaging

Tape Dimensions

For 86 Outline



Description		Symbol	Size (mm)
Cavity	Length	A	6.10 ± 0.10
	Width	B	6.20 ± 0.10
	Socket	H	3.10 ± 0.10
	Depth	K	2.00 ± 0.10
	Pitch	P	8.00 ± 0.10
	Bottom Hole diameter	D_1	1.50 min.
Perforation	Diameter	D_o	1.50 ± 0.10
	Pitch	P_o	4.00 ± 0.10
	Position	E	1.75 ± 0.10
Cover Tape	Width	C	9.10 ± 0.25
	Tape Thickness	t	0.05 ± 0.01
Carrier Tape	Width	W	12.00 ± 0.30
	Tape Thickness	T	0.30 ± 0.05
Distance	Cavity to Perforation (Width Direction)	F	5.50 ± 0.05
	Cavity to Perforation (Length Direction)	P_2	2.00 ± 0.05