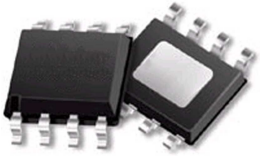
Preliminary

SPA-2118

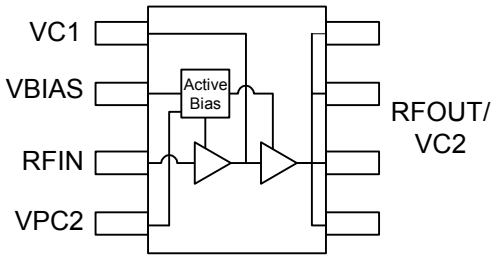
850 MHz 1 Watt Power Amplifier with Active Bias



Product Description

Stanford Microdevices' SPA-2118 is a high efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. These HBT amplifiers are fabricated using molecular beam epitaxial growth technology which produces reliable and consistent performance from wafer to wafer and lot to lot.

This product is specifically designed for use as a driver amplifier for infrastructure equipment in the 850 MHz band. Its high linearity makes it an ideal choice for multi-carrier and digital applications.



Product Features

- **High Linearity Performance:**
  +48 dBm Typ. OIP3 at 900 MHz
  +24 dBm IS-95 CDMA Channel Power at -45 dBc ACP
- **On-chip Active Bias Control**
- **High Gain: 32.5 dB Typ.**
- **Patented High Reliability GaAsHBT Technology**
- **Surface-Mountable Plastic Package**

Applications

- **IS-95 CDMA Systems**
- **Multi-Carrier Applications**
- **AMPS, ISM Applications**

Symbol	Parameters: Test Conditions: Z_0 = 50 Ohms Temp = 25°C, Vcc=5.0V	Units	Min.	Typ.	Max.
f_0	Frequency of Operation	MHz	850	900	950
P_{1dB}	Output Power at 1dB Compression	dBm		30.5	
S_{21}	Small Signal Gain	dB		32.5	
VSWR	Input VSWR	-		1.5:1	
OIP_3	Output Third Order Intercept Point Power out per tone = +14dBm	dBm		48	
NF	Noise Figure	dB		5.0	
Icc	Device Current **Ibias** = 10mA, **Ic1** = 70mA, **Ic2** = 320mA	mA		400	
$R_{th\ j-l}$	Thermal Resistance (junction - lead)	°C/W		32	

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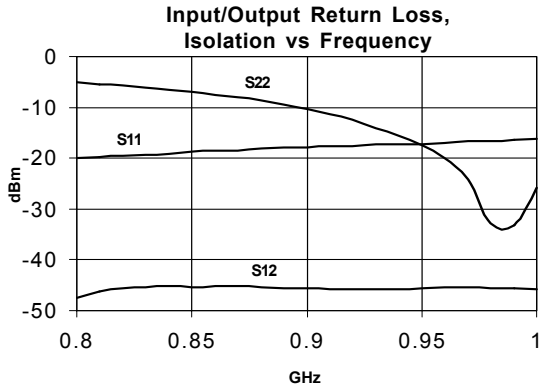
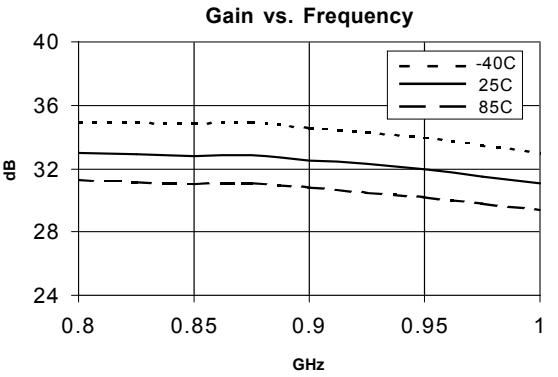
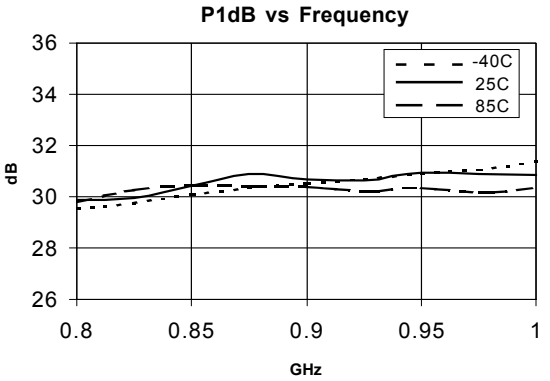
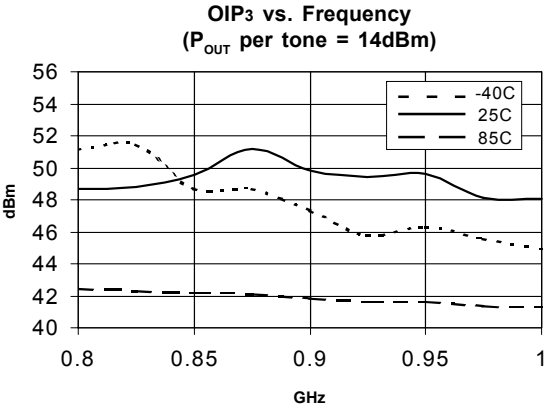
850-950 MHz Application Circuit Data, Icc=400mA, T=+25C, Vcc=5V

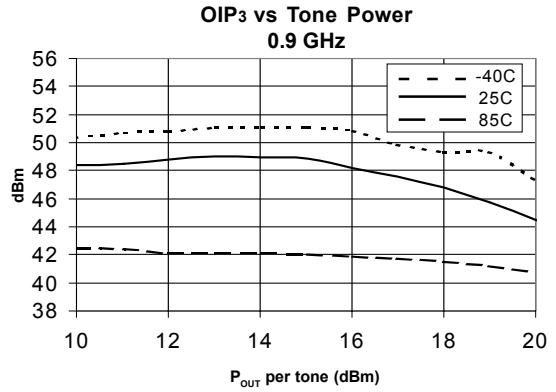
Note: Tuned for Output IP3





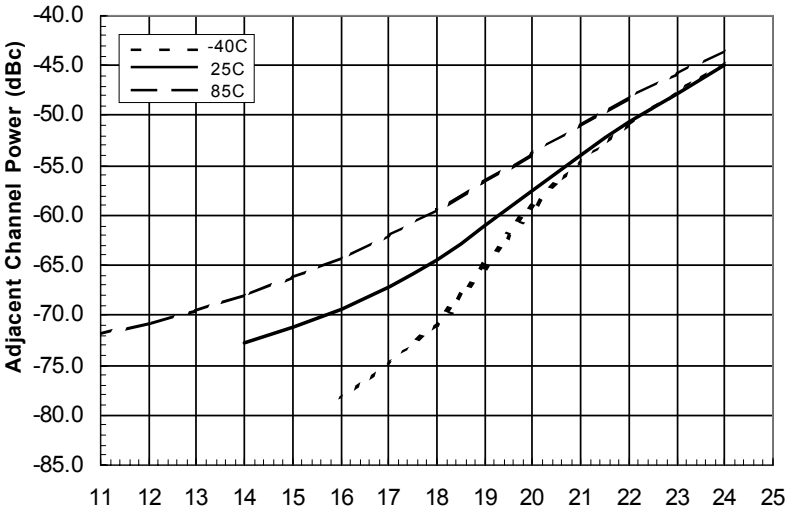




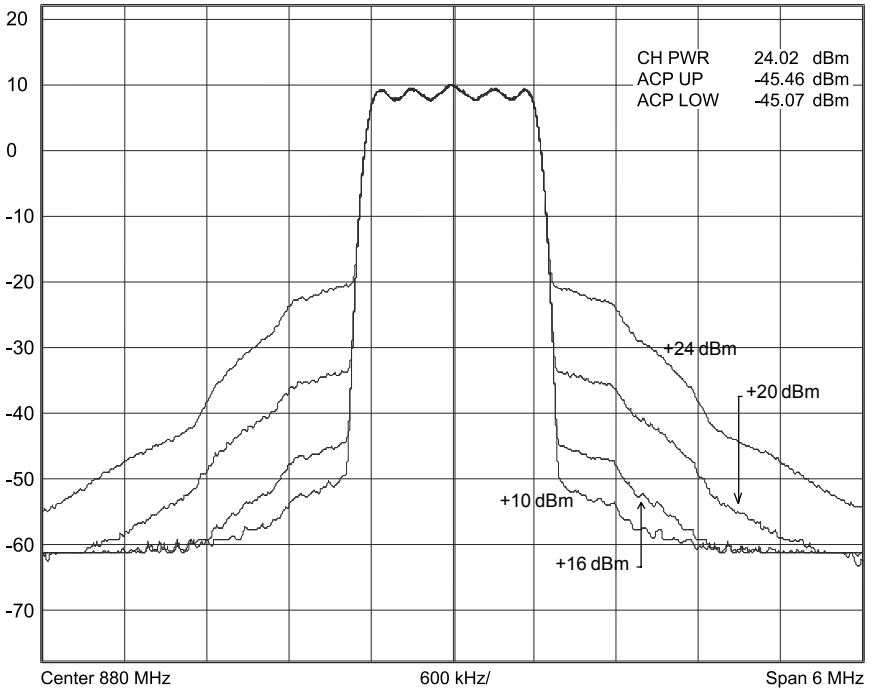


850-950 MHz Application Circuit Data, Icc=400mA, T=+25C, Vcc=5V, IS-95, 9 Channels Forward

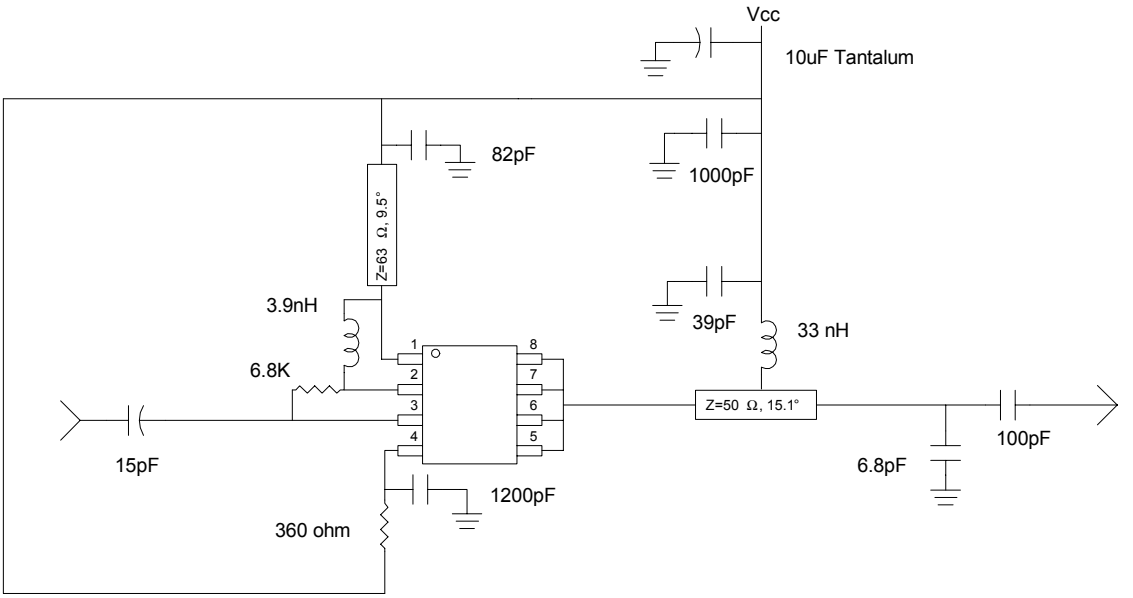
880 MHz Adjacent Channel Power vs. Channel Output Power



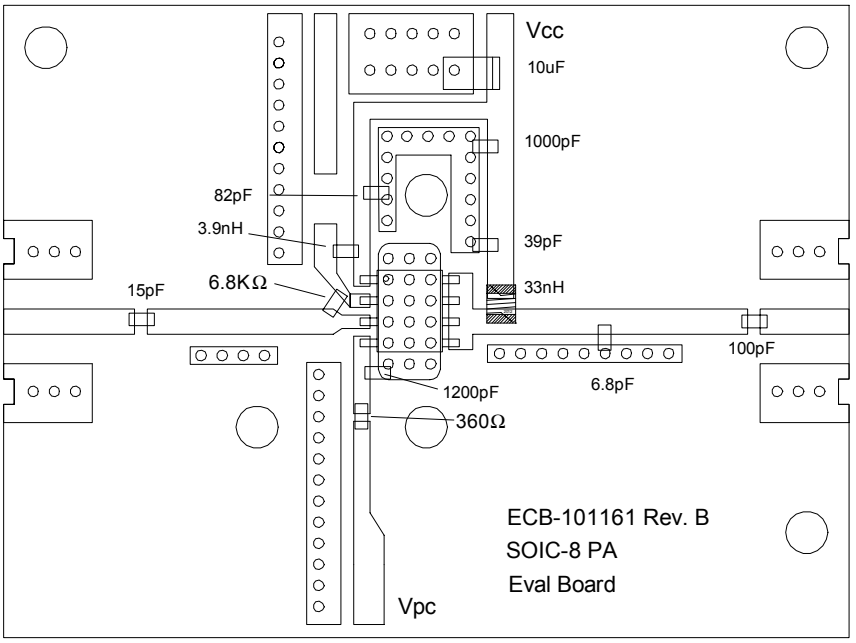
IS-95 CDMA at 880 MHz



850 - 950 MHz Schematic

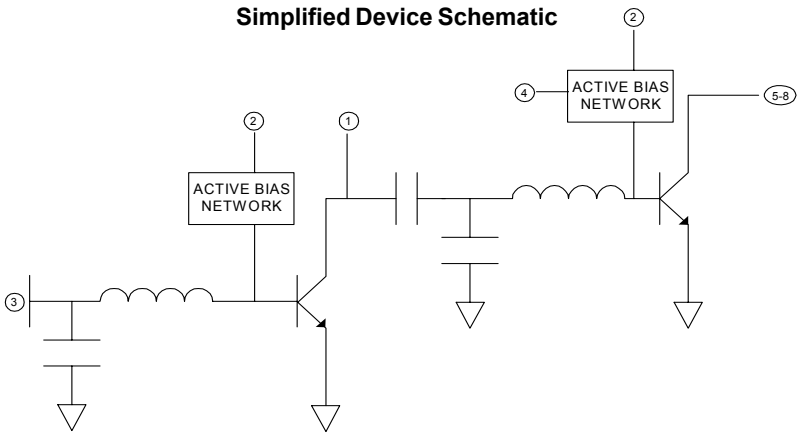


850 - 950 MHz Evaluation Board Layout



Pin #	Function	Description
1	Vc1	VC1 is the supply voltage for the first stage transistor. The configuration as shown on application schematic is required for optimum RF performance.
2	Vbias	Vbias is the bias control pin for the active bias network. Recommended configuration is shown in the Application Schematic.
3	RF In	RF input pin. This pin requires the use of an external DC blocking capacitor as shown in the Application Schematic.
4	Vpc2	Vpc2 is the bias control pin for the active bias network for the second stage. The recommended configuration is shown in the Application Schematic.
5, 6, 7, 8	RF Out/Vc2	RF output and bias pin. Bias should be supplied to this pin through an external RF choke. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed. An output matching network is necessary for optimum performance.
EPAD	Gnd	Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern (page 6).

Simplified Device Schematic



Absolute Maximum Ratings

Operation of this device above any one of these parameters may cause permanent damage.

Bias Conditions should also satisfy the following expression: $I_D V_D$ (max) < $(T_J - T_L)/R_{th,j-l}$

Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

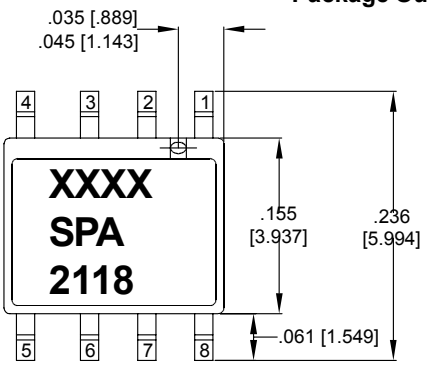
Parameter	Value	Unit
Supply Current (V_{C1})	150	mA
Supply Current (V_{C2})	750	mA
Device Voltage (V_D)	6.0	V
Power Dissipation	4.0	W
Operating Lead Temperature (T_L)	-40 to +85	°C
RF Input Power	+10	mW
Storage Temperature	-40 to +150	°C
Operating Junction Temperature (T_J)	+150	°C

SPA-2118 850 MHz 1 Watt Power Amp

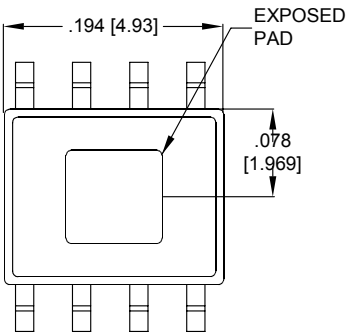
Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
SPA-2118	500	7"

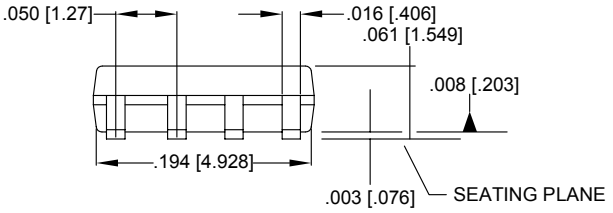
Package Outline Drawing



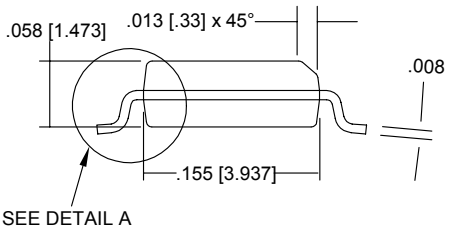
TOP VIEW



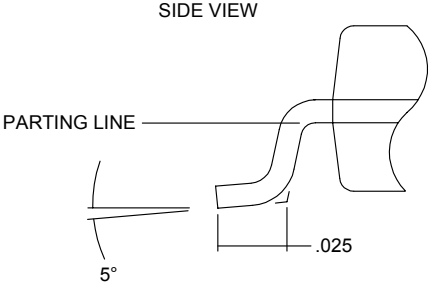
BOTTOM VIEW



SIDE VIEW

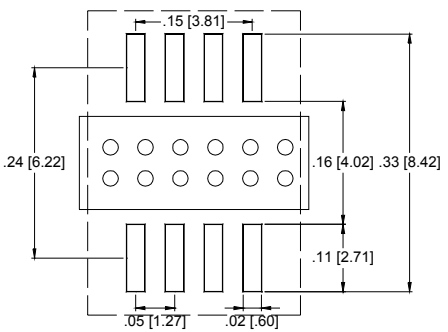


END VIEW



DETAIL A

Recommended Land Pattern



Note: Parts need to be baked prior to use as discussed in application note AN-029 (Special handling information for Exposed Pad ™ SOIC-8 products) to ensure no moisture is trapped in the encapsulated package. In production, this baking procedure is not necessary if parts are used within 48 hours of opening the sealed shipping materials.