

# M13 Multiplexer/Demultiplexer

## FEATURES

- Integrates a complete M13 multiplexer/demultiplexer in a single monolithic device.
- Integral framer supports the M23 or C-bit parity DS3 format with path maintenance datalink processing and bit-oriented code support for Far-End Alarm and Control (FEAC) channel termination.
- Supports either the M12 or the G.747 formats to allow DS1 or E1 signals to be multiplexed into a DS3 signal.
- Allows the M12 stages to be bypassed allowing direct input of DS2 signals.
- Generates an interrupt upon detection of various alarms, events, or changes in status. Identification of interrupt sources, masking of interrupt sources, and acknowledgement of interrupts is provided via internal registers.
- Application-compatible with the PM4351 COMET T1 Transceiver, PM4341A T1XC T1 Transceiver, PM4344 TQUAD Quad T1 Framer, PM4388 TOCTL Octal T1 Framer, PM6341 E1XC E1 Transceiver, PM6344 EQUAD Quad E1 Framer, PM6388 EOCTL Octal E1 Framer, PM4314 QDSX Quad E1/T1 LIU, and the PM7344 S/UNI®-MPH.
- Provides a generic 8-bit microprocessor interface for configuration, control, and status monitoring.
- Low power 5 V CMOS technology.
- Available in a high density (28 by 28 mm) 208-pin Plastic Quad Flat Pack (PQFP) package.

## DS3 FRAMER SECTION

- Detects/inserts DS3 Alarm Indication Signal (AIS) and Idle signal - operates correctly in the presence of 10-3 Bit Error Ratio (BER).
- Extracts/inserts the X,P,M,F,C and the stuff opportunity bits and serializes for optional external processing.
- Extracts/inserts the C-bit parity mode path maintenance datalink and serializes for optional external processing.
- Extracts/inserts the C-bit parity bit-oriented codes in the FEAC channel.
- Detects and accumulates EXcessive Zeros (EXZ), Loss Of Signal (LOS), Line Code Violations (LCVs) P-bit, F-bit, or M-bit errors, C-bit parity errors and Far-End Block Errors (FEBEs).
- Supports DS3 line loopback and DS3 diagnostic loopback modes to assist in fault isolation.

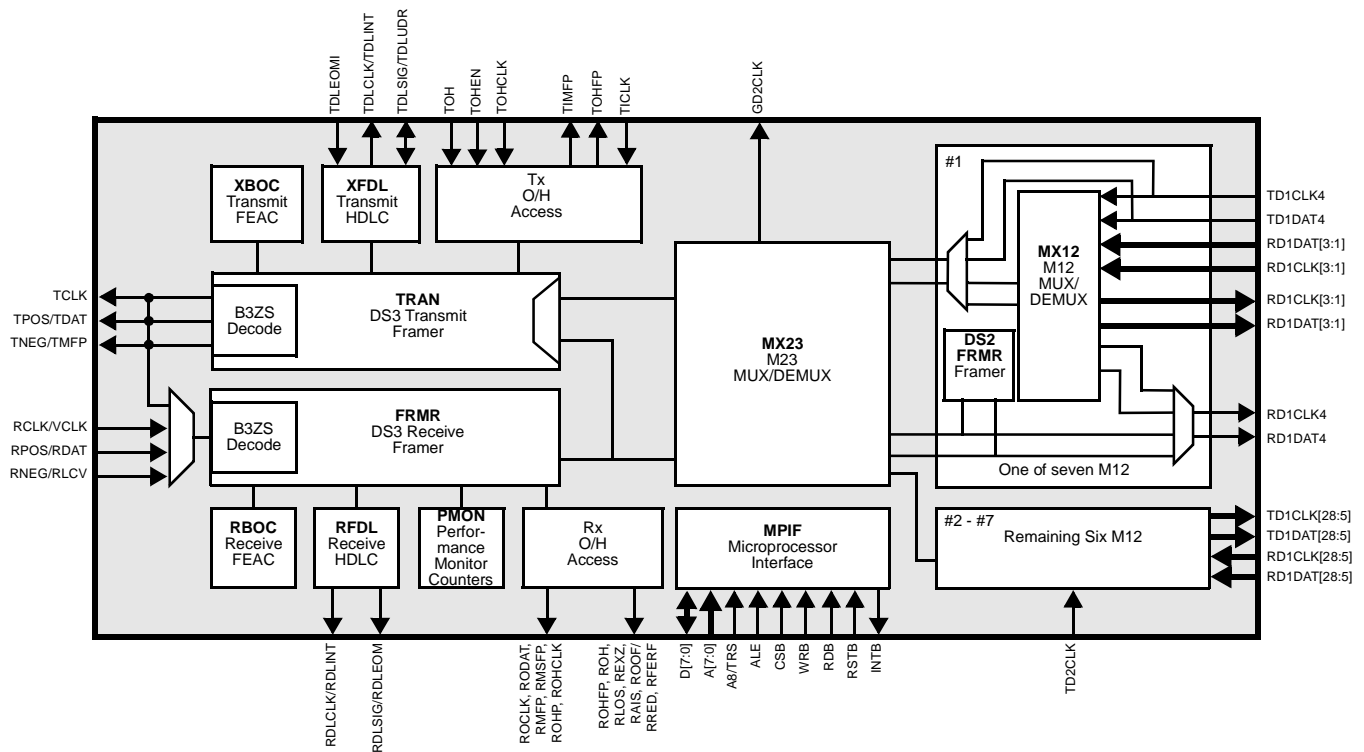
## M23 AND M12 MULTIPLEX/DEMULPLEX SECTIONS

- Supports combination of four DS1 bit streams or the combination of three E1 bit streams per G.747 into a single M12 stream.
- Supports per-DS2 payload loopback requests via C-bits or microprocessor control.
- Accumulates DS2 M-bit, F-bit, and G.747 framing bit/word error events.
- Supports DS2 AIS assertion based on DS3 LOF, or under microprocessor control.
- Supports DS2 tributary AIS activation/deactivation in either direction under microprocessor control.
- Inserts/detects per-DS1 payload loopback requests transmitted via C-bits.

## APPLICATIONS

- M23 or C-Bit Parity Format DS1 to DS3 Mux/Demux Equipment
- Fractional T3 Access Equipment
- DS2-to-DS3 Mux/Demux Equipment
- DS1-to-DS3 Mux/Demux Equipment Supporting G.747 Tributary Format

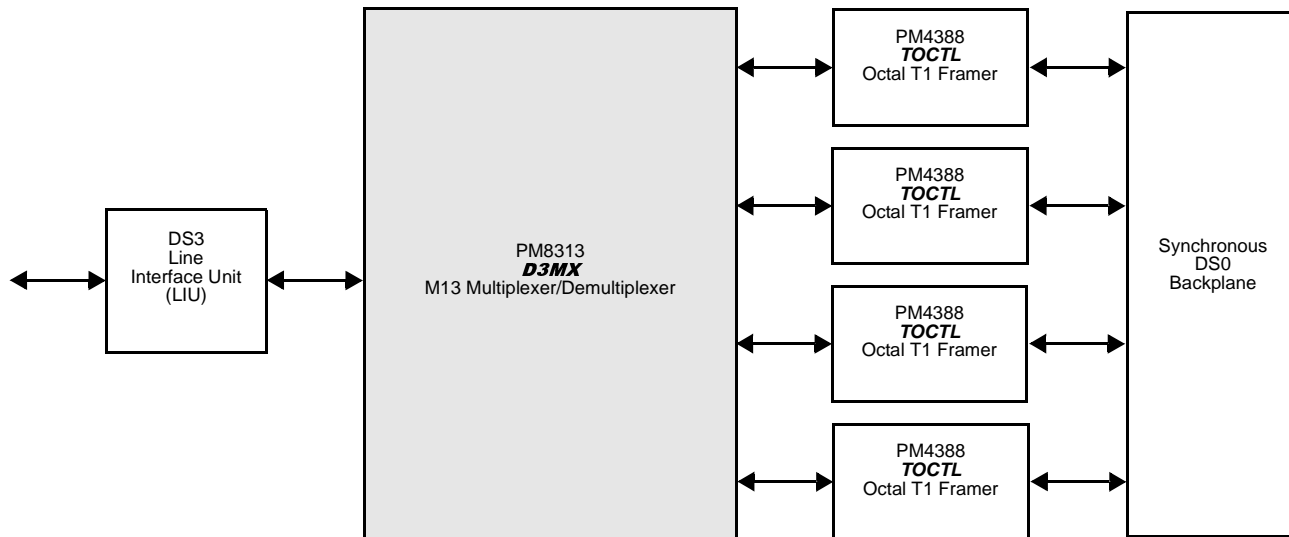
## BLOCK DIAGRAM



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## TYPICAL APPLICATIONS

### DS3 TERMINAL MULTIPLEXER OR DIGITAL CROSS-CONNECT



### HYBRID MULTIPLEXER-28xDS1 (ANSI FORMAT) OR 21xE1 (ITU G.747 FORMAT) TO DS3