XC61C Series

Low Voltage Detectors (VDF=0.9V~1.5V)

TOREX

◆**CMOS**
◆**Highly Accurate : ± 2%**
◆**Low Power Consumption : 0.7μA (VIN = 1.5V)**
◆**Ultra small SSOT-24 (SC-82) Package**

■General Description

The XC61C series are highly precise, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies. Detect voltage is extremely accurate with minimal temperature drift.
Both CMOS and N-channel open drain output configurations are available.

■Applications

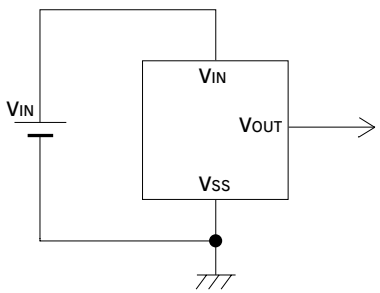
●Microprocessor reset circuitry
●Memory battery back-up circuits
●Power-on reset circuits
●Power failure detection
●System battery life and charge voltage monitors

■Features

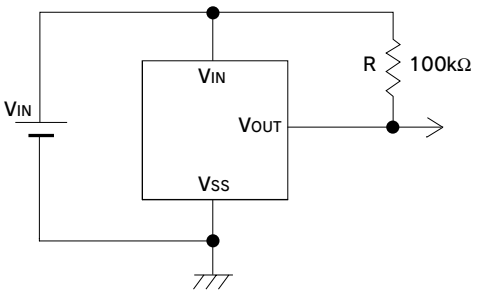
Highly accurate : ± 2%
Low power consumption : TYP 0.7 μA [VIN=1.5V]
Detect voltage range : 0.9V ~ 1.5V in 0.1V increments
Operating voltage range : 0.7V ~ 6.0V
Detect voltage temperature characteristics
: TYP± 100ppm/°C
Output configuration : N-channel open drain or CMOS
Ultra small package : SSOT-24 (150mW) super mini-mold
: SOT-23 (150mW) mini-mold
: SOT-89 (500mW) mini-power mold
: TO-92 (300mW)

Note : There are no products available with a set-up voltage accuracy of ± 1%.

■Typical Application Circuits



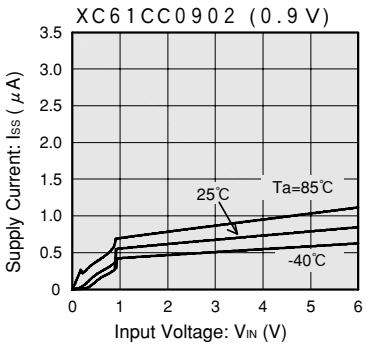
CMOS Output



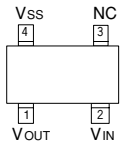
N-ch Open Drain Output

■Typical Performance Characteristic

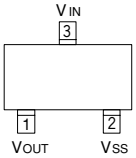
SUPPLY CURRENT vs. INPUT VOLTAGE



■Pin Configuration



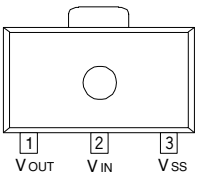
SSOT-24(SC-82)
(TOP VIEW)



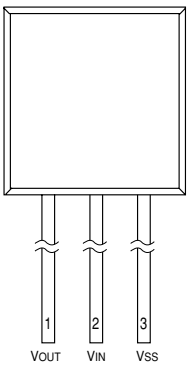
SOT-23
(TOP VIEW)

■Pin Assignment

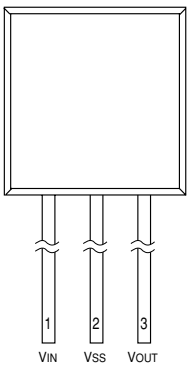
PIN NUMBER					PIN NAME	FUNCTION
SSOT-24	SOT-23	SOT-89	TO-92 (T)	TO-92 (L)		
2	3	2	2	1	VIN	Supply Voltage Input
4	2	3	3	2	VSS	Ground
1	1	1	1	3	VOUT	Output
3	-	-	-	-	NC	No Connection



SOT-89
(TOP VIEW)



TO-92 (T Type)
(TOP VIEW)



TO-92 (L Type)
(TOP VIEW)

■Product Classification

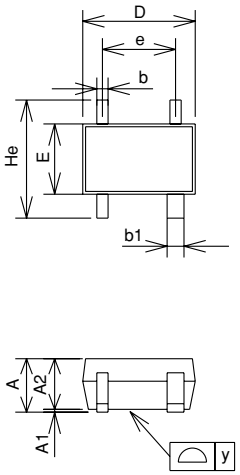
●Ordering Information

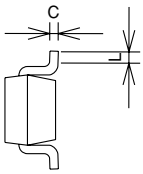
XC61C xx x x x x x
a b c d e f

DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	Output Configuration : C = CMOS N = N-ch open drain	e	Package Type: N = SSOT-24 (SC-82) M = SOT-23 P = SOT-89 T = TO-92 (Standard) L = TO-92 (Custom pin Configuration)
b	Detect Voltage : 09 = 0.9V 15 = 1.5V		
c	Output Delay : 0 = No delay	f	Device Orientation : R = Embossed Tape (Right) L = Embossed Tape (Left) H = Paper Type (TO-92) B = Bag (TO-92)
d	Detect Accuracy : 2 = within ±2.0%		

■Packaging Information

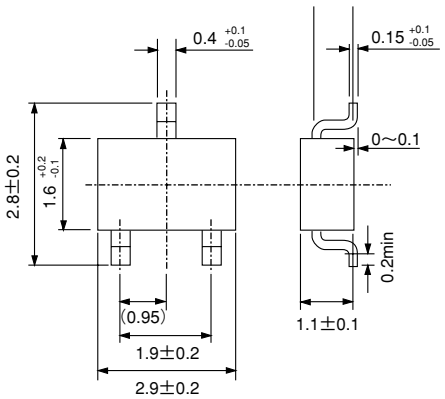
●SSOT-24 (SC-82)



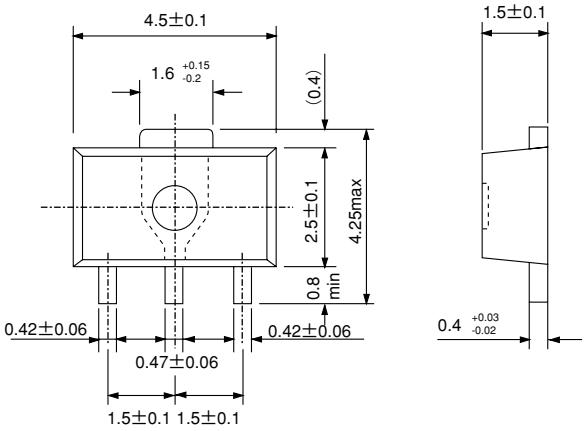


	SIZE mm		
	MIN	TYP	MAX
A	0.80	—	1.10
A1	0.00	—	0.10
A2	0.80	—	1.00
b	0.15	0.25	0.30
b1	0.25	0.35	0.40
C	0.075	0.125	0.225
D	1.80	2.00	2.20
E	1.15	1.25	1.45
He	1.80	2.10	2.40
e	1.10	1.30	1.50
L	0.10	0.30	—
y	—	—	0.10

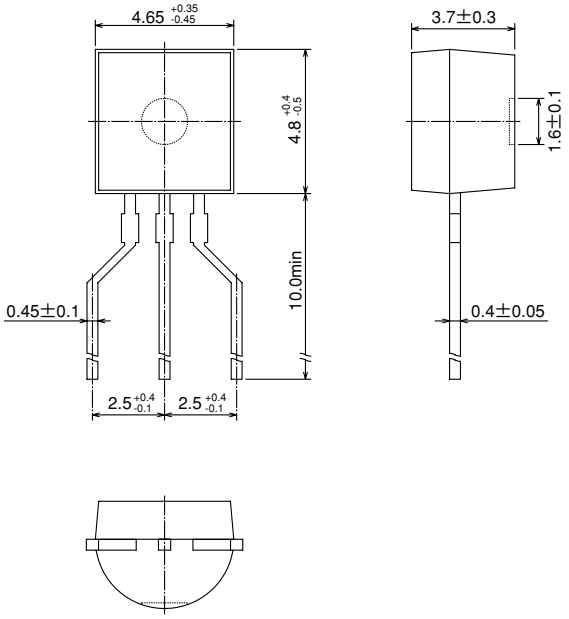
●SOT-23



●SOT-89

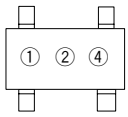

4.5±0.1
1.6 +0.15 -0.2
(0.4)
2.5±0.1
4.25max
0.8 min
0.42±0.06
0.42±0.06
0.47±0.06
1.5±0.1 1.5±0.1
1.5±0.1
0.4 +0.03 -0.02

●TO-92

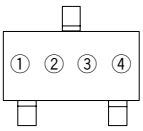

4.65 +0.35 -0.45
4.8 +0.4 -0.5
10.0min
0.45±0.1
2.5 +0.4 -0.1
2.5 +0.4 -0.1
3.7±0.3
1.6±0.1
0.4±0.05

■Marking

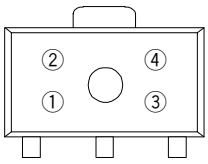
●SSOT-24, SOT-23, SOT-89



SSOT-24(SC-82)
(TOP VIEW)



SOT-23
(TOP VIEW)



SOT-89
(TOP VIEW)

① Represents the integer of the Output Voltage and Detect Voltage

CMOS Output (XC61CC series)

DESIGNATOR	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.②
B	CMOS	1.②

N-Channel Open Drain Output (XC61CN series)

DESIGNATOR	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.②
L	N-ch	1.②

② Represents the decimal number of the Detect Voltage

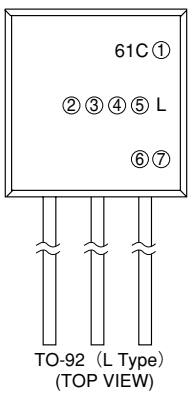
DESIGNATOR	VOLTAGE	DESIGNATOR	VOLTAGE
0	①.0	5	①.5
1	①.1	6	①.6
2	①.2	7	①.7
3	①.3	8	①.8
4	①.4	9	①.9

③ Based on internal standards
(SSOT-24 excepted)

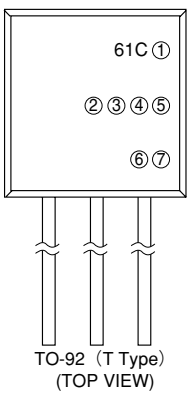
DESIGNATOR
3

④ Represents the assembly lot no.
Based on internal standards

●TO-92



TO-92（L Type）
(TOP VIEW)



TO-92（T Type）
(TOP VIEW)

① Represents the output configuration

DESIGNATOR	OUTPUT CONFIGURATION
C	CMOS
N	N-ch

② Represents the Detect Voltage

DESIGNATOR		VOLTAGE (V)
②	③	
0	9	0.9
1	5	1.5

④ Indicates Delay Time

DESIGNATOR	DELAY TIME
0	No delay

⑤ Represents the Detect Voltage Accuracy

DESIGNATOR	DETECT VOLTAGE ACCURACY
2	within ±2%

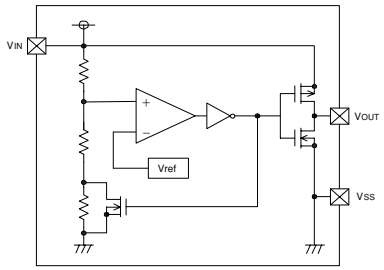
⑥ Represents a least significant digit of the produced year

DESIGNATOR	Produced year
0	2000
1	2001

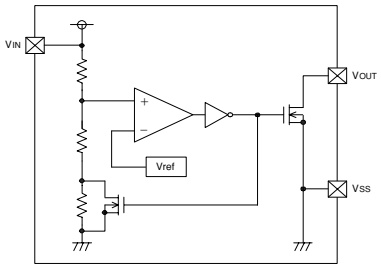
⑦ Denotes the production lot number
0 to 9, A to Z repeated(G.I.J.O.Q.W excepted)

■Block Diagram

(1) CMOS Output



(2) N-ch Open Drain Output



■Absolute Maximum Ratings

Ta = 25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		VIN	9	V
Output Current		IOUT	50	mA
Output Voltage	CMOS	VOUT	VSS -0.3 ~ VIN +0.3	V
	N-ch open drain		VSS -0.3 ~ 9	
Power Dissipation	SSOT-24	Pd	150	mW
	SOT-23		150	
	SOT-89		500	
	TO-92		300	
Operating Ambient Temperature		Topr	-40 ~ +85	°C
Storage Temperature		Tstg	-40 ~ +125	°C

■Electrical Characteristics

V_{DF} (T) = 0.9 to 1.5V ± 2%　　Ta = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage	V_{DF}		V_{DF} x 0.98	V_{DF}	V_{DF} x 1.02	V	1
Hysteresis Range	V_{HYS}		V_{DF} x 0.02	V_{DF} x 0.05	V_{DF} x 0.08	V	1
Supply Current	I_{SS}	V_{IN} = 1.5V		0.7	2.3	μA	2
		=2.0V		0.8	2.7		
		=3.0V		0.9	3.0		
		=4.0V		1.0	3.2		
		=5.0V		1.1	3.6		
Operating Voltage	V_{IN}	V_{DF}(T) = 0.9V to 1.5V	0.7		6.0	V	1
Output Current	I_{OUT}	N-ch V_{DS}=0.5V, V_{IN}=0.7V	0.1	0.8		mA	3
		N-ch V_{DS}=0.5V, V_{IN}=1.0V	0.85	2.7			
		P-ch V_{DS}=2.1V, V_{IN}=6.0V (with CMOS output)		-7.5	-1.5		4
Temperature Characteristics	$\frac{\Delta V_{DF}}{\Delta Topr \cdot V_{DF}}$	-40°C ≤ Topr ≤ 85°C		±100		ppm/°C	-
Delay Time (V_{DR}→V_{OUT} inversion)	tDLY				0.2	ms	5

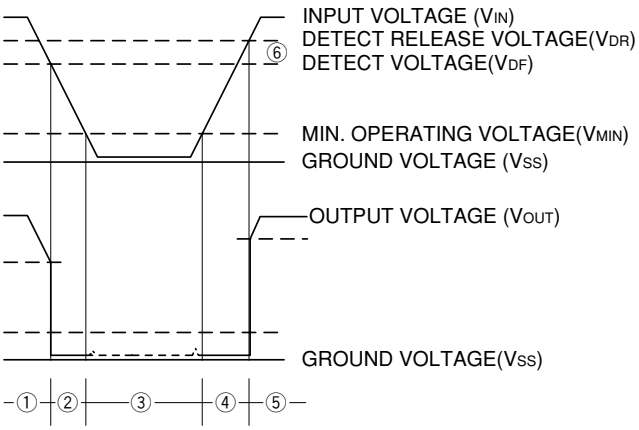
Note :
V_{DF} (T) : Established Detect Voltage Value
Release Voltage : V_{DR} = V_{DF} + V_{HYS}

■Functional Description

●Functional Description (CMOS output)

① When input voltage (V_{IN}) rises above detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to V_{IN}.
(A condition of high impedance exists with N-ch open drain output configurations.)
② When input voltage (V_{IN}) falls below detect voltage (V_{DF}), output voltage (V_{OUT}) will be equal to the ground voltage (V_{SS}) level.
③ When input voltage (V_{IN}) falls to a level below that of the minimum operating voltage (V_{MIN}), output will become unstable. In this condition, V_{IN} will equal the pulled-up output (should output be pulled-up.)
④ When input voltage (V_{IN}) rises above the ground voltage (V_{SS}) level, output will be unstable at levels below the minimum operating voltage (V_{MIN}). Between the V_{MIN} and detect release voltage (V_{DR}) levels, the ground voltage (V_{SS}) level will be maintained.
⑤ When input voltage (V_{IN}) rises above detect release voltage (V_{DR}), output voltage (V_{OUT}) will be equal to V_{IN}.
(A condition of high impedance exists with N-ch open drain output configurations.)
⑥ The difference between V_{DR} and V_{DF} represents the hysteresis range.

●Timing Chart



■Directions for use

●Notes on Use

1. Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at R_{IN} if load current (I_{OUT}) exists. (refer to the Oscillation Description (1) below)
3. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (I_{OUT}) does not exist. (refer to the Oscillation Description (2) below)
4. With a resistor connected between the V_{IN} pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{IN} pin.
5. In order to stabilise the IC's operations, please ensure that V_{IN} pin's input frequency's rise and fall times are more than several μ sec / V.
6. Please use N-ch open drains configuration, when a resistor R_{IN} is connected between the V_{IN} pin and power source.
   In such cases, please ensure that R_{IN} is less than 10kΩ and that C is more than 0.1 μF.

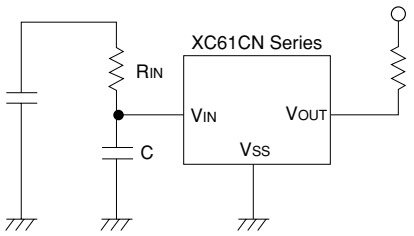


Diagram: Circuit using an input resistor

●Oscillation Description

(1) Output current oscillation with the CMOS output configuration

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (I_{OUT}) will flow at R_L. Because a voltage drop (R_{IN} x I_{OUT}) is produced at the R_{IN} resistor, located between the input (IN) and the V_{IN} pin, the load current will flow via the IC's V_{IN} pin. The voltage drop will also lead to a fall in the voltage level at the V_{IN} pin. When the V_{IN} pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at R_{IN} will disappear, the voltage level at the V_{IN} pin will rise and release operations will begin over again.

Oscillation may occur with this " release - detect - release " repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current

Since the XC61C series are CMOS IC s, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (R_{IN}) during release voltage operations. (refer to diagram 2)

Since hysteresis exists during detect operations, oscillation is unlikely to occur.

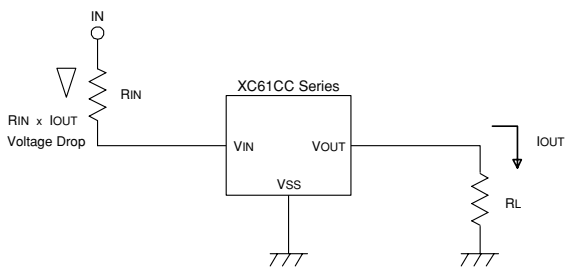


Diagram 1: Oscillation in relation to output current

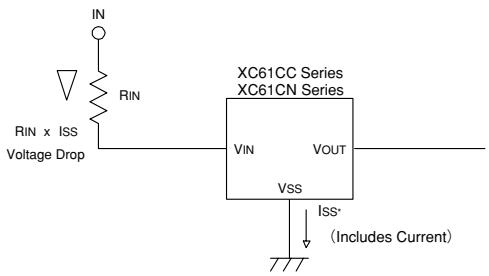
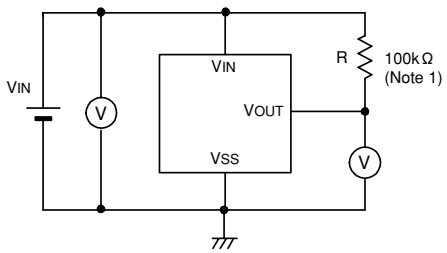


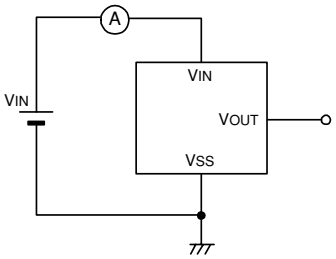
Diagram 2: Oscillation in relation to through current

■Measuring Circuits

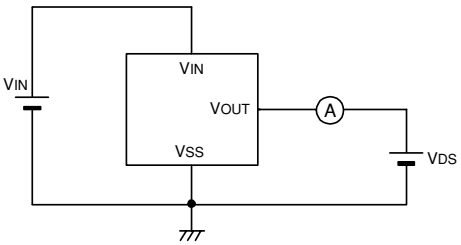
Circuit 1



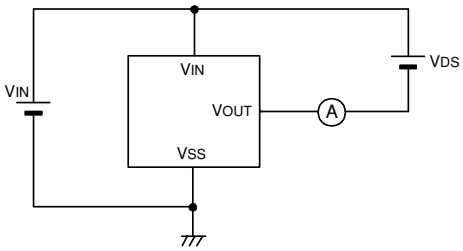
Circuit 2



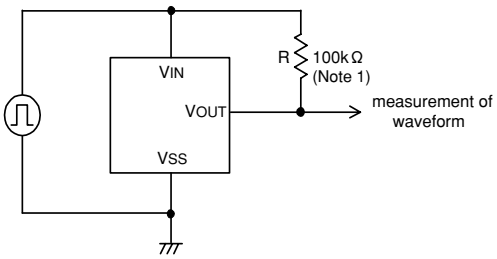
Circuit 3



Circuit 4



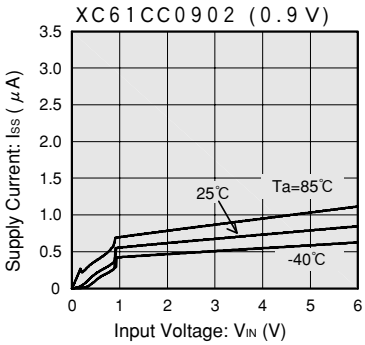
Circuit 5

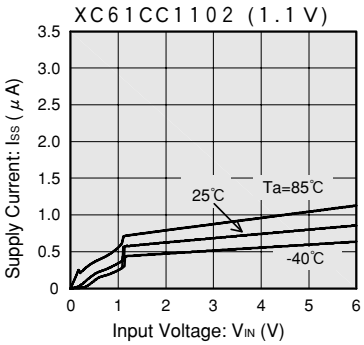


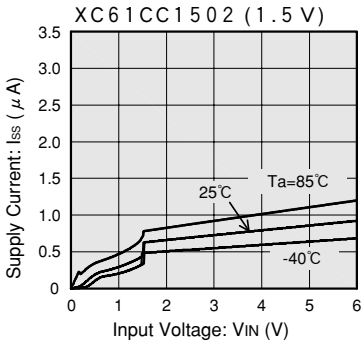
Note 1 : Not necessary with CMOS output products.

■Typical Performance Characteristics

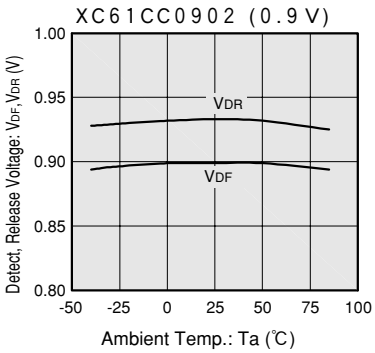
(1) SUPPLY CURRENT vs. INPUT VOLTAGE

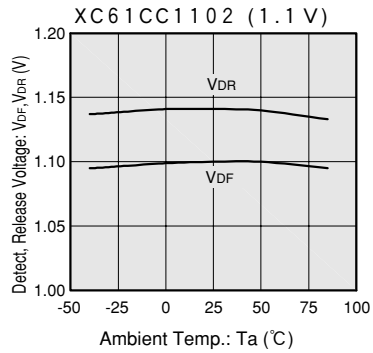


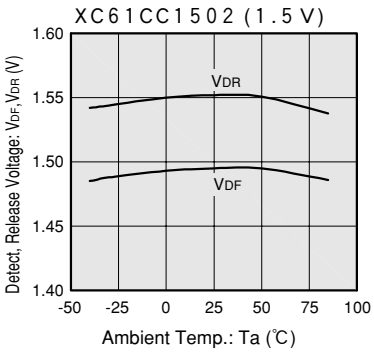




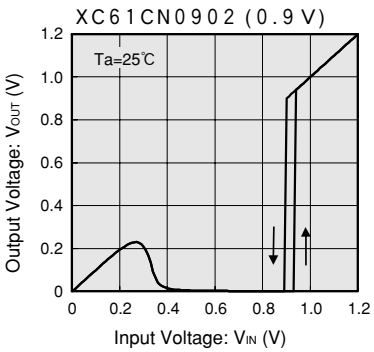
(2) DETECT, RELEASE VOLTAGE vs. AMBIENT TEMPERATURE

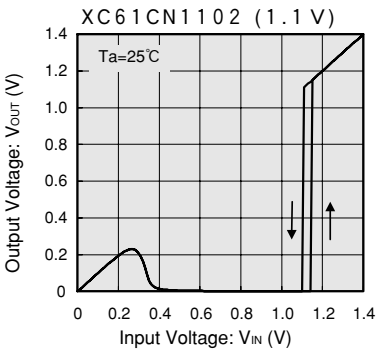


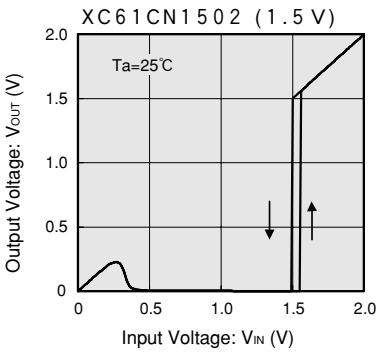




(3) OUTPUT VOLTAGE vs. INPUT VOLTAGE



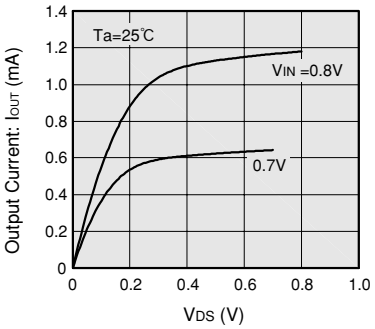




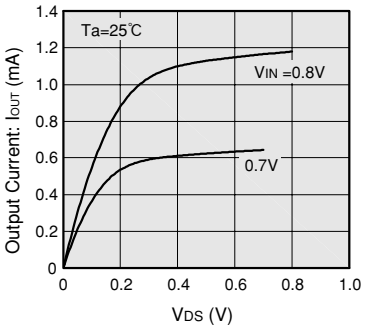
Note : The N-channel open drain pull up resistance value is 100kΩ

(4) N-ch DRIVER OUTPUT CURRENT vs. VDS

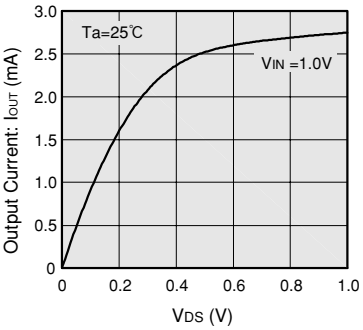
XC61CC0902 (0.9V)



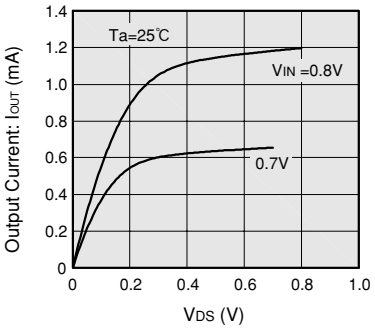
XC61CC1102 (1.1V)



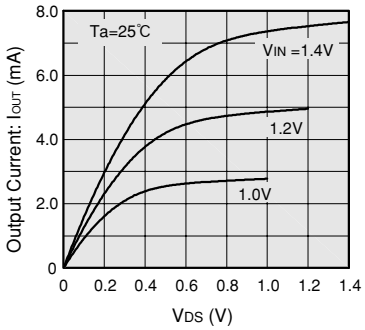
XC61CC1102 (1.1V)



XC61CC1502 (1.5V)

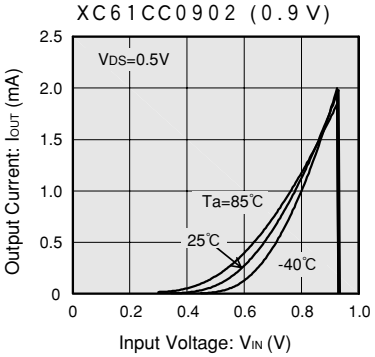


XC61CC1502 (1.5V)

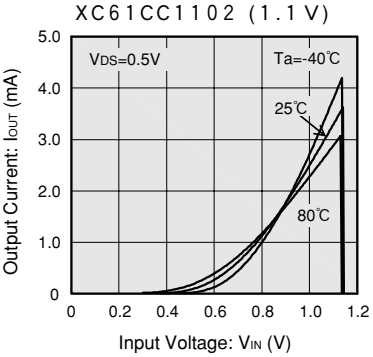


(5) N-ch DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE

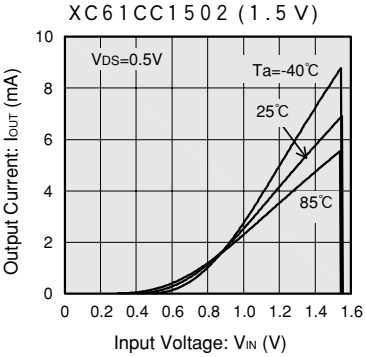
XC61CC0902 (0.9V)



XC61CC1102 (1.1V)

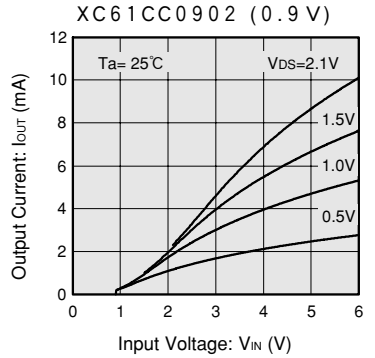


XC61CC1502 (1.5V)

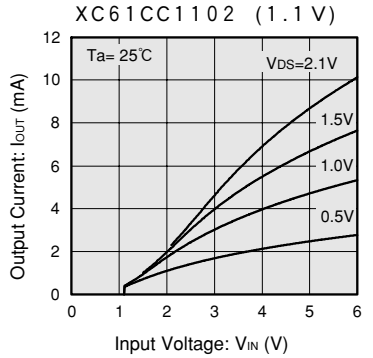


(6) P-ch DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE

XC61CC0902 (0.9V)



XC61CC1102 (1.1V)



XC61CC1502 (1.5V)