



Monolithic CMOS Analog Multiplexers

General Description

Maxim's DG506A and DG507A are monolithic CMOS analog multiplexers. The DG506A is a single 16 channel (1 of 16) multiplexer, and the DG507A is a differential 8 channel (2 of 16) multiplexer.

Both devices feature break-before-make switching. Maxim guarantees that these multiplexers will not latch-up if the power supplies are turned off with the input signals still present as long as absolute maximum ratings are not violated. The multiplexers operate over a wide range of power supplies from $\pm 4.5V$ to $\pm 18V$.

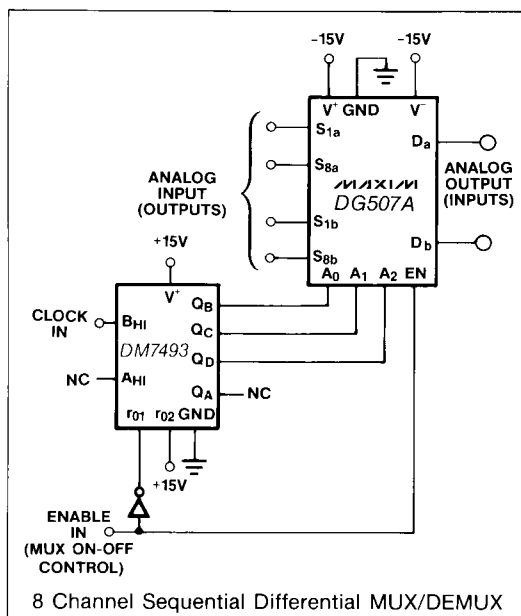
Compared to the original manufacturer's devices, Maxim's DG506A and DG507A consume significantly less power, making them ideal for portable equipment.

Maxim's DG506A and DG507A meet or exceed the specifications of, and are drop-in replacements for, Intersil's IH6116 and IH6216, Siliconix's DG506A and DG507A, and Harris' HI506 and HI507.

Applications

Control Systems
Data Logging Systems
Aircraft Heads Up Displays
Data Acquisition Systems
Signal Routing

Typical Operating Circuit



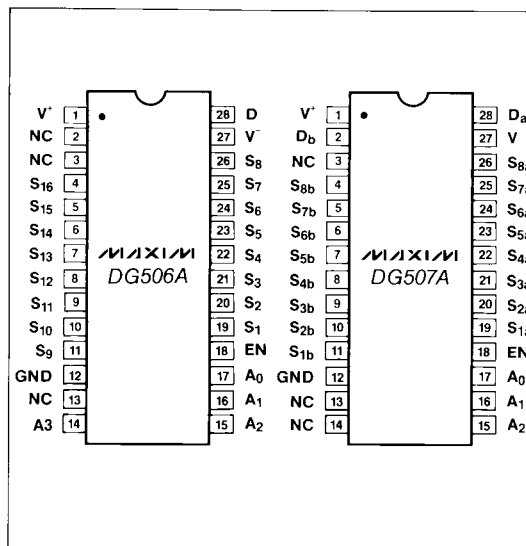
Features

- ◆ Improved 2nd Source!
- ◆ Pin compatible with Harris, Siliconix, Intersil
- ◆ Operable with $\pm 4.5V$ to $\pm 18V$ Supplies
- ◆ Symmetrical, Bi-Directional Operation
- ◆ Logic and Enable inputs, TTL and CMOS Compatible
- ◆ Latch-Up Proof Construction
- ◆ Monolithic, Low-Power CMOS Design

Ordering Information

PART	TEMP RANGE	PACKAGE
DG506AAK	-55°C to +125°C	28 Lead Cerdip
DG506ABK	-20°C to +85°C	28 Lead Cerdip
DG506AC/D	0°C to +70°C	Dice
DG506ACJ	0°C to +70°C	28 Lead Plastic DIP
DG506ACK	0°C to +70°C	28 Lead Cerdip
DG506ACWI	0°C to +70°C	28 Lead Wide SO
DG507AAK	-55°C to +125°C	28 Lead Cerdip
DG507ABK	-20°C to +85°C	28 Lead Cerdip
DG507AC/D	0°C to +70°C	Dice
DG507ACJ	0°C to +70°C	28 Lead Plastic DIP
DG507ACK	0°C to +70°C	28 Lead Cerdip
DG507ACWI	0°C to +70°C	28 Lead Wide SO

Pin Configurations



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DG506A/DG507A

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ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V ⁻		Operating Temperature (A Suffix)	-55°C to 125°C
V ⁺	44V	(B Suffix)	-25°C to 85°C
GND	25V	(C Suffix)	0°C to 70°C
Digital Inputs V _S , V _D (Note 1)	-2V to (V ⁺ + 2V) or 20mA, whichever occurs first.	Power Dissipation (Package)*	
Current, Any Terminal Except S or D	30mA	28 Pin Ceramic DIP**	1200mW
Continuous Current, S or D	20mA	28 Pin Plastic DIP***	625mW
Peak Current, S or D			
(Pulsed at 1msec, 10% duty cycle max)	40mA		
Storage Temperature (A & B Suffix)	-65°C to 150°C		
(C Suffix)	-65°C to 125°C		

*All leads soldered or welded to PC board.

**Derate 16mW/°C above 75°C

***Derate 8.3mW/°C above 75°C

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V⁺ = 15V, V⁻ = -15V, GND = 0V, T_A = 25°C, unless otherwise indicated.)

PARAMETER		SYMBOL	TEST CONDITIONS		DG506AA DG507AA			DG506AB/C DG507AB/C			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	
SWITCH											
Analog Signal Range		V _{ANALOG}			-15		15	-15		15	V
Drain-Source ON Resistance		r _{DS(on)}	Sequence Each Switch On V _{AL} = 0.8V, V _{AH} = 2.4V, V _{EN} = 2.4V	V _D = 10V, I _S = -200μA	270	400		270	450	Ω	
				V _D = -10V, I _S = -200μA	230	400		230	450		
Greatest Change in Drain-Source ON Resistance Between Channels			Δr _{DS(on)}	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}^{MAX} - r_{DS(on)}^{MIN}}{r_{DS(on)}^{AVE}} \right)$ -10V ≤ V _S ≤ 10V			6		6	%	
Source OFF Leakage Current		I _{S(off)}	V _{EN} = 0.8V V _{AL} = 0.8V	V _S = 10V, V _D = -10V	-1	0.002	1	-5	0.002	5	nA
				V _S = -10V, V _D = 10V	-1	-0.005	1	-5	-0.005	5	
Drain OFF Leakage Current	DG506A	I _{D(off)}		V _D = 10V, V _S = -10V	-10	0.02	10	-20	0.02	20	
				V _D = -10V, V _S = 10V	-10	-0.03	10	-20	-0.03	20	
	DG507A			V _D = 10V, V _S = -10V	-5	0.007	5	-10	0.007	10	
				V _D = -10V, V _S = 10V	-5	-0.015	5	-10	-0.015	10	
Channel ON Leakage Current	DG506A	I _{D(on)} ⁴	V _{S(all)} = V _D = 10V	-10	0.03	10	-20	0.03	20		
			V _{S(all)} = V _D = -10V	-10	-0.06	10	-20	-0.06	20		
	DG507A		V _{S(all)} = V _D = 10V	-5	0.015	5	-10	0.015	10		
			V _{S(all)} = V _D = -10V	-5	-0.03	5	-10	-0.03	10		
INPUT											
Address Input Current, Input Voltage High		I _{AH}	V _A = 2.4V	-10	-0.002		-10	-0.002		μA	
			V _A = 15V		0.006	10		0.006	10		
Address Input Current, Input Voltage Low		I _{AL}	All V _A = 0	V _{EN} = 2.4V	-10	-0.002		-10	-0.002		
				V _{EN} = 0	-10	-0.002		-10	-0.002		

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ELECTRICAL CHARACTERISTICS (Continued)

($V^+ = 15V$, $V^- = -15V$, GND = 0V, $T_A = 25^\circ C$, unless otherwise indicated.)

PARAMETER		SYMBOL	TEST CONDITIONS	DG506AA DG507AA			DG506AB/C DG507AB/C			UNITS
				MIN (Note 2)	TYP (Note 3)	MAX (Note 3)	MIN (Note 2)	TYP (Note 3)	MAX (Note 3)	
DYNAMIC										
Switching Time Of Multiplexer		t _{transition}	See Figure 1		0.6	1	0.6		μs	
Break-Before-Make Interval		t _{open}	See Figure 3		0.2		0.2			
Enable Turn-ON Time		t _{on(EN)}	See Figure 2		1		1			
Enable Turn-OFF Time		t _{off(EN)}			0.4		0.4			
OFF Isolation ²		OIRR	V _{EN} = 0, R _L = 1kΩ, C _L = 15pF V _S = 7Vrms, f = 500kHz		68		68		dB	
Source OFF Capacitance		C _{S(off)}	V _{EN} = 0, f = 140kHz	V _S = 0	6		6		pF	
Drain OFF Capacitance	DG506A	C _{D(off)}		V _D = 0	45		45			
	DG507A				23		23			
SUPPLY										
Positive Supply Current		I ⁺	V _{EN} = 0V or 5V, All V _A = 0		.13	.25	.13 .3		mA	
Negative Supply Current		I ⁻			-.15	-.07	-.25 -.07			

Note 1: Signals on S_X , D_X , or IN_X exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 4: $I_{D(\text{on})}$ is leakage from driver into "ON" switch.

Note 5: OFF isolation = $20 \log \frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S .

DG506A/DG507A

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ELECTRICAL CHARACTERISTICS (Over Temperature)

($V^+ = 15V$, $V^- = -15V$, GND = 0V, T_A = Over Temperature Range, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS		DG506AA DG507AA		DG506AB/C DG507AB/C		UNITS	
				MIN	TYP	MAX	MIN		TYP
(Note 2) (Note 3) (Note 2) (Note 3)									
SWITCH									
Analog Signal Range		V _{ANALOG}		-15	15	-15	15	V	
Drain-Source ON Resistance		r _{DS(on)}	Sequence Each Switch On V _{AL} = 0.8V, V _{AH} = 2.4V, V _{EN} = 2.4V	V _D = 10V, I _S = -200μA	500	550	Ω		
				V _D = -10V, I _S = -200μA	500	550			
Source OFF Leakage Current		I _{S(off)}	V _{EN} = 0.8V V _{AL} = 0.8V	V _S = 10V, V _D = -10V	-50	50	-50	50	nA
Drain OFF Leakage Current		I _{D(off)}		V _S = -10V, V _D = 10V	-50	50	-50	50	
				V _D = 10V, V _S = -10V	-300	300	-300	300	
				V _D = -10V, V _S = 10V	-300	300	-300	300	
				V _D = 10V, V _S = -10V	-200	200	-200	200	
				V _D = -10V, V _S = 10V	-200	200	-200	200	
Channel ON Leakage Current		DG506A	I _{D(on)} ⁴	Sequence Each Switch On V _{AL} = 0.8V, V _{AH} = 2.4V, V _{EN} = 2.4V	V _{S(alt)} = V _D = 10V	-300	300	-300	300
		DG507A			V _{S(alt)} = V _D = -10V	-300	300	-300	300
			V _{S(alt)} = V _D = 10V		-200	200	-200	200	
			V _{S(alt)} = V _D = -10V		-200	200	-200	200	
			V _{S(ALL)} = V _D = -10V		-200	200	-200	200	
INPUT									
Address Input Current, Input Voltage High		I _{AH}	V _A = 2.4V	-30	-30	μA			
			V _A = 15V	30	30				
Address Input Current, Input Voltage Low		I _{AL}	All V _A = 0	V _{EN} = 2.4V	-30	-30			
				V _{EN} = 0	30	30			

Note 1: Signals on S_X , D_X , or IN_X exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

Note 2: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

Note 3: Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Note 4: $I_{D(on)}$ is leakage from driver into "ON" switch.

Note 5: OFF isolation = $20 \log \frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S .

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DG506A/DG507A

Truth Tables

DG506A					
A ₃	A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG507A				
A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$
 "0" = DON'T CARE

Switching Time Test Circuit

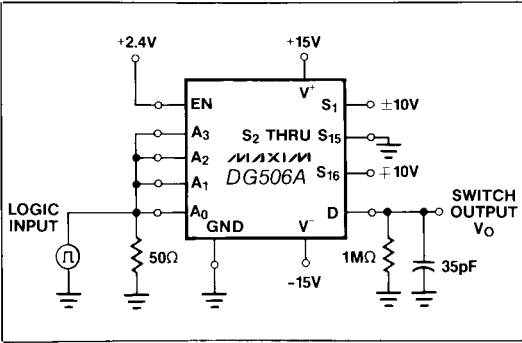


Figure 1A. Transition Switching Time

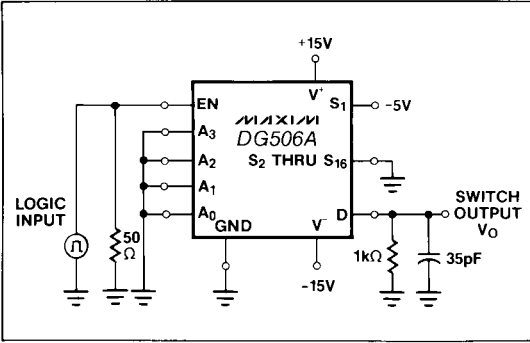


Figure 2A. Enable Switching Time

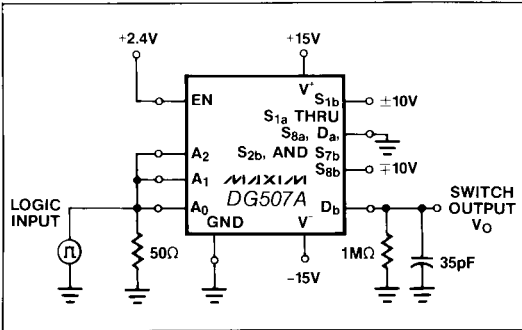


Figure 1B. Transition Switching Time

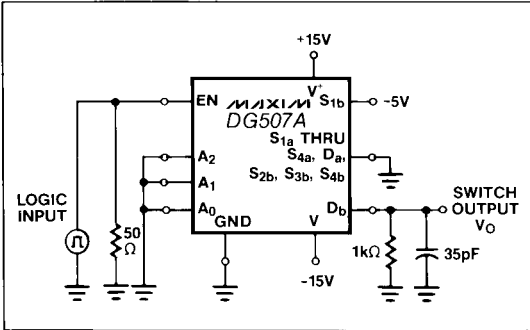


Figure 2B. Enable Switching Time

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Switching Time Test Circuit (continued)

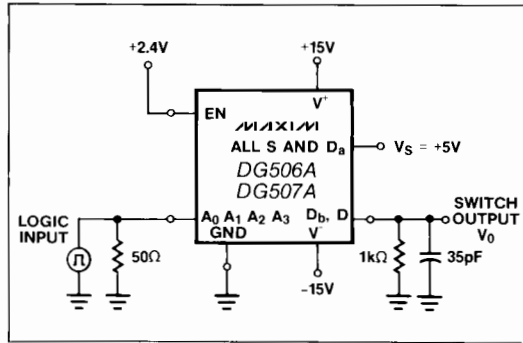


Figure 3. Break-Before-Make

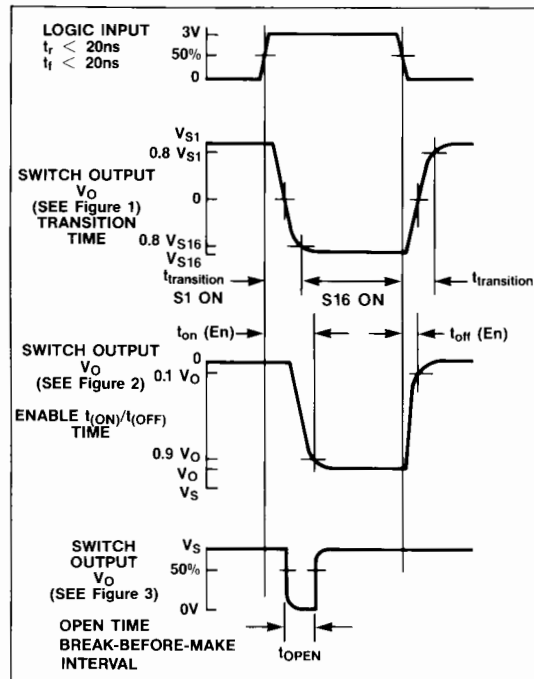
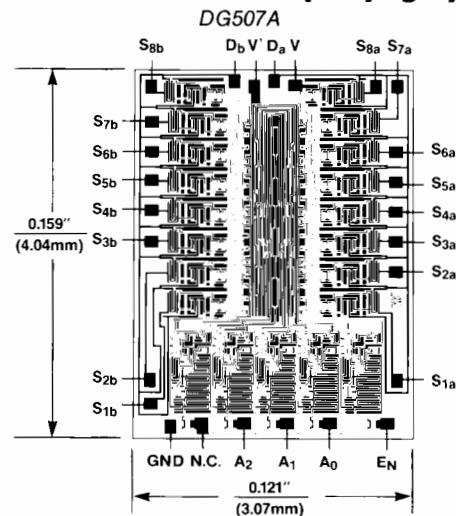
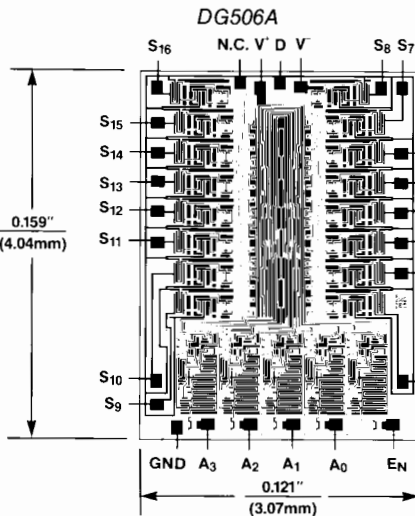


Figure 4. Timing Diagrams for Figures 1, 2, and 3

Chip Topography



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