

# MAXIM

## MAX1181 Evaluation Kit

### General Description

The MAX1181 Evaluation kit (EV Kit) is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the nonmultiplexed MAX1180–MAX1184 and MAX1190 or multiplexed MAX1185 and MAX1186, dual 10-bit analog-to-digital converters (ADC). The MAX1180–MAX1186 and MAX1190 accept differential or single-ended analog inputs and the EV kit allows for evaluation of each ADC with both types of signals from one single-ended analog signal. The digital output produced by the ADC can easily be sampled with a user-provided high-speed logic analyzer or data-acquisition system. The EV kit operates from 3.0V analog and 2.0V digital power supplies. It includes circuitry that generates a clock signal from an AC signal provided by the user. The EV kit comes with the MAX1181 installed. Order free samples of the pin-compatible MAX1180, MAX1182, MAX1183, MAX1184, MAX1185, MAX1186, or MAX1190 to evaluate these parts.

### Selector Guide

| PART       | SPEED (Msps)    |
|------------|-----------------|
| MAX1190ECM | 120             |
| MAX1180ECM | 105             |
| MAX1181ECM | 80              |
| MAX1182ECM | 65              |
| MAX1183ECM | 40              |
| MAX1184ECM | 20              |
| MAX1185ECM | 20, multiplexed |
| MAX1186ECM | 40, multiplexed |

### Features

- ◆ Up to 80Msps Sampling Rate (MAX1181)
- ◆ Low Voltage and Power Operation
- ◆ Single-Ended or Fully Differential Signal Input Configuration
- ◆ Clock-Shaping Circuit
- ◆ Fully Assembled and Tested
- ◆ Supports Both Nonmultiplexed (MAX1180–MAX1184/MAX1190) and Multiplexed (MAX1185/MAX1186) Output Operation

### Ordering Information

| PART         | TEMP RANGE   | IC PACKAGE |
|--------------|--------------|------------|
| MAX1181EVKIT | 0°C to +70°C | 48 TQFP-EP |

### Component List

| DESIGNATION                                                                           | QTY | DESCRIPTION                                                                                         |
|---------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------------------------|
| C1–C5, C7, C9, C11, C16–C19, C21, C23, C27, C31, C33, C34, C36–C39, C42–C49, C51, C52 | 32  | 0.1μF, 16V, X7R, ±10% ceramic capacitors (0603)<br>Taiyo Yuden EMK107BJ104KA or TDK C1608X7R1E104KT |
| C24, C25, C28, C29                                                                    | 4   | 22pF, 50V, ±5% ceramic capacitors (0603)<br>TDK C1608CCOG1H220JT                                    |
| C8, C10, C20, C22, C26, C32, C35, C40, C41                                            | 9   | 2.2μF, 10V tantalum capacitors (A)<br>AVX TAJA225K010 or Kemet T494A225K010AS                       |
| C30                                                                                   | 1   | 1000pF, 50V ±10% ceramic capacitor (0603)<br>TDK C1608X7R1H102KT                                    |

| DESIGNATION          | QTY | DESCRIPTION                                                                   |
|----------------------|-----|-------------------------------------------------------------------------------|
| C12–C15              | 4   | 10μF, 10V, tantalum capacitors (B)<br>AVX TAJB106M010 or Kemet T494B106K010AS |
| C6, C50              | 0   | Not installed (0603)                                                          |
| R1, R6, R19          | 0   | Not installed (0603)                                                          |
| R31–R33              | 0   | Not installed (0805)                                                          |
| R7                   | 1   | 0Ω ±5% resistor (0603)                                                        |
| R38                  | 1   | 3.9Ω ±5% resistor (0805)                                                      |
| R2–R5, R35, R51–R71  | 26  | 49.9Ω ±1% resistors (0603)                                                    |
| R15–R18              | 4   | 24.9Ω ±1% resistors (0603)                                                    |
| R8, R21–R30, R41–R50 | 21  | 100Ω ±1% resistors (0603)                                                     |

Component List continued on next page.

Evaluates: MAX1180–MAX1186/MAX1190



# MAX1181 Evaluation Kit

## Component List (continued)

| DESIGNATION                                         | QTY | DESCRIPTION                                                                                                                                    |
|-----------------------------------------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------|
| R9, R10, R13,<br>R14, R36                           | 5   | 2k $\Omega$ $\pm$ 1% resistors (0603)                                                                                                          |
| R11                                                 | 1   | 6.04k $\Omega$ $\pm$ 1% resistor (0603)                                                                                                        |
| R12, R37                                            | 2   | 4.02k $\Omega$ $\pm$ 1% resistors (0603)                                                                                                       |
| R20                                                 | 1   | 10k $\Omega$ $\pm$ 1% resistor (0603)                                                                                                          |
| R34                                                 | 1   | 5k $\Omega$ potentiometer, 12-turn, 1/4"<br>BI Technologies 3266W-1-502                                                                        |
| T1, T2                                              | 2   | RF transformers<br>Mini-Circuits TT1-6-KK81                                                                                                    |
| U1                                                  | 1   | MAX1181ECM (48-pin TQFP-EP)                                                                                                                    |
| U2                                                  | 1   | Dual CMOS differential line<br>receiver (8-pin SO)<br>Maxim MAX9113ESA                                                                         |
| U3, U4                                              | 2   | Buffer/Driver three-state outputs<br>(48-pin TSSOP)<br>Texas Instrument<br>SN74ALVCH16244DGG                                                   |
| L1, L2                                              | 2   | Ferrite chip beads, 90 $\Omega$ at<br>100MHz (1206), Fair-Rite<br>Products Corp.<br>2512069007Y0 or Mouser<br>436-2600 (60 $\Omega$ at 100MHz) |
| J1                                                  | 1   | 2 x 25-pin header                                                                                                                              |
| S/E_INA,<br>D/E_INA,<br>S/E_INB, D/E_<br>INB, CLOCK | 5   | SMA PC-mount connectors                                                                                                                        |
| JU1–JU8                                             | 8   | 3-pin headers                                                                                                                                  |
| None                                                | 8   | Shunt (JU1–JU8)                                                                                                                                |
| None                                                | 1   | MAX1181 PC board                                                                                                                               |
| None                                                | 1   | MAX1181 data sheet                                                                                                                             |
| None                                                | 1   | MAX1181 EV kit data sheet                                                                                                                      |

## Quick Start

Required equipment:

- DC power supplies  
Digital 2.0V, 100mA  
Analog 3.0V, 300mA
- Function generator with low-phase noise and low-jitter for clock input (e.g., HP8662A)
- Function generators for analog signal inputs (e.g., HP8662A)

## Component Suppliers

| SUPPLIER           | PHONE        | FAX          |
|--------------------|--------------|--------------|
| AVX                | 843-448-9411 | 843-448-1943 |
| Fair-Rite Products | 888-324-7748 | 888-337-7483 |
| Kemet              | 864-963-6300 | 864-963-6322 |
| Mini-Circuits      | 718-934-4500 | 718-934-7092 |
| Pericom            | 800-435-2336 | 408-435-1100 |
| Taiyo Yuden        | 800-348-2496 | 847-952-0899 |
| TDK                | 847-803-6100 | 847-803-6296 |
| Texas Instruments  | 972-644-5580 | 214-480-7800 |

**Note:** Please indicate that you are using the MAX1181 when contacting these component suppliers.

- Logic analyzer or data-acquisition system (e.g., HP16500C with HP16517A High-Speed Logic State Card)
- Analog bandpass filters (e.g., TTE Elliptical Bandpass Filter Q56 series)
- Digital voltmeter

The MAX1181 EV kit is a fully assembled and tested surface-mount board. Follow the steps below for board operation. **Do not turn on power supplies or enable function generators until all connections are complete.**

- 1) Verify that shunts are installed across pins 2 and 3 of jumpers JU5 (offset binary digital output), JU6 (normal operation), JU7 (MAX1181 operating), and JU8 (outputs enabled).
- 2) Connect the clock function generator to the CLOCK SMA connector.
- 3) Connect the output of the analog signal function generator to the input of the bandpass filter.
- 4) a) To evaluate differential analog signals on Channel A, verify that shunts are installed on pins 2 and 3 of jumpers JU1 and JU2. Connect the output of the analog bandpass filter to the D/E\_INA SMA connector. For single-ended analog signal evaluation on Channel A, verify that shunts are installed on pins 1 and 2 of jumpers JU1 and JU2, and connect the output of the bandpass filter to the S/E\_INA SMA connector.  
b) To evaluate differential analog signals on Channel B, verify that shunts are installed on pins 2 and 3 of jumpers JU3 and JU4. Connect the output of the analog bandpass filter to the D/E\_INB SMA connector. For single-ended analog signal evaluation on Channel B, verify that shunts are installed on pins 1 and 2 of jumper JU3 and JU4, and connect the output of the bandpass filter to the S/E\_INB SMA connector.

# MAX1181 Evaluation Kit

Evaluates: MAX1180-MAX1186/MAX1190

**Note:** Both input channels may be configured identically or differently.

- 5) Connect the logic analyzer to the square pin header (J1). Channel A (Channel B) data is captured on J1-1 (J1-23) through J1-19 (J1-41). If evaluating the multiplexed ADC (MAX1185 or MAX1186), the output data for Channel A and Channel B is captured on a single 10-bit bus (J1-1 through J1-19) and the A/B indicator signal can be monitored on J1-23 (see Table 4 for bit locations and J1 header designators). The system clock for both multiplexed and nonmultiplexed output operation is available on pin J1-43.
- 6) Connect a 3.0V, 300mA power supply to VA and VADUT. Connect the ground terminal of this supply to AGND.
- 7) Connect a 2.0V, 100mA power supply to VD and VDDUT. Connect the ground terminal of this supply to DGND.
- 8) Turn on both power supplies.
- 9) With a voltmeter, verify that 1.20V is measured across test points TP1 and TP2. If the voltage is not 1.20V, adjust potentiometer R34 until 1.20V is obtained.
- 10) Enable the function generators. Set the clock function generator for an output amplitude of 2.4V<sub>P-P</sub> and frequency ( $f_{CLK}$ )  $\leq$  80MHz. Set the analog input signal generators for an output amplitude  $\leq$  2V<sub>P-P</sub> and to the desired frequency. The two function generators should be phase-locked to each other.
- 11) Set the logic analyzer to capture on the clock's rising edge. In multiplexed output operation mode capture Channel A data on the falling edge and Channel B data on the rising edge of the logic analyzer clock.
- 12) Enable the logic analyzer.
- 13) Collect data using the logic analyzer.

## Detailed Description

The MAX1181 EV kit is a fully-assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX1180, MAX1181, MAX1182, MAX1183, MAX1184, MAX1185, MAX1186, or MAX1190, dual 10-bit ADCs (Channel A and Channel B). The MAX1180-MAX1184/MAX1190 dual outputs (Channel A and Channel B) are nonmultiplexed and the data is captured with two separate 10-bit buses. The MAX1185 and MAX1186 dual outputs (Channel A and Channel B) are multiplexed and data is captured with a single 10-bit bus. The EV kit comes with the MAX1181 which can be evaluated with a maximum clock frequency

( $f_{CLK}$ ) of 80MHz. The MAX1181 accepts differential or single-ended analog input signals. With the proper board configuration (as specified below), the ADC can be evaluated with both types of signals by supplying only one single-ended analog signal to the EV kit.

The EV kit was designed as a four-layer PC board to optimize the performance of the MAX1181. Separate analog and digital power planes minimize noise coupling between analog and digital signals. For simple operation, the EV kit is specified to have 3.0V and 2.0V DC power supplies applied to analog and digital power planes, respectively. However, the digital plane can be operated down to 1.7V without compromising the board's performance. The logic analyzer's threshold must be adjusted accordingly.

Access to Channel A and Channel B outputs is provided through connector J1. The 50-pin connector interfaces directly with a user-provided logic analyzer or data acquisition system.

## Power Supplies

The MAX1181 EV kit requires separate analog and digital power supplies for best performance. A 3.0V power supply is used to power the analog portion of the MAX1181 and the clock signal circuit. The MAX1181 analog supply voltage has a range of 2.7V to 3.6V, however, 3.0V must be supplied to the EV kit (VADUT, VA) to meet the minimum input voltage supply to the clock shaping circuit. A separate 2.0V power supply is used to power the digital portion (VDDUT, VD) of the MAX1181 and the buffer/driver. It will operate with a voltage supply as low as 1.7V and as high as 3.6V. Enhanced dynamic performance is normally achieved when the digital supply voltage is lower than the analog supply voltage.

## Clock

An on-board clock-shaping circuit generates a clock signal from an AC sine-wave signal applied to the CLOCK SMA connector. The input signal should not exceed a magnitude of 2.6V<sub>P-P</sub>. The frequency of the signal should not exceed 80MHz for the MAX1181. The frequency of the sinusoidal input signal determines the sampling frequency ( $f_{CLK}$ ) of the ADC. A differential line receiver (U2) processes the input signal to generate the CMOS clock signal. The signal's duty cycle can be adjusted with potentiometer R34. A clock signal with a 50% duty cycle (recommended) can be achieved by adjusting R34 until 1.20V is produced across test points TP1 and TP2, when the analog voltage supply is set to 3.0V (40% of the analog power supply). The clock signal is available at the J1-J43 pin (CK), which can be used to synchronize the output signal to the logic analyzer.

# MAX1181 Evaluation Kit

## Input Signal

The MAX1181 accepts differential or single-ended analog input signals applied to Channels A or B. The EV kit requires only single-ended analog input signals, with an amplitude of less than 2V<sub>p-p</sub> provided by the user. During single-ended operation the signal is applied directly to the ADC, while in differential mode, an on-board transformer takes the single-ended analog input and generates a differential analog signal at the ADCs differential input pins. To evaluate single-ended signal input, connect the input signal to the S/E\_INA (Channel A) or S/E\_INB (Channel B) SMA connectors. To evaluate differential signals, connect the input signal to the D/E\_INA (Channel A) or D/E\_INB (Channel B) SMA connectors. For single-ended or differential operation, see Table 1 for jumper configuration.

**Note:** When a differential signal is applied to the ADC, the positive and negative input pins of the ADC each receive half of the input signal supplied at SMA connector D/E\_INA(D/E\_INB) centered at the common mode voltage of VADUT/2.

## Output Enable/Power-Down/Sleep Modes

The MAX1181 EV kit also features jumpers that allow the user to enable or disable certain functions or the entire data converter. Jumper JU6 controls the Sleep mode, jumper JU7 controls a full power-down mode, and jumper JU8 controls the outputs enable/disable mode. Operating the ADC in these modes supports the reduction of the IC's overall power consumption. Refer to Table 2 to configure the board and operate the ADC in these modes.

**Table 1. Single-Ended/Differential Operation Jumper Configuration**

| JUMPER   | SHUNT STATUS | PIN CONNECTION                                                                | EV KIT OPERATION                                                              |
|----------|--------------|-------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| JU1, JU2 | 1 and 2      | INA+ pin connected to SMA connector S/E_INA and INA- pin connected to COM pin | Analog input signal is applied to the ADC's Channel A as a single-ended input |
|          | 2 and 3      | INA+ and INA- pins connected to transformer T1                                | Analog input signal is applied to Channel A as a differential input           |
| JU3, JU4 | 1 and 2      | INB+ pin connected to SMA connector S/E_INB and INB- pin connected to COM pin | Analog input signal is applied to the ADC's Channel B as a single-ended input |
|          | 2 and 3      | INB+ and INB- pins connected to transformer T2                                | Analog input signal is applied to Channel B as a differential input           |

**Table 2. Output Enable/Power-Down/Sleep Mode Configuration**

| JUMPER | SHUNT STATUS | PIN CONNECTION                     | EV KIT OPERATION                                      |
|--------|--------------|------------------------------------|-------------------------------------------------------|
| JU6    | 1 and 2      | SLEEP connected to VDDUT           | MAX1181 is disabled except for the internal reference |
|        | 2 and 3      | SLEEP connected to DGND            | MAX1181 in normal operation mode                      |
| JU7    | 1 and 2      | PD connected to VDDUT              | MAX1181 is powered down                               |
|        | 2 and 3      | PD connected to DGND               | MAX1181 in normal operation mode                      |
| JU8    | 1 and 2      | $\overline{OE}$ connected to VDDUT | Digital outputs disabled                              |
|        | 2 and 3      | $\overline{OE}$ connected to DGND  | Digital output enabled                                |

# MAX1181 Evaluation Kit

Evaluates: MAX1180-MAX1186/MAX1190

## Reference Voltage

The MAX1181 requires an input voltage reference at its REFIN pin to set the full-scale analog signal voltage input. The ADC has a stable on-chip voltage reference of 2.048V that can be accessed at REFOUT. The EV kit was designed to use the on-chip voltage reference by connecting REFIN to REFOUT through resistor R20. The user can externally adjust the reference level, and hence the full-scale range, by installing a resistor at the R19 pad. The adjusted reference level can be calculated by applying the following equation:

$$V_{\text{REFIN}} = \left( \frac{R19}{R19 + R20} \right) \times V_{\text{REFOUT}}$$

where R19 is the value of the resistor installed, R20 is a 10kΩ resistor, and VREFOUT is 2.048V. Alternatively, the user can apply a stable, low noise, external voltage reference directly at the REFIN pad to set the full scale.

## Output Signal

The MAX1181 features two 10-bit, parallel, CMOS-compatible, digital outputs channels (Channels A and B). The digital output coding can be chosen to be either in two's complement format or straight offset binary format by configuring jumper JU5. Refer to Table 3 for jumper configuration. Two drivers buffer the ADC's Channel A and B digital outputs. The buffer is able to drive large capacitive loads, which may be present at the logic analyzer connection, without compromising the digital output signal. The outputs of the buffers are connected to a 50-pin header (J1) located on the right side of the EV kit, where the user can connect a logic analyzer or data-acquisition system. Refer to Table 4 for channel and bit location on header J1.

**Table 3. Output Format**

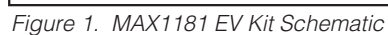
| JUMPER | SHUNT STATUS | PIN CONNECTION         | EV KIT OPERATION                         |
|--------|--------------|------------------------|------------------------------------------|
| JU5    | 1 and 2      | T/B connected to VDDUT | Digital output in two's complement       |
|        | 2 and 3      | T/B connected to DGND  | Digital output in straight offset binary |

**Table 4. Output Bit Location (Nonmultiplexed/Multiplexed Output Operation)**

| CHANNEL                                | A/B STATE  | BIT D0      | BIT D1      | BIT D2      | BIT D3      | BIT D4      | BIT D5      | BIT D6      | BIT D7      | BIT D8      | BIT D9      |
|----------------------------------------|------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| <b>NONMULTIPLEXED OUTPUT OPERATION</b> |            |             |             |             |             |             |             |             |             |             |             |
| <b>A</b><br>CLK ↑                      | N/A        | J1-19<br>A0 | J1-17<br>A1 | J1-15<br>A2 | J1-13<br>A3 | J1-11<br>A4 | J1-9<br>A5  | J1-7<br>A6  | J1-5<br>A7  | J1-3<br>A8  | J1-1<br>A9  |
| <b>B</b><br>CLK ↑                      | N/A        | J1-23<br>B0 | J1-25<br>B1 | J1-27<br>B2 | J1-29<br>B3 | J1-31<br>B4 | J1-33<br>B5 | J1-35<br>B6 | J1-37<br>B7 | J1-39<br>B8 | J1-41<br>B9 |
| <b>MULTIPLEXED OUTPUT OPERATION*</b>   |            |             |             |             |             |             |             |             |             |             |             |
| <b>A</b><br>CLK ↓                      | J1-23<br>1 | J1-19<br>A0 | J1-17<br>A1 | J1-15<br>A2 | J1-13<br>A3 | J1-11<br>A4 | J1-9<br>A5  | J1-7<br>A6  | J1-5<br>A7  | J1-3<br>A8  | J1-1<br>A9  |
| <b>B</b><br>CLK ↑                      | J1-23<br>0 | J1-19<br>A0 | J1-17<br>A1 | J1-15<br>A2 | J1-13<br>A3 | J1-11<br>A4 | J1-9<br>A5  | J1-7<br>A6  | J1-5<br>A7  | J1-3<br>A8  | J1-1<br>A9  |

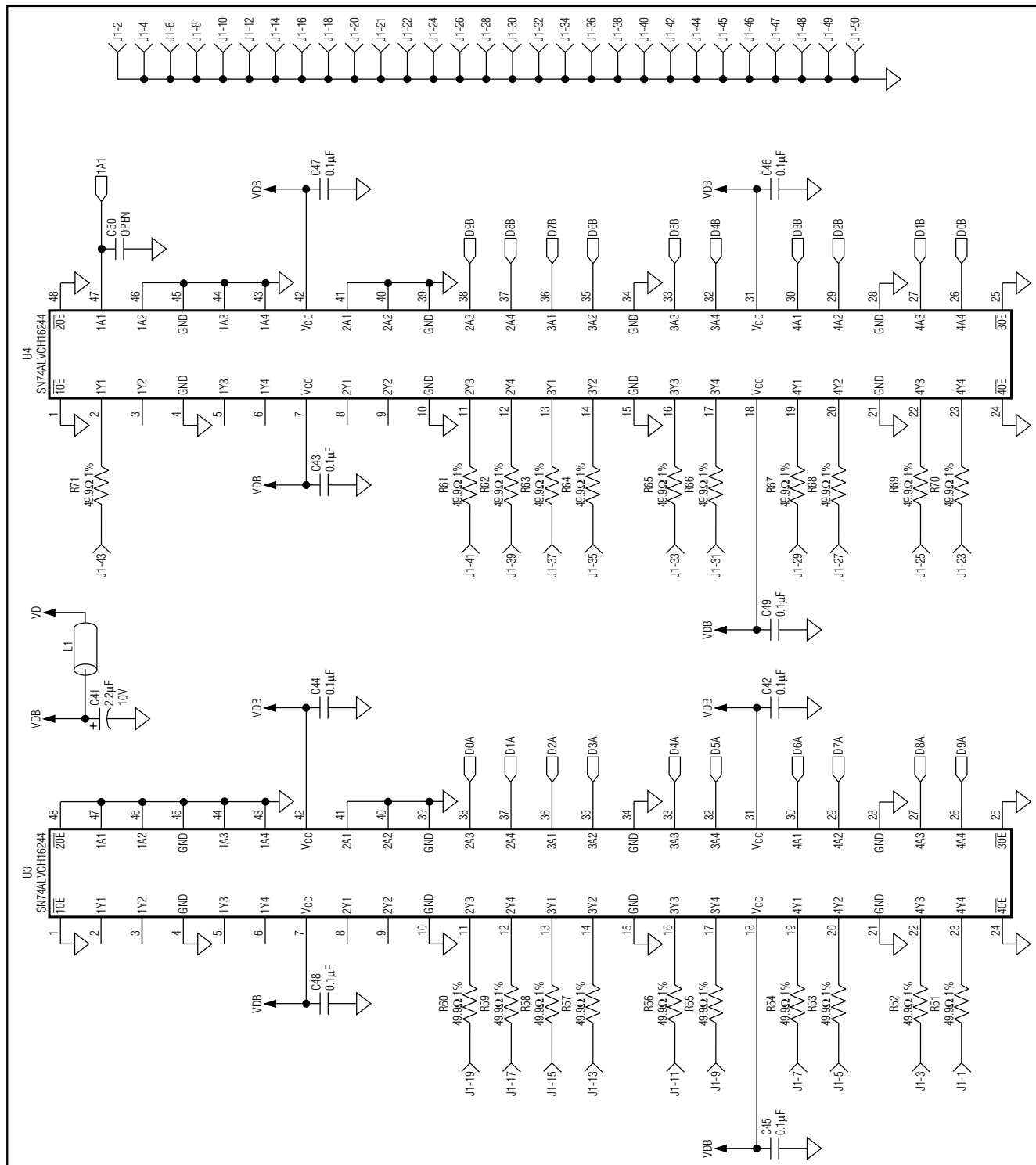
\*For multiplexed output operation, Channel A and Channel B data is captured with a single 10-bit bus. Leave header designators J25 (B1) through J41 (B9) open.

# MAX1181 Evaluation Kit



# MAX1181 Evaluation Kit

Evaluates: MAX1180-MAX1186/MAX1190



# MAX1181 Evaluation Kit

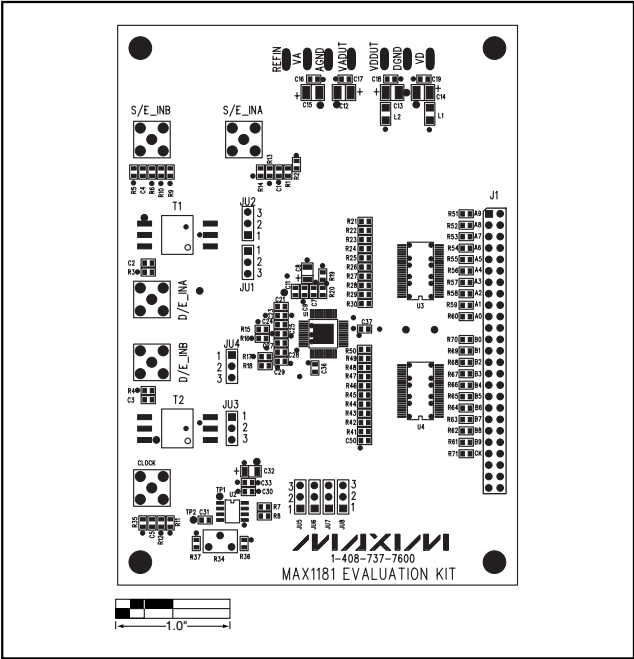


Figure 3. MAX1181 EV Kit Component Placement Guide—Component Side

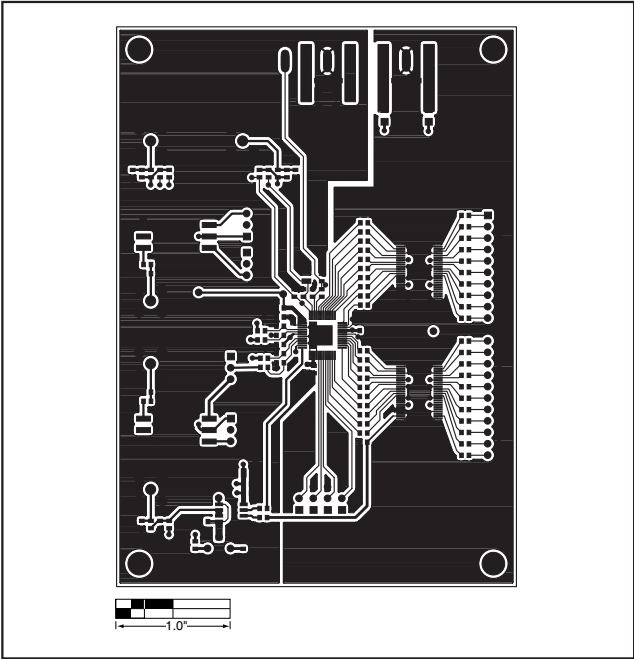


Figure 4. MAX1181 EV Kit PC Board Layout—Component Side

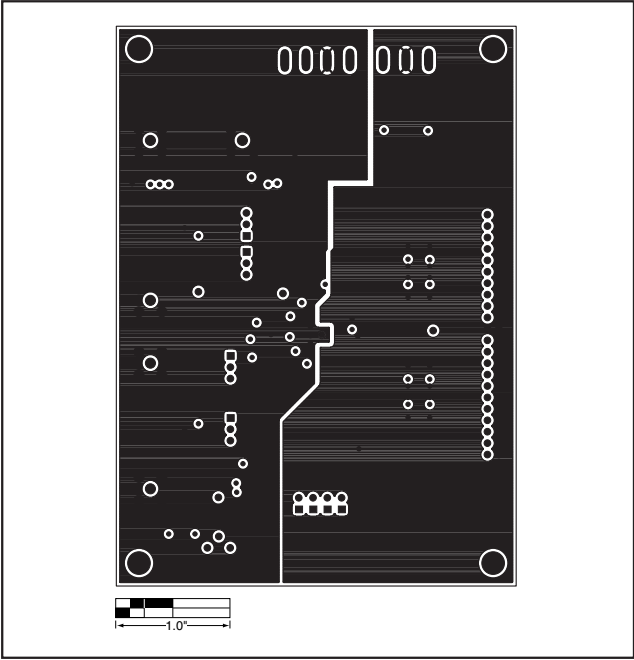


Figure 5. MAX1181 EV Kit PC Board Layout—Ground Planes

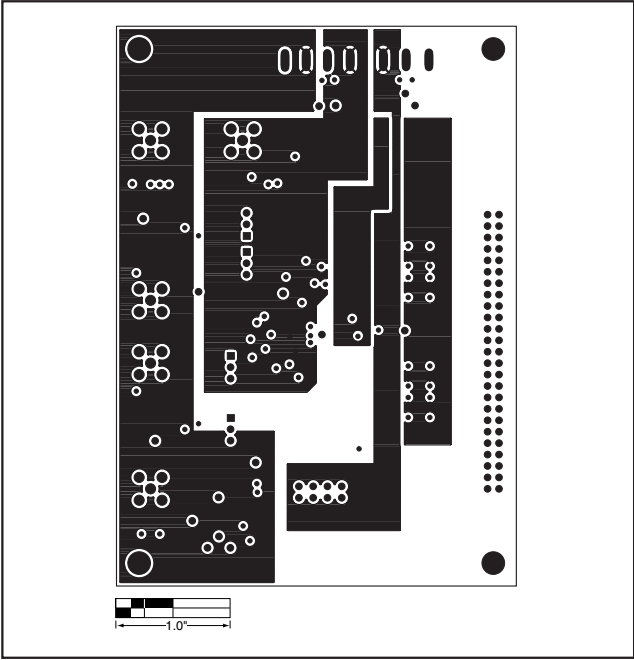


Figure 6. MAX1181 EV Kit PC Board Layout—Power Planes



# MAX1181 Evaluation Kit

Evaluates: MAX1180-MAX1186/MAX1190

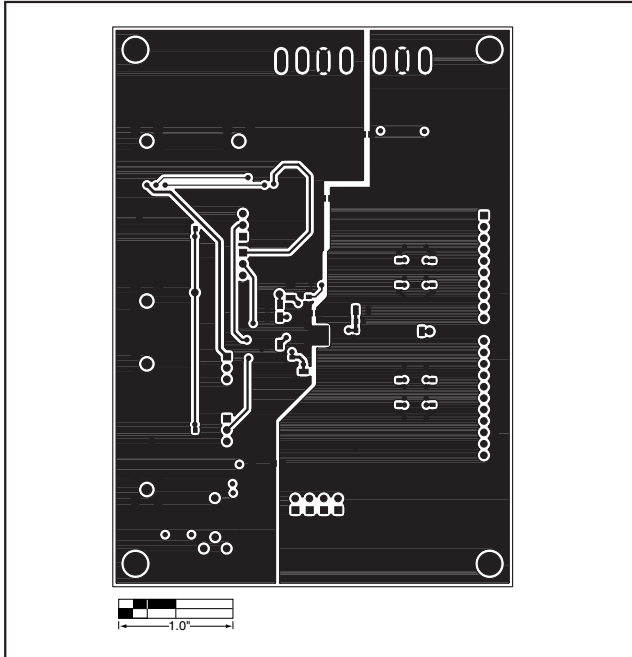


Figure 7. MAX1181 EV Kit PC Layout—Solder Side

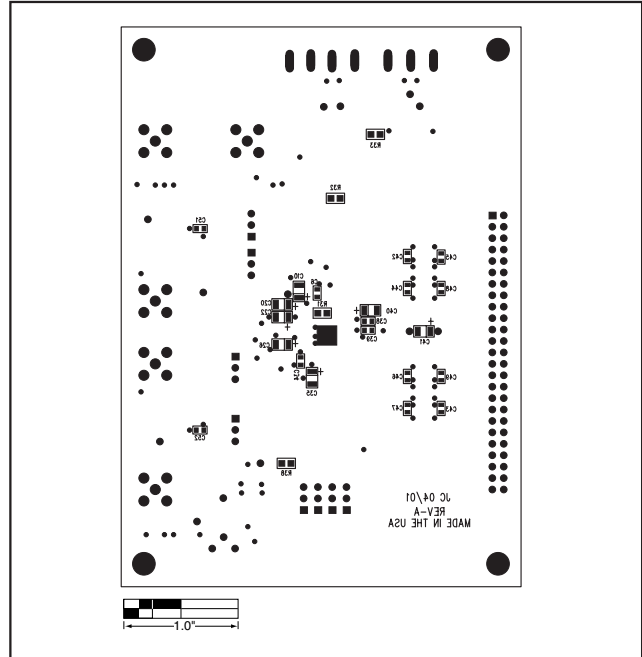


Figure 8. MAX1181 EV Kit Component Placement Guide—Solder Side

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

**Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600** \_\_\_\_\_ **9**