

RELIABILITY REPORT  
FOR  
**MAX2055EUP**  
PLASTIC ENCAPSULATED DEVICES

April 2, 2004

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Reviewed by



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## Conclusion

The MAX2055 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX2055 high-performance, digitally controlled, variable-gain, differential analog-to-digital converter (ADC) driver/amplifier (DVGA) is designed for use from 30MHz to 300MHz in base-station receivers.

The device integrates a digitally controlled attenuator and a high-linearity single-ended-to-differential output amplifier, which can either eliminate an external transformer, or can improve the even-order distortion performance of a transformer-coupled circuit, thus relaxing the requirements of the anti-alias filter preceding an ADC. Targeted for ADC driver applications to adjust gain either dynamically or as a one-time channel gain setting, the MAX2055 is ideal for applications requiring high performance. The attenuator provides 23dB of attenuation range with  $\pm 0.2$ dB accuracy.

The MAX2055 is available in a thermally enhanced 20-pin TSSOP-EP package and operates over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
All Pins to GND	-0.3V to $+(V_{CC} + 0.25\text{V})$
Input Signal (RF_IN)	20dBm
Output Power (RF_OUT)	24dBm
Operating Temperature Range	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
Junction Temperature	$+150^{\circ}\text{C}$
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+165^{\circ}\text{C}$
Lead Temperature (soldering, 10s)	$+300^{\circ}\text{C}$
Continuous Power Dissipation ( $T_A = +85^{\circ}\text{C}$ )	
28-Pin TSSOP	2100mW
Derates above $+85^{\circ}\text{C}$	
28-Pin TSSOP	21.7mW/ $^{\circ}\text{C}$

## II. Manufacturing Information

A. Description/Function:	Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier
B. Process:	GST4
C. Number of Device Transistors:	325
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	April, 2003

## III. Packaging Information

A. Package Type:	<b>28-Pin TSSOP</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0419
H. Flammability Rating:	Class: UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-A:	Level 1

## IV. Die Information

A. Dimensions:	125 x 79 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 10.78 \times 10^{-8} \quad \lambda = 10.78 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-7097) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-1M & RR-B3A**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The CR17 die type has been found to have all pins able to withstand a transient pulse of +/-200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX2055EUP**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test</b> (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
<b>Moisture Testing</b> (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

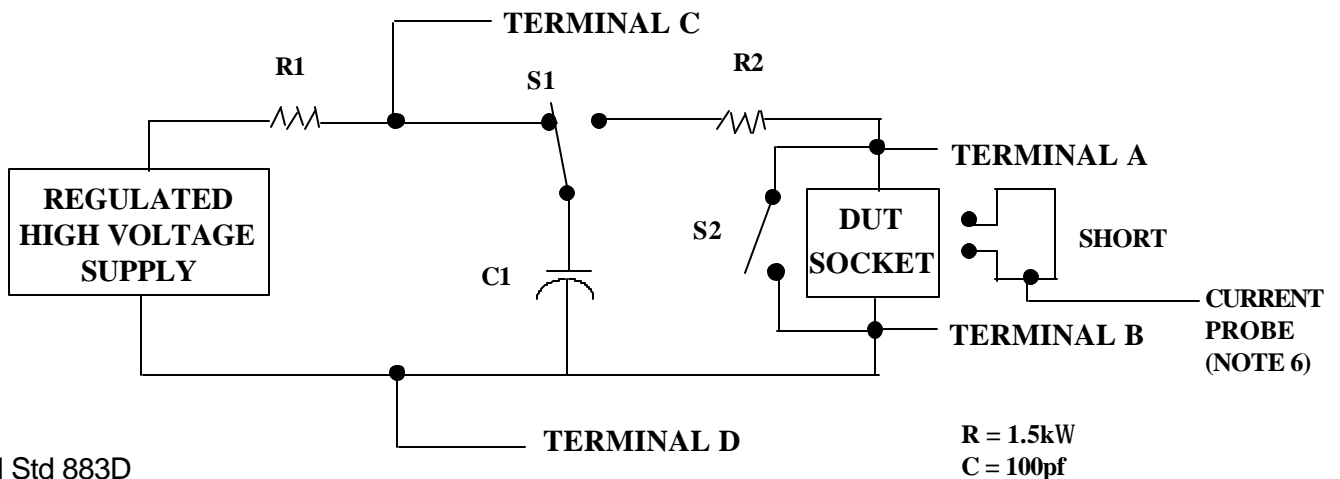
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

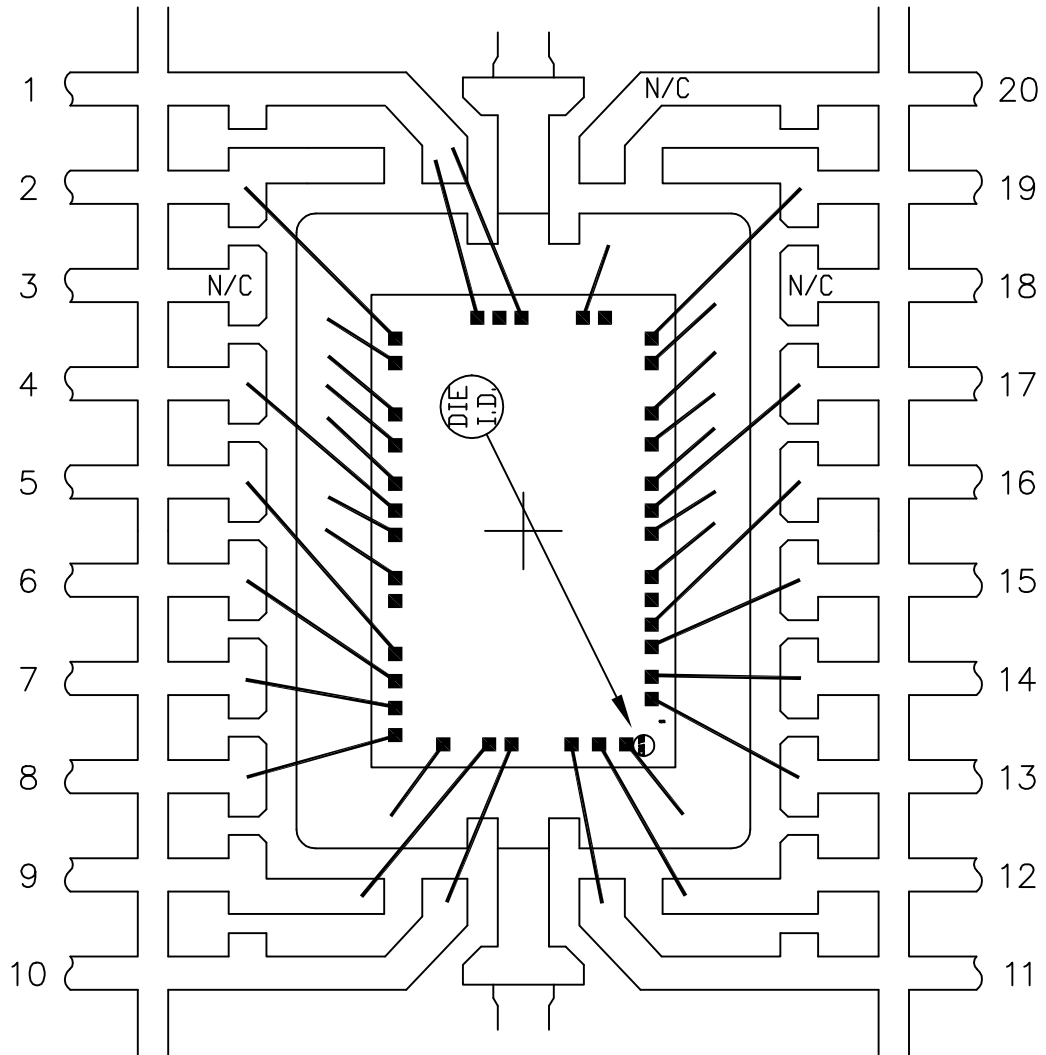
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ ,  $GND$ ,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



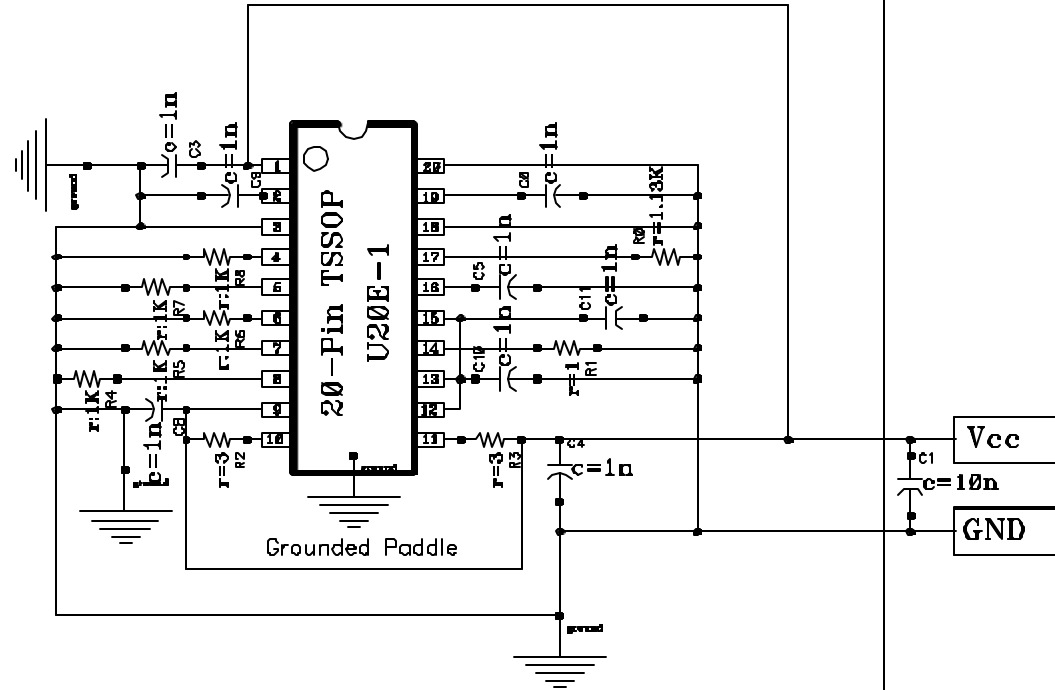
EXPOSED PAD PKG.



PKG. CODE: U20E-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x165	PKG. DESIGN			BOND DIAGRAM #: 05-9000-0419	REV: A

ONCE PER SOCKET

ONCE PER BOARD



HEADER GROUNDED (Yes/No): Yes

PRODUCT: MAX2055

PACKAGE TYPE: U20E-1

VERSION #:

DATE : Feb 21 14:09:41 2003

ICC (MAX) : 280mA

VCC : 5.25 VOLTS

NOTES: Die Type: CR17Z

The exposed paddle needs to be grounded.