



Complete DBS Direct-Conversion Tuner ICs with Monolithic VCOs

MAX2116/MAX2118

General Description

The MAX2116/MAX2118 family of low-cost direct-conversion tuner ICs are designed for use in digital direct broadcast satellite (DBS) television applications, professional VSAT systems, and two-way Internet through satellite applications. These devices set the standard for integration and performance, significantly reducing the required RF know-how for design implementation. Uniquely architected, the MAX2116/MAX2118 simplify direct main board and tuner module designs.

The MAX2116/MAX2118 devices directly convert L-band signals to baseband using a broadband I/Q downconverter. The operating frequency range extends from 925MHz to 2175MHz.

Each IC includes an LNA with gain control, I and Q downconverting mixers, and baseband lowpass filters gain and cutoff frequency control. Together, the RF and baseband variable gain amplifiers provide more than 79dB of gain control range.

The devices include fully monolithic VCOs, as well as a complete frequency synthesizer. Additionally, an on-chip crystal oscillator is provided along with a buffered output for driving additional tuners and demodulators. Synthesizer programming and device configuration are accomplished with a 2-wire serial interface. For multi-tuner applications, each device can be configured to have one of eight possible 2-wire interface addresses.

Simplifying the interface to low-voltage CMOS demodulators, the MAX2116/MAX2118 incorporate two 2.85V regulated outputs for pulling up open-drain interface connections, thus preventing noisy 3V rails from corrupting the sensitive analog signal of the tuners.

The MAX2116/MAX2118 devices are the most versatile family of DBS products available. With both single-ended and differential baseband outputs, these devices are compatible with virtually all QPSK/8-PSK demodulators. The tuners are available in a very small 40-pin QFN package.

Applications

- DVB
- DSS (U.S.)
- VSAT
- Internet Through Satellite

I²C is a trademark of Philips Corp.

Features

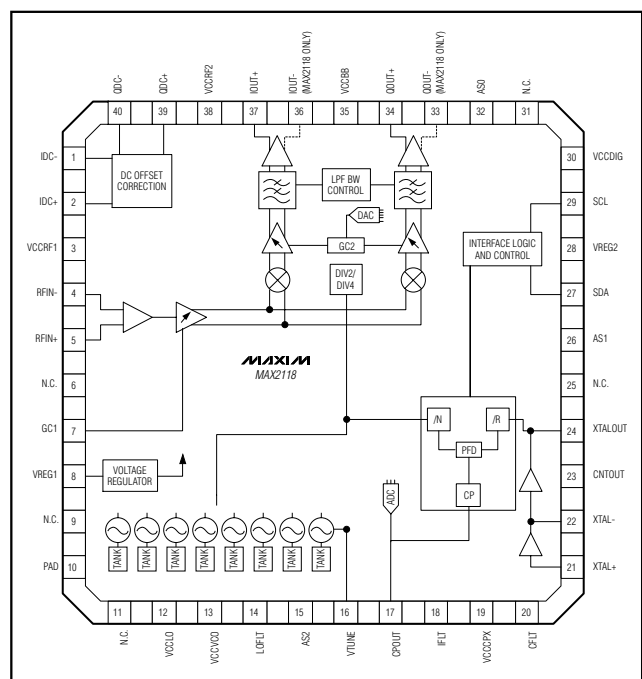
- ◆ Fully Integrated VCOs
- ◆ Supports 1Mbaud to 45Mbaud, 925MHz to 2175MHz Operation
- ◆ 4MHz to 33MHz Tunable LP Filters
- ◆ Complete Synthesizer with I²C™ Interface
- ◆ Analog RF VGA and Digital Baseband VGA
- ◆ Multiple I²C Addresses for Multituner Applications
- ◆ Single-Ended (MAX2116) and Differential (MAX2118) I/Q Interface

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|------------|--------------|------------------------|
| MAX2116UGL | 0°C to +85°C | 40 QFN-EP* (6mm x 6mm) |
| MAX2118UGL | 0°C to +85°C | 40 QFN-EP* (6mm x 6mm) |

*EP = exposed pad.

Pin Configuration/Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| V _{CC} to GND | -0.3V to +5.5V |
| All Other Pins to GND | -0.3V to (V _{CC} + 0.3V) |
| RFIN+ to RFIN-, XTL+ to XTL-, IDC+ to IDC- | |
| QDC+ to QDC- | ±2.0V |
| CNTOUT, XTALOUT, CPOUT, VREG1/2, I/QOUT± to GND Short-Circuit Duration | 10s |
| Continuous Current (any pin other than V _{CC} or GND) | 10mA |

| | |
|---|-----------------|
| Continuous Power Dissipation (T _A = +85°C) | |
| 40-pin QFN (derate 23.3mW/°C above +85°C) | 1.86W |
| Operating Temperature Range | 0°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +160°C |
| Soldering Temperature (10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, GND = 0V, GC1 = +0.75V; no AC signal applied, default register settings, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|---------------|------|------|------------------|
| SUPPLY | | | | | |
| Supply Voltage | | 4.75 | | 5.25 | V |
| Supply Current | LO locked at 2175MHz | | 195 | 265 | mA |
| ANALOG GAIN CONTROL INPUT—GC1 | | | | | |
| Usable Voltage Range | | 0.75 | | 2.6 | V |
| Input Current | 0.75V < GC1 < 2.6V (Note 2) | -50 | | +50 | μA |
| BASEBAND OUTPUTS— IOUT, QOUT (MAX2116) | | | | | |
| Nominal Output Voltage Swing | R _{LOAD} = 1kΩ // 10pF (Note 3) | | 0.8 | | V _{P-P} |
| Output Clipping Voltage | | | 2 | | V _{P-P} |
| DC Output Voltage | | | 1.2 | | V |
| BASEBAND OUTPUTS— IOUT±, QOUT± (MAX2118) | | | | | |
| Nominal Output Voltage Swing | R _{LOAD} = 2kΩ // 10pF (differential) (Note 3) | Bit DL = high | 1 | | V _{P-P} |
| | | Bit DL = low | 0.59 | | |
| Output Clipping Voltage | | | 2 | | V _{P-P} |
| Common-Mode Voltage | | 0.65 | 0.75 | 0.85 | V |
| DC Offset Voltage | | -50 | 0 | +50 | mV |
| ANALOG OUTPUT— VREG1, VREG2 | | | | | |
| Output Voltage | | 2.7 | 2.85 | 3.05 | V |
| Source Current | Each output | | | 3 | mA |
| STATIC CONTROL INPUTS—AS2, AS1, AS0 | | | | | |
| Input Voltage High | | 4 | | | V |
| Input Voltage Low | | | | 0.5 | V |
| Input Current | | -50 | | +50 | μA |
| SYNTHESIZER DC PARAMETERS | | | | | |
| Charge Pump Source/Sink Current | Bits CP1 = 0, CP0 = 0 | ±35 | ±50 | ±68 | μA |
| | Bits CP1 = 0, CP0 = 1 | ±70 | ±100 | ±136 | |
| | Bits CP1 = 1, CP0 = 0 | ±140 | ±200 | ±272 | |
| | Bits CP1 = 1, CP0 = 1 | ±280 | ±400 | ±544 | |

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MAX2116/MAX2118

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +4.75V$ to $+5.25V$, $GND = 0V$, $GC1 = +0.75V$, no AC signal applied, default register settings, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|---|------------|-----------------|-----------------|-----------------|---|
| Charge Pump Off-Leakage Current | | -10 | | +10 | nA | |
| Charge Pump Output Voltage Compliance | Charge-pump positive-to-negative current matching of $\pm 10\%$ | 0.4 | | $V_{CC} - 0.6$ | V | |
| I²C INTERFACE—SDA, SCL | | | | | | |
| Clock Rate | | | | 400 | kHz | |
| Input Logic Level Low | | | | 1.5 | V | |
| Input Logic Level High | | 2.3 | | | V | |
| Input Hysteresis | | | 0.2 | | V | |
| Input Current | | -10 | | +10 | μA | |
| Output Logic Level Low | 6mA sink current | | 0.6 | | V | |
| VTUNE ADC | | | | | | |
| Resolution | | | 3 | | Bits | |
| Input Voltage Range | (Note 4) | 0 | | V_{CC} | V | |
| ADC Reference Ladder Trip Point | ADC read bits | 110 to 111 | $V_{CC} - 0.70$ | $V_{CC} - 0.65$ | $V_{CC} - 0.60$ | V |
| | | 101 to 110 | 2.8 | 2.97 | 3.14 | |
| | | 100 to 101 | 1.91 | 2.03 | 2.15 | |
| | | 011 to 100 | 1.29 | 1.38 | 1.47 | |
| | | 010 to 011 | 0.87 | 0.94 | 1.01 | |
| | | 001 to 010 | 0.60 | 0.65 | 0.70 | |
| | | 000 to 001 | 0.40 | 0.44 | 0.48 | |

AC ELECTRICAL CHARACTERISTICS

(MAX2116/MAX2118 EV kits, $V_{CC} = +4.75V$ to $+5.25V$, $GC1$ and $GC2$ set for maximum gain, $GND = 0V$, $I_{OUT} = Q_{OUT} = 800mV_{P-P}$ (MAX2116), loaded with $1k\Omega$ $I_{OUT\pm} = Q_{OUT\pm} = 590mV_{P-P}$ differential ($DL = 0$, MAX2118), $I_{OUT\pm} = Q_{OUT\pm} = 1V_{P-P}$ differential ($DL = 1$, MAX2118), loaded with differential $2k\Omega$. Baseband LPF BW = 33MHz, $f_{RFIN} = 2175MHz$. For default register values, see the *Serial Interface and Control Registers* section. $T_A = +25^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|-----|-----|------|-------|
| RF FRONT END | | | | | |
| RF Input Frequency Range | $T_A = 0^\circ C$ to $+85^\circ C$ | 925 | | 2175 | MHz |
| Input Carrier Levels Necessary to Produce $800mV_{P-P}$ at I/Q Baseband Outputs (MAX2116) | $GC1 = 0.75V$ (max gain), bits $GC2(4) - GC2(0) = 00000$ (max gain), for output $\geq 800mV_{P-P}$ | | -77 | -72 | dBm |
| | $GC1 = 2.6V$ (min gain), bits $GC2(4) - GC2(0) = 11111$ (min gain), for output $\leq 800mV_{P-P}$ | 3 | 16 | | |

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2116/MAX2118 EV kits, $V_{CC} = +4.75V$ to $+5.25V$, GC1 and GC2 set for maximum gain, GND = 0V, IOUT = QOUT = 800mV_{P-P} (MAX2116), loaded with 1k Ω IOUT \pm = QOUT \pm = 590mV_{P-P} differential (DL = 0, MAX2118), IOUT \pm = QOUT \pm = 1V_{P-P} differential (DL = 1, MAX2118), loaded with differential 2k Ω . Baseband LPF BW = 33MHz, $f_{RFIN} = 2175MHz$. For default register values, see the *Serial Interface and Control Registers* section. $T_A = +25^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|------|---------|------|----------|
| Input Carrier Levels Necessary to Produce 1V _{P-P} (Differential) at I/Q Baseband Outputs (MAX2118) | GC1 = 0.75V (max gain), bit DL = 1, bits GC2(4) - GC2(0) = 00000 (max gain) for output \geq 800mV _{P-P} | | -77 | -72 | dBm |
| | GC1 = 2.6V (min gain), bit DL = 1, bits GC2(4) - GC2(0) = 11111 (min gain), for output \leq 800mV _{P-P} | 3 | 16 | | |
| Input Carrier Levels Necessary to Produce 590mV _{P-P} (Differential) at I/Q Baseband Outputs (MAX2118) | GC1 = 0.75V (max gain), bit DL = 0, bits GC2(4) - GC2(0) = 00000 (max gain), for output \geq 800mV _{P-P} | | -77 | -72 | dBm |
| | GC1 = 2.6V (min gain), bit DL = 0, bits GC2(4) - GC2(0) = 11111 (min gain), for output \leq 800 mV _{P-P} | 3 | 16 | | |
| RF Gain Control (GC1) Range | 0.75V < GC1 < 2.6V | 60 | 69 | | dB |
| Baseband Gain Control (GC2) Range | Bits GC2(4) - GC2(0) = 00000 to 11111 | 19 | 24 | | dB |
| IIP3 | (Note 5) | | 10 | | dBm |
| IIP2 | (Note 6) | | 22 | | dBm |
| NF | GC1 = 0.75V (max gain), bits GC2(4) - GC2(0) = 00000 (max gain) | | 10.5 | | dB |
| Minimum RF Input Return Loss | 75 Ω input source, 925MHz < f_{RFIN} < 2175MHz | | 13.5 | | dB |
| Maximum LO Leakage at RFIN | 925MHz < f_{LO} < 2175MHz | | -80 | -63 | dBm |
| LO-Generated RFIN Second Harmonic Rejection | Unwanted in 925MHz to 2175MHz band | 33 | 50 | | dB |
| | Unwanted = 2250MHz | 30 | 45 | | |
| | Unwanted above 2250MHz | | 6dB/oct | | |
| BASEBAND OUTPUTS | | | | | |
| Baseband I/Q Output Impedance | Single ended, real Z _{OUT} | | 30 | | Ω |
| Baseband Highpass -3dB Point | 0.1 μ F capacitors at IDC \pm , QDC \pm | | 850 | | Hz |
| Quadrature Phase Error | 125kHz baseband test tone | | | 4 | Degrees |
| Quadrature Gain Error | 125kHz baseband test tone | | | 1.2 | dB |
| Baseband Lowpass BW Range | Baseband -3dB cutoff frequency | 4 | | 33 | MHz |
| LP Filter BW Accuracy | F _c = 4MHz | -5.5 | | +5.5 | % |
| | F _c = 33MHz (Note 7) | -10 | | +10 | % |
| Ratio of In-Filter-Band to Out-of-Filter-Band Noise | F _{inband} = 100Hz to 22.5MHz, F _{outband} = 87.5MHz to 112.5MHz | | 25 | | dB |

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MAX2116/MAX2118

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2116/MAX2118 EV kits, $V_{CC} = +4.75V$ to $+5.25V$, GC1 and GC2 set for maximum gain, GND = 0V, IOUT = QOUT = 800mV_{P-P} (MAX2116), loaded with 1k Ω IOUT \pm = QOUT \pm = 590mV_{P-P} differential (DL = 0, MAX2118), IOUT \pm = QOUT \pm = 1V_{P-P} differential (DL = 1, MAX2118), loaded with differential 2k Ω . Baseband LPF BW = 33MHz, $f_{RFIN} = 2175MHz$. For default register values, see the *Serial Interface and Control Registers* section. $T_A = +25^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|---------------|------|-------|------------------|
| VCO PERFORMANCE | | | | | |
| VCO Tuning Range | VCO 0 to VCO 7 coverage | 2250 | | 4500 | MHz |
| VCO Tuning Gain | Worst case, any VCO, any tuning voltage | | 500 | | MHz/V |
| LO Phase Noise Referred to Mixer LO Port | Bit DIV2 = 1, $f_{LO} = 2175MHz$ | 10kHz offset | | -75 | dBc/Hz |
| | | 100kHz offset | | -99 | |
| SYNTHESIZER PERFORMANCE | | | | | |
| Phase Detector Comparison Frequency | | 0.15 | | 2 | MHz |
| Reference Divide Range | | 2 | | 128 | |
| RF Divide Range | | 256 | | 32768 | |
| Level at XTALOUT | 4MHz to 27MHz, driving 10pF | 0.75 | 1 | 1.5 | V _{P-P} |
| PLL-Referred Phase Noise Floor | | | -143 | | dBc/Hz |
| XTAL Frequency Range | | 4 | | 27 | MHz |

Note 1: Parameters are production tested at $T_A = +25^\circ C$ and $+85^\circ C$; limits called out at $0^\circ C$ are guaranteed by design and characterization and are not production tested.

Note 2: GCI gain control is guaranteed over this voltage range. 0.75V corresponds to maximum gain and 2.6V corresponds to minimum gain.

Note 3: RF front-end specification met at this output level.

Note 4: The VTUNE ADC transfer curve has been tailored to that of the VCO tuning curve.

Note 5: Input IP3 test conditions: VGC1 set to provide 800mV_{P-P} (MAX2116), 1V_{P-P} differential (MAX2118, DL = high), 0.59V_{P-P} differential (MAX2118 DL = low) baseband output when mixing down a -25dBm tone at 2175MHz to 5MHz baseband, with VGC2 = 00000. Two tones at -18dBm each are applied at $f_{LO} - 100MHz$ and $f_{LO} - 195MHz$; IM3 tone at 5MHz is measured at baseband but is referred to RF input.

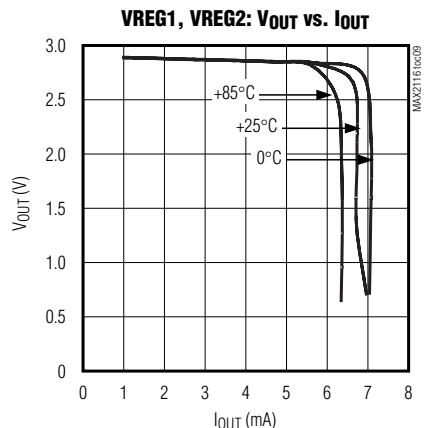
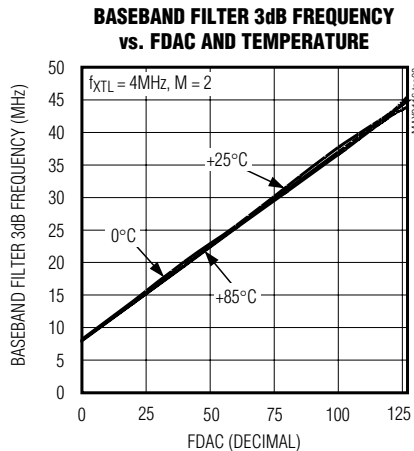
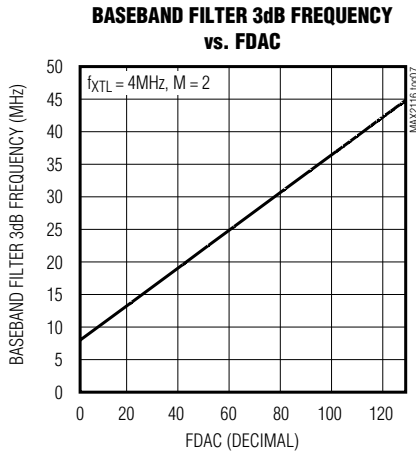
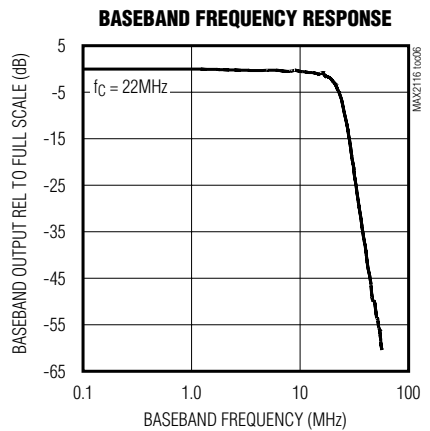
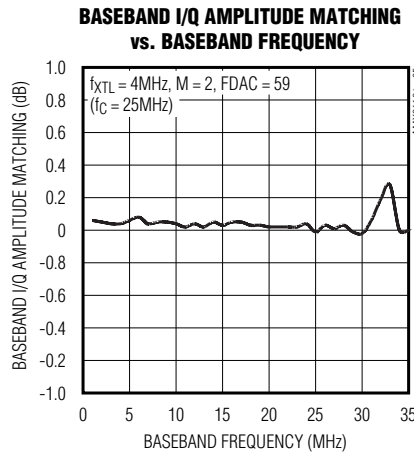
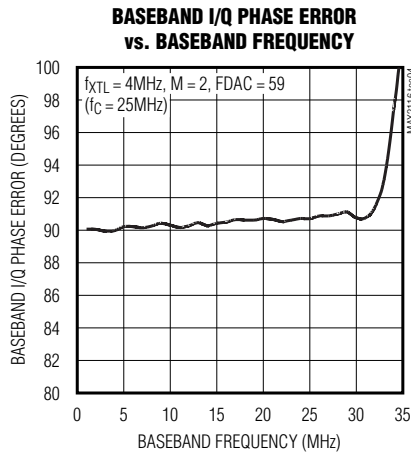
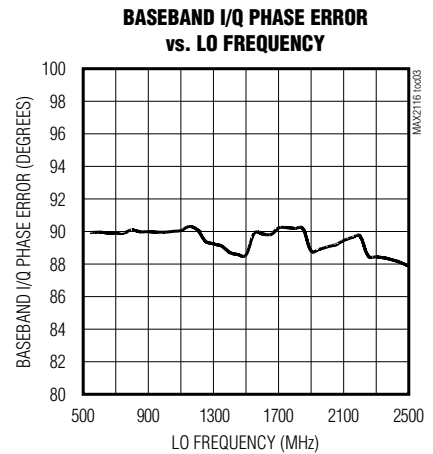
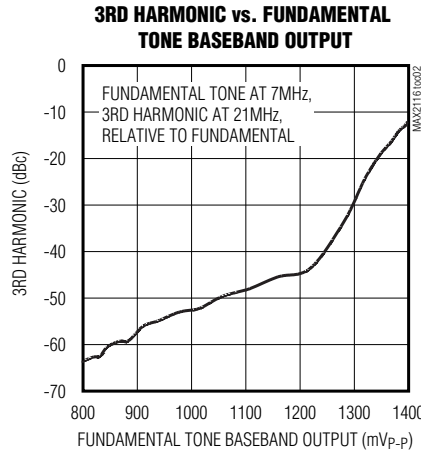
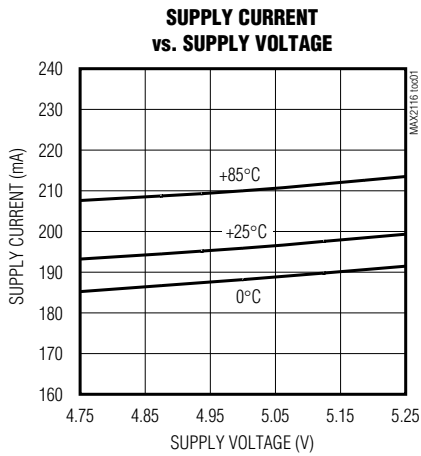
Note 6: Input IP2 test conditions: VGC1 set to provide 800 mV_{P-P} (MAX2116), 1V_{P-P} differential (MAX2118, DL = high), 0.59V_{P-P} differential (MAX2118 DL = low) baseband output when mixing down a -25dBm tone at 2175MHz to 5MHz baseband, with VGC2 = 0.75V. Two tones at -25dBm each are applied at $f_{RF} = 925MHz$ and $f_{RF} = 1245MHz$; IM2 tone at $f_{LO} - 5MHz$ is measured at baseband but is referred to RF input.

Note 7: These parameters are guaranteed by design and characterization, and are not production tested.

Complete DBS Direct-Conversion Tuner ICs with Monolithic VCOs

Typical Operating Characteristics

(MAX2116/MAX2118 EV kits, $V_{CC} = +4.75V$ to $+5.25V$, GC1 and GC2 set for maximum gain, $GND = 0V$, $I_{OUT} = Q_{OUT} = 800$ mV_{P-P} (MAX2116), loaded with $1k\Omega$ $I_{OUT\pm} = Q_{OUT\pm} = 590$ mV_{P-P} differential (DL = 0, MAX2118), $I_{OUT\pm} = Q_{OUT\pm} = 1V$ _{P-P} differential (DL = 1, MAX2118), loaded with differential $2k\Omega$. Baseband LPF BW = 33MHz, $f_{RFIN} = 2175$ MHz. For default register values, see the *Serial Interface and Control Registers* section. $T_A = 0^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

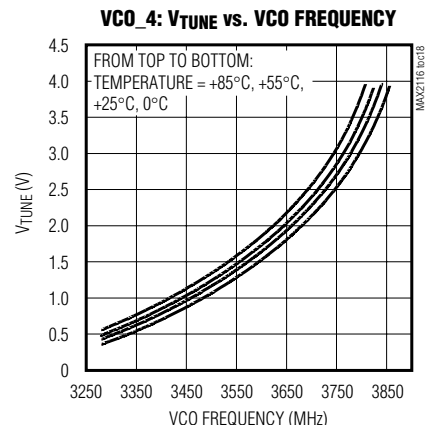
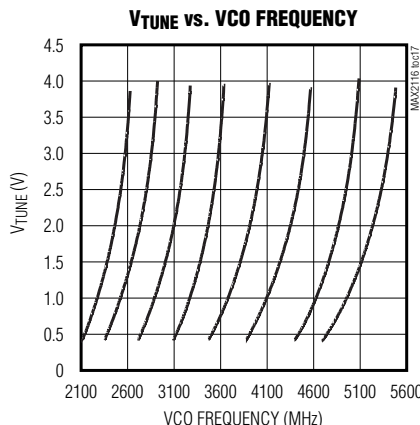
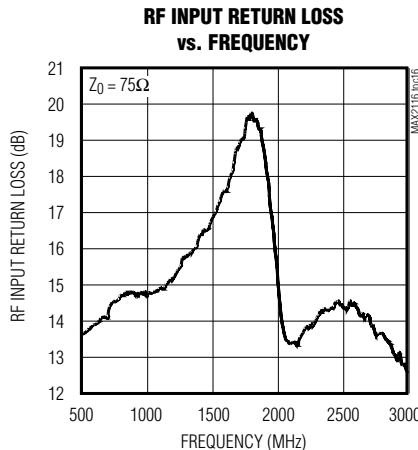
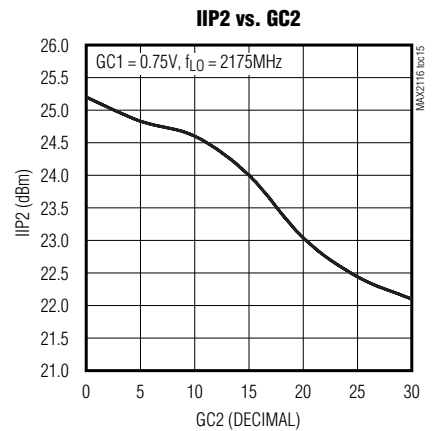
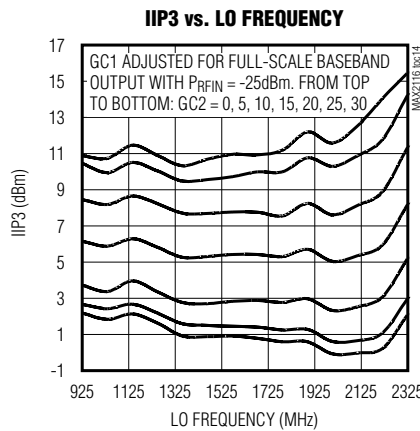
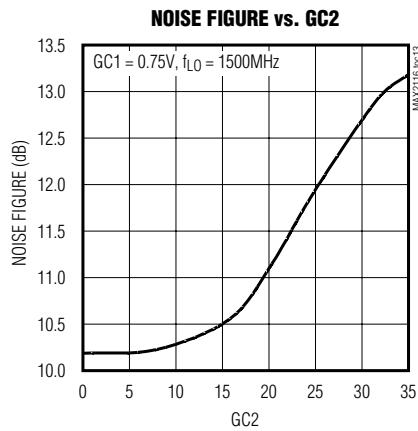
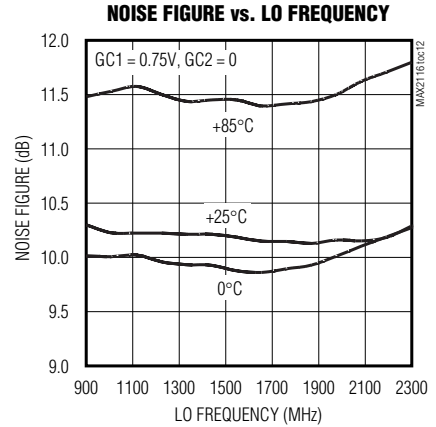
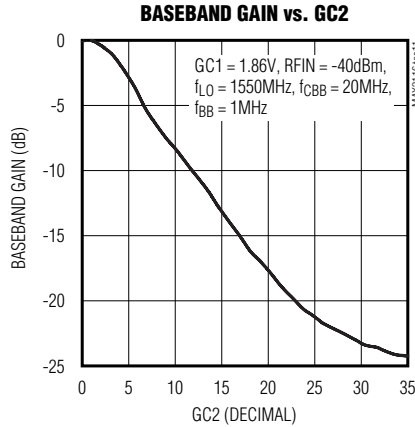
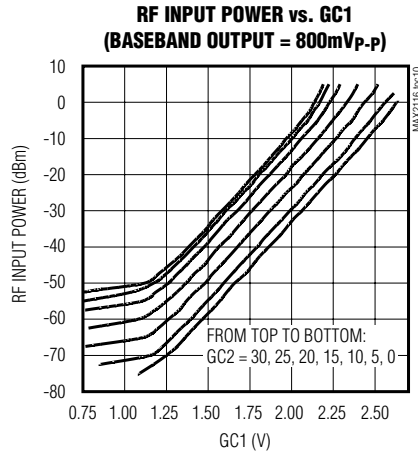


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MAX2116/MAX2118

Typical Operating Characteristics (continued)

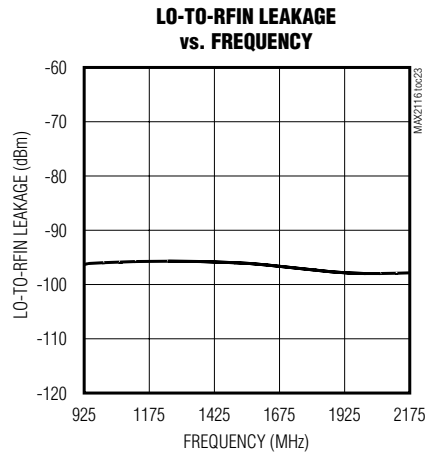
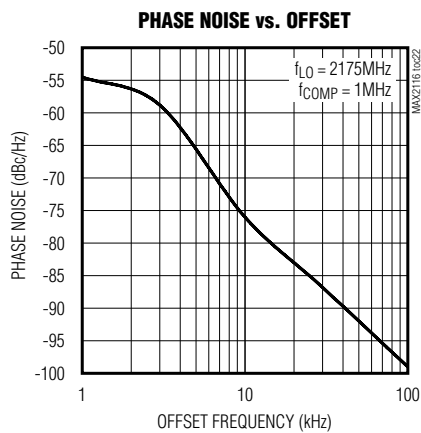
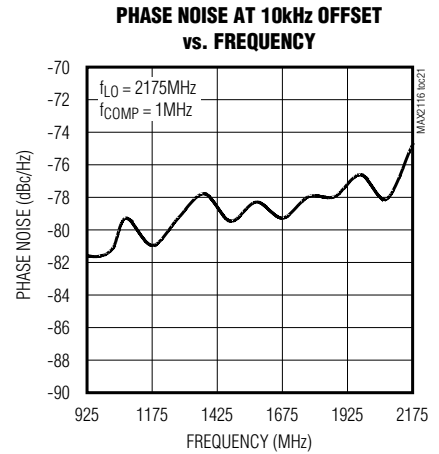
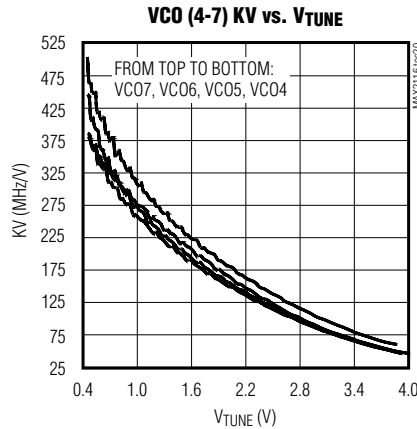
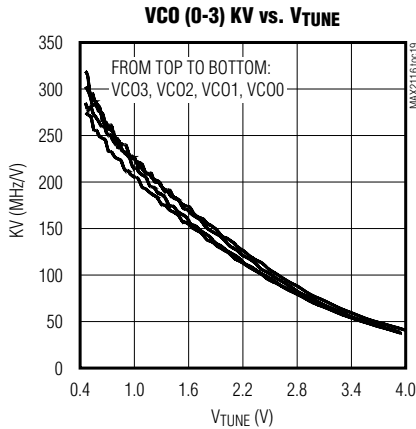
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Typical Operating Characteristics (continued)

(MAX2116/MAX2118 EV kits, $V_{CC} = +4.75V$ to $+5.25V$, GC1 and GC2 set for maximum gain, GND = 0V, $I_{OUT} = Q_{OUT} = 800$ mV_{P-P} (MAX2116), loaded with $1k\Omega$ $I_{OUT\pm} = Q_{OUT\pm} = 590$ mV_{P-P} differential (DL = 0, MAX2118), $I_{OUT\pm} = Q_{OUT\pm} = 1$ V_{P-P} differential (DL = 1, MAX2118), loaded with differential $2k\Omega$. Baseband LPF BW = 33MHz, $f_{RFIN} = 2175$ MHz. For default register values, see the *Serial Interface and Control Registers* section. $T_A = 0^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

MAX2116/MAX2118

| PIN | NAME | FUNCTION |
|------------------|-----------------|--|
| 1, 2 | IDC-, IDC+ | I-Channel Baseband DC Offset Correction. Connect a 0.1 μ F ceramic chip capacitor from IDC- to IDC+. |
| 3 | VCCRF1 | DC Power Supply for LNA and First-Stage RF VGA. Connect to a 5V \pm 5% low-noise supply. Bypass with a 1nF capacitor directly to GND. Do not share vias. |
| 4 | RFIN- | 75 Ω RF-Inverting Input. Working in conjunction with RFIN+ for differential input. Terminate with 22pF capacitor in series with a 75 Ω resistor to GND for single-ended input. |
| 5 | RFIN+ | 75 Ω RF Noninverting Input. Working in conjunction with RFIN- for differential input. Connect to source through a 22pF series capacitor. |
| 6, 9, 11, 25, 31 | N.C. | No Connection. Pin should be connected directly to GND. |
| 7 | GC1 | Gain Control Input for RF Front End. High-impedance analog input with an operating range of 0.75V to 2.6V. VGC1 = 0.75V corresponds to maximum gain. |
| 8, 28 | VREG1, VREG2 | 2.85V Linear Regulator. Used for terminating open-drain interfaces from demodulator. Each regulator can source 3mA. |
| 10 | PAD | Ground. Direct connection to exposed pad. Can be used to check exposed pad continuity to ground. |
| 12 | VCCLO | DC Power Supply for LO Circuits. Connect to a 5V \pm 5% low-noise supply. Bypass with a 1nF capacitor directly to GND. Do not share vias. |
| 13 | VCCVCO | DC Power Supply for VCO Circuits. Connect to a 5V \pm 5% low-noise supply. See the <i>Applications Information</i> section for more details. |
| 14 | LOFLT | LO Internal Regulator Bypass. Bypass with a 0.22 μ F ceramic chip capacitor to GND. |
| 15, 26, 32 | AS2, AS1, AS0 | I ² C Address Select Control. See Table 1 and Table 2. These pins are internally pullup to V _{CC} . For logic high, leave these pins open. |
| 16 | VTUNE | High Impedance VCO Tune Input |
| 17 | CPOUT | Charge-Pump Output |
| 18 | IFLT | Test Pin. For normal operation, connect IFLT to ground. |
| 19 | VCCCPX | DC Power Supply for Charge Pump and XTAL Oscillator Circuits. Connect to a 5V \pm 5% low-noise supply. Bypass with a 1nF capacitor directly to GND. Do not share vias. |
| 20 | CFLT | Bypass for Internal Crystal Oscillator Bias. Bypass with a 0.22 μ F ceramic chip capacitor to GND. |
| 21, 22 | XTL+, XTAL- | Crystal Oscillator Interface. See <i>Typical Operating Circuit</i> . |
| 23 | CNTOUT | Test Pin. Must be left open. |
| 24 | XTALOUT | Crystal Oscillator Buffer Output. Requires a 10nF DC-blocking capacitor. |
| 27, 29 | SDA, SCL | I ² C Data and Clock Interface. See the <i>Applications Information</i> section for details. |
| 30 | VCCDIG | DC Power Supply for Digital Circuits. Connect to a 5V \pm 5% low-noise supply. Bypass with a 1nF capacitor directly to GND. Do not share vias. |
| 33 | N.C. (MAX2116) | No Connection. Pin should be connected directly to GND. |
| | QOUT- (MAX2118) | Inverting Baseband Quadrature Output |

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Pin Description (continued)

| PIN | NAME | FUNCTION |
|--------|-----------------|---|
| 34 | QOUT+ | Noninverting Baseband Quadrature Output |
| 35 | VCCBB | DC Power Supply for Baseband Circuits. Connect to a 5V ±5% low-noise supply. Bypass with a 1nF capacitor directly to GND. Do not share vias. |
| 36 | N.C. (MAX2116) | No Connection. Pin should be connected directly to GND. |
| | IOUT- (MAX2118) | Inverting Baseband In-Phase Output |
| 37 | IOUT/IOUT+ | Noninverting Baseband In-Phase Output |
| 38 | VCCRF2 | DC Power Supply for RF Circuits and Second-Stage RF VGA Circuits. Connect to a 5V ±5% low-noise supply. Bypass with a 1nF capacitor directly to GND. Do not share vias. |
| 39, 40 | QDC+, QDC- | Q-Channel Baseband DC Offset Correction. Connect a 0.1µF ceramic chip capacitor from QDC- to QDC+. |
| — | Exposed Pad | Ground |

Detailed Description

The MAX2116/MAX2118 downconvert RF signals in the 925MHz to 2175MHz range directly to baseband I/Q signals. They are targeted for digital DBS tuner applications. However, the MAX2116/MAX2118 are applicable to any system requiring a broadband I/Q downconversion.

Internally, the MAX2116/MAX2118 consist of a broadband front-end LNA and variable gain stage, quadrature downconverter, monolithic broadband VCOs, complete frequency synthesizer, crystal reference oscillator and buffer amplifier, programmable baseband lowpass filters, high-linearity I and Q baseband amplifiers, and offset correction amplifiers.

The MAX2116/MAX2118 feature a front-end VGA dynamic range in excess of 60dB. Additionally, the baseband VGA provides in excess of 19dB of additional gain control. The VSWR at RFIN is unaffected by the VGA setting.

The MAX2116/MAX2118 include completely monolithic VCOs to cover the entire 925MHz to 2175MHz frequency range. The complete frequency range is covered within a 5V tuning range, thus eliminating the need for costly 30V supplies and varactor diodes. The VCO architecture also eliminates problems associated with frequency pulling with high receive input signal levels.

Applications Information

VCCVCO (Pin 13) Bypass

Adequate filtering of the VCC connection to the VCCVCO supply pin is critical to achieve low phase noise performance. See the *Typical Operating Circuit*.

Baseband LPFs

The MAX2116/MAX2118 include programmable on-chip 7th-order Butterworth lowpass filters. The filter bandwidth is adjusted by setting two internal registers (M, FDAC). The M counter should be set such that the crystal frequency divided by M is between 1MHz and 2.5MHz. The FDAC register is then used to fine tune the bandwidth. The -3dB cutoff frequency is determined by the following equation:

$$f(3dB) = f_{XTAT} / M \times (4 + 0.145 \times FDAC)$$

where M and FDAC are decimals.

The filter can be adjusted from approximately 4MHz to 33MHz. Total device supply current is dependent on the filter BW setting, with increasing current commensurate with increasing 3dB BW.

I/Q Output Voltage Level

The MAX2116 I/Q outputs are single-ended and optimized for a nominal output voltage drive of 800mV_{P-P}. Output clipping levels are typically 2V_{P-P}.

The MAX2118 I/Q outputs are differential, with two possible nominal output voltage levels. The nominal output voltage swing is set through the DL bit Byte 04 (see register table description). With DL = low, the nominal output voltage swing is 590mV_{P-P} differential; DL = high

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boosts the baseband output gain by 4.5dB, thus allowing the output voltage swing of 1VP-P. Output clipping levels are typically 2VP-P differential.

DC Offset Compensation IDC± and QDC±

The baseband highpass response is set through a capacitor connected between IDC+ and IDC- for the I channel and QDC+ and QDC- for the Q channel. The 3dB highpass bandwidth is determined by the following equation:

$$F_{3dB} \text{ (highpass in Hz)} = 1 / (11.750\Omega \times C), C \text{ in farads}$$

To reduce the potential for baseband spurious pickup, keep the connection between the DC compensation capacitors and the IDC± and QDC± pins as short as possible by placing the capacitors as close to the device as manufacturing allows.

VREG1 and VREG2

The MAX2116/MAX2118 include two 2.85V voltage regulator outputs, with a maximum source current rating of 3mA each. These outputs ease the interface to low-voltage demodulators by providing a clean pullup termination for open-drain/collector outputs. VREG1 is located by the GC1 input control, with VREG2 conveniently located between the 2-wire interface control pins.

VCO Selection

The MAX2116/MAX2118 include eight fully monolithic VCOs to cover the entire 925MHz to 2175MHz range. Maxim has a detailed application note that describes the operation of the VCO system and proper selection of the desired VCO. This application note is available by request from Maxim.

Crystal Output Buffer (XTALOUT)

The on-chip crystal oscillator circuit has been designed for operation from 4MHz to 27MHz. The crystal output buffer amplifier is designed to nominally deliver between 0.75VP-P and 1.5VP-P. However, it might be necessary to add a resistor between the XTALOUT pin and ground to increase the signal swing when using

higher frequency crystals (>20MHz). Recommended values are between 2kΩ and 5kΩ.

Serial Interface and Control Registers

Programming Bits

The MAX2116/MAX2118 conform to the Philips I²C standard, 400kbps (fast mode), and operate as a slave.

The MAX2116/MAX2118 have eight read and write addresses, which are determined by the logic state of the three address-select pins (AS2, AS1, and AS0). In all cases, the MSB is transmitted and read first (see Tables 1, 2, 3).

Programming Bit Definition

Byte 00 (Default = 03)

Bit DIV2 controls the VCO frequency divider. High level = divide-by-2 enabled; low level = divide-by-4 enabled. Default is DIV2 = 0 (divide-by-4 enabled).

Bits N(14)–N(8) are the 7 upper bits of the 15-bit programmable N divider, with the default value of N = 950.

The overall VCO divide ratio is:

$$2^{14} \times N(14) + 2^{13} \times N(13) \dots + 2^5 \times N(5) + 2^4 \times N(4) + 2^3 \times N(3) \dots + 2^0 \times N(0)$$

Byte 01 (Default = B6)

Bits N(7)–N(0) are the 8 lower bits of the 15-bit programmable N divider.

Table 1. MAX2116/MAX2118 Write Address Byte

| AS2 | AS1 | AS0 | MSB | ADDRESS BYTE | | | | | | LSB |
|------|------|------|-----|--------------|---|---|---|---|---|-----|
| Low | Low | Low | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Low | Low | High | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| Low | High | Low | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Low | High | High | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| High | Low | Low | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| High | Low | High | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| High | High | Low | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| High | High | High | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |

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Table 2. MAX2116/MAX2118 Read Address Byte

| AS2 | AS1 | AS0 | MSB | ADDRESS BYTE | | | | | | LSB |
|------|------|------|-----|--------------|---|---|---|---|---|-----|
| Low | Low | Low | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Low | Low | High | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| Low | High | Low | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| Low | High | High | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| High | Low | Low | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| High | Low | High | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| High | High | Low | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| High | High | High | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

| WRITE TO MODE | RESET VALUE | ADDR-H | MSB | CONTROL BYTE | | | | | | LSB |
|------------------|-------------|--------|------|--------------|-----|-----|-----|------|------|------|
| Address | — | C0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | C2 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | C4 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| | | C6 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| | | C8 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| | | CA | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| | | CC | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| | | CE | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| N High | 03 | 00 | DIV2 | N14 | N13 | N12 | N11 | N10 | N9 | N8 |
| N Low | B6 | 01 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |
| R and CP and VCO | 9F | 02 | R2 | R1 | R0 | CP1 | CP0 | OSC2 | OSC1 | OSC0 |
| I/Q Filter DAC | 7F | 03 | X0 | F6 | F5 | F4 | F3 | F2 | F1 | F0 |
| LPF Divider DAC | 04 | 04 | ADL | ADE | DL | M4 | M3 | M2 | M1 | M0 |
| GC2 and Diag | 1F | 05 | D2 | D1 | D0 | G4 | G3 | G2 | G1 | G0 |

Byte 02 (Default = 3D)

Bits R(2), R(1), and R(0) are the reference divider bits.

The overall reference divide ratio is $2^{(4 \times R(2) + 2 \times R(1) + R(0))}$, with the default value of R = 4.

Bits CP1, CP0 control the charge pump current, with the default value of $\pm 400\mu\text{A}$ (Table 4).

Bits OSC2, OSC1, and OSC0 control which of the eight on-chip VCOs is activated. Default is VCO 5 (101) (Table 5).

Byte 03 (Default = 7F)

Bit X(0) is unused; default = 0.

Bits F(6)–F(0) set the value of FDAC for the baseband lowpass filter -3dB cutoff frequency. (see the *Baseband LPFs* section).

$\text{FDAC} = 2^7 \times F(7) + 2^6 \times F(6) + \dots + 2^0 F(0)$. (Default FDAC = 127.)

Byte 04 (Default = 02)

Bit ADL is the VCO ADC latch-enable bit. ADL = 1 latches ADC value (ADL = 0, default).

Bit ADE enables VCO tune voltage DAC read. ADE = 1 enables ADC read (ADE = 0, default).

Bit DL sets the differential output drive level for the MAX2118 (default, DL = 0) (Table 6). This bit is unused for the MAX2116.

Bits M(4)–M(0) set the value of M counter of lowpass filter BW control.

$M = 2^4 \times M(4) + 2^3 \times M(3) + \dots + 2^0 F(0)$. (Default M = 2.)

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Table 4. Charge Pump Current Setting (Byte 02)

| CP1 | CP0 | CHARGE PUMP CURRENT (μ A) |
|-----|-----|--------------------------------|
| 0 | 0 | ± 50 |
| 0 | 1 | ± 100 |
| 1 | 0 | ± 200 |
| 1 | 1 | ± 400 (default) |

Table 5. On-Chip VCO Selection (Byte 02)

| OSC2 | OSC1 | OSC0 | VCO BAND |
|------|------|------|-------------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 (Default) |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

Table 6. MAX2118 Output Drive Level Selection (Byte 04)

| DL | IOUT \pm , QOUT \pm OUTPUT VOLTAGE LEVEL (DIFFERENTIAL) (V _{P-P}) |
|----|---|
| 0 | 0.59 |
| 1 | 1.0 |

BYTE 05 (default = 1F)

Bits D(2), D(1), and D(0) control diagnostic features (Table 7).

Bits G(4)–G(0) controls the gain of the baseband VGA. The BB gain is minimum at 11111 and the BB gain is maximum at 00000. Default is minimum gain setting of 11111 (Table 8).

I²C Read Status Bits

Bit PWR high indicates power has been cycled, and the MAX2116/MAX2118 registers have been reset to default values. A stop condition while in read mode resets this bit.

Bits ADC(2), ADC(1), and ADC(0) represent a 3-bit ADC conversion of the VCO tune voltage used for VCO and charge pump current selection and calibration.

Bits F(6)–F(0) are a 7-bit representation of the LPF DAC current.

Serial Interface Functional Description

Register Map

This is the standard I²C protocol. The write/read/address bytes are dependent on the states of pins AS0/AS1/AS2.

Write Operation

The first byte is the device address plus the direction bit (R/W = 0).

The second byte contains the internal address command of the first address to be accessed.

The third byte is written to the internal register directed by the command address byte.

The following bytes (if any) are written into successive internal registers.

The transfer lasts until stop conditions are encountered. The MAX2116 acknowledges every byte transfer.

Read Operation

When an address is sent, the MAX2116 sends back first the status byte and then the I/Q DAC byte.

Example: Write registers 0 to 3 with 0E, D8, 26 (Table 9).

Example: Read from status registers. Sending an ACK terminates slave transmit mode (Table 10).

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Table 7. Diagnostic Functions (Byte 05)

| D2 | D1 | D0 | DIAGNOSTIC FUNCTIONS |
|----|----|----|---|
| 0 | 0 | 0 | Normal operation |
| 0 | 0 | 1 | Force charge pump source current |
| 0 | 1 | 0 | Force charge pump sink current |
| 0 | 1 | 1 | Force charge pump High-Z state |
| 1 | 0 | 0 | Unused |
| 1 | 0 | 1 | N divider output frequency at CNTOUT pin and filter DAC output at IFILT pin |
| 1 | 1 | 0 | R divider output frequency at CNTOUT pin and GC2 DAC output at IFILT pin |
| 1 | 1 | 1 | M divider output frequency at CNTOUT pin |

Table 8. Baseband Gain Setting (Byte 5)

| READ FROM MODE | RESET VAL | ADDR-H | MSB | | | | | | | LSB |
|----------------|-----------|--------|-----|-----|----|------|------|------|----|-----|
| Address | — | C1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | C3 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | C5 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| | | C7 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| | | C9 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| | | CB | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| | | CD | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| | | CF | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| Status Info | 00 | — | 0 | PWR | 0 | ADC2 | ADC1 | ADC0 | 0 | 0 |
| I/Q Filter DAC | 00 | — | 0 | F6 | F5 | F4 | F3 | F2 | F1 | F0 |

Table 9. Example 1

| | | | | | | | | | | | |
|-------|----------------------|-----|---------------------|-----|---------|-----|---------|-----|---------|-----|------|
| Start | Device Address Write | ACK | Register Address 00 | ACK | DATA 0E | ACK | DATA D8 | ACK | DATA 26 | ACK | STOP |
|-------|----------------------|-----|---------------------|-----|---------|-----|---------|-----|---------|-----|------|

Table 10. Example 2

| | | | | | | | | | | | |
|-------|---------------------|-----|--------------------|-----|--------|----------|------|--|--|--|--|
| Start | Device Address Read | ACK | Status Register 00 | ACK | DAC D8 | ACK/NACK | STOP | | | | |
|-------|---------------------|-----|--------------------|-----|--------|----------|------|--|--|--|--|

Chip Information

TRANSISTOR COUNT: 10,935

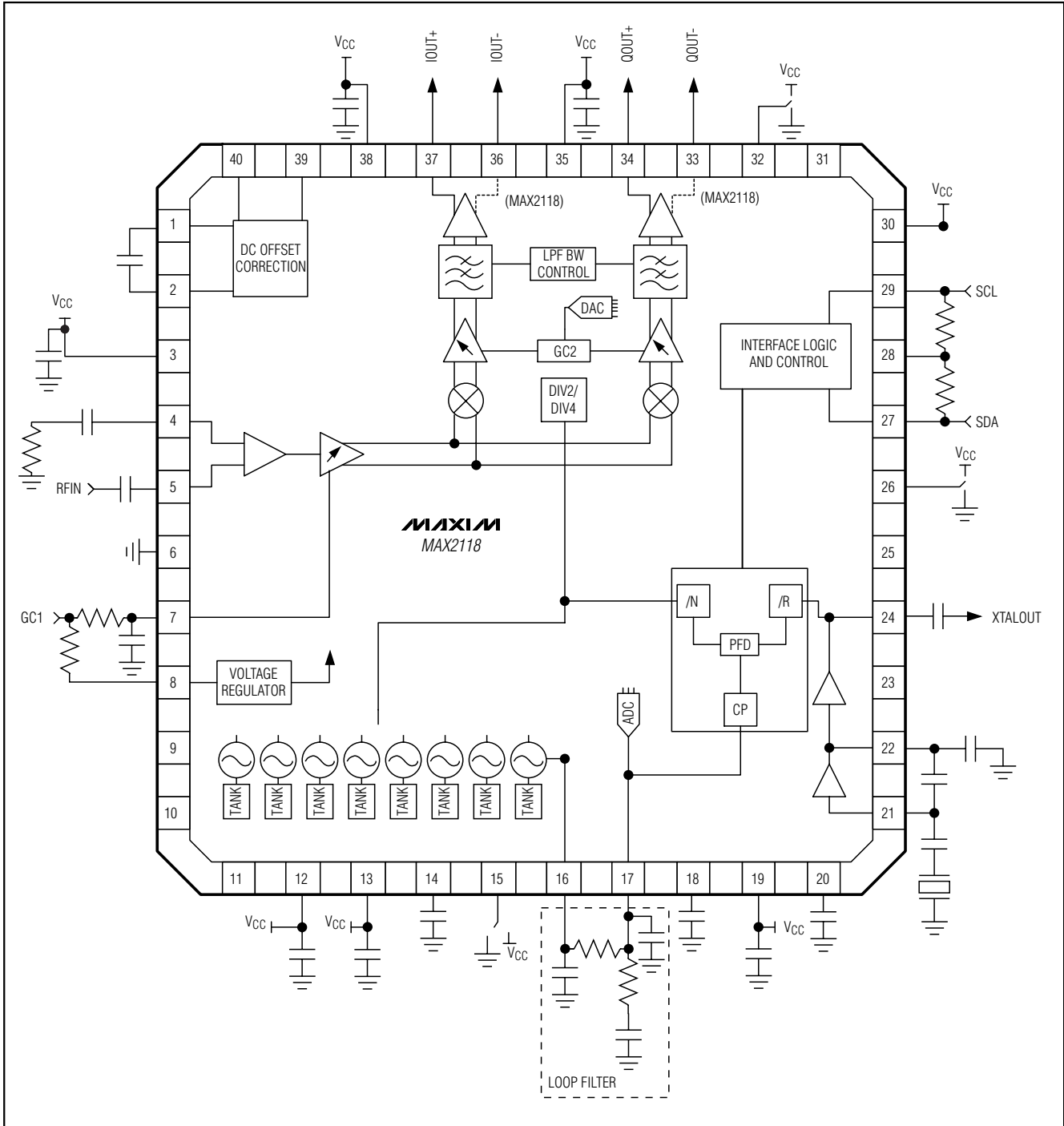
Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

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Typical Operating Circuit

MAX2116/MAX2118



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