19-2375; Rev 1; 7/03

MAXIM

Dual-Rate Fibre Channel Limiting Amplifier

General Description

The MAX3274 dual-rate Fibre Channel limiting amplifier is optimized for use in dual-rate 2.125Gbps/1.0625Gbps Fibre Channel optical receiver systems. An on-chip selectable fourth-order Bessel Thompson filter offers 15dB (typ) of attenuation at 2GHz to suppress the relaxation oscillation (RO) found in legacy transmitters. The amplifier accepts a wide range of input voltages and provides constant-level output voltages with controlled edge speeds. Receivers using the MAX3275/MAX3277 transimpedance amplifiers (TIA) and the MAX3274 dual-rate limiting amplifier can meet the Fibre Channel receiver sensitivity optical modulation amplitude (OMA) specification of 49mW$_{P-P}$ at 2.125Gbps and 31mW$_{P-P}$ at 1.0625Gbps. Additional features include a programmable threshold loss-of-signal (LOS) detector, output squelch, and bandwidth select. The MAX3274 features current-mode logic (CML) data outputs. The MAX3274 is available in a 16-pin QFN package, making it ideal for GBIC and small form-factor receiver modules.

Applications

Fibre Channel GBIC Optical Modules

Dual-Rate Fibre Channel SFF/SFP Optical Modules

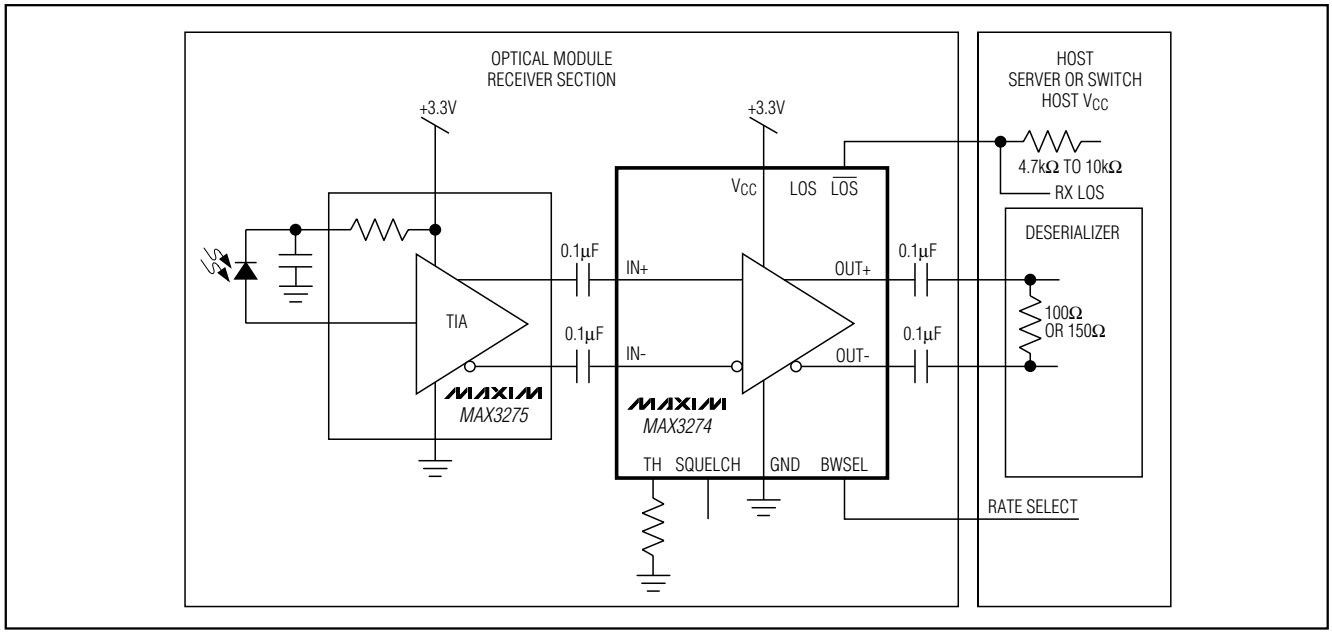
Features

- **Dual-Rate 1.0625Gbps/2.125Gbps Operation**
- **On-Chip Selectable 4th-Order Filter**
- **Relaxation Oscillation Suppression of Legacy, CD Laser-Based Transmitters**
- **Available in a 100Ω Output Termination**
- **Programmable Loss-of-Signal (LOS) Threshold**
- **Output Squelch Control**
- **Power-On Reset Minimizes Inrush Current**
- **4mm × 4mm 16-Pin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG. CODE
MAX3274UGE	0°C to +85°C	16 QFN	G1644-1

Typical Operating Circuit



Pin Configurations appear at end of data sheet.

Dual-Rate Fibre Channel Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....-0.5V to +6.0V
Continuous CML Output Current
(OUT+, OUT-) .....-25mA to +25mA
CML Input Voltage (IN+, IN-) .....-0.5V to (V_{CC} + 0.5V)
Differential Input Voltage (IN+, IN-).....2V_{P-P}
TTL Input Voltage
(BWSEL, SQUELCH, TEST).....-0.5V to (V_{CC} + 0.5V)
Voltage at TH .....-0.5V to V_{CC} + 0.5V
Current into TH.....5.0mA
Open Collector (LOS, $\overline{LOS}$).....-0.5V to +5.5V
Operating Ambient Temperature Range .....-40°C to +85°C
Storage Ambient Temperature Range.....-55°C to +100°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current				78	99	mA
Data Rate		BWSEL = 0		1.0625		Gbps
		BWSEL = 1		2.125		
Small-Signal Bandwidth		-3dB, BWSEL = 0 (Note 1)	0.77	0.89	1.0	GHz
		-15dB, BWSEL = 0 (Note 1)			2.0	
		-3dB, BWSEL = 1 (Note 1)		1.7		
BWSEL Response Time		(Note 2)			10	µs
Input Range	V_{IN}	(Notes 2, 3)	10		1200	mV_{P-P}
Deterministic Jitter		BWSEL = 0, 10mV ≤ input ≤ 20mV (Notes 2, 4)		44	60	ps_{P-P}
		BWSEL = 0, 20mV < input ≤ 1200mV (Notes 2, 4)		37	44	
		BWSEL = 1, 10mV ≤ input ≤ 1200mV (Notes 2, 4)		10	20	
Random Jitter		BWSEL = 0 (Notes 2, 5)		5.1		ps_{RMS}
		BWSEL = 1 (Notes 2, 5)		2.8		
Total Jitter		BWSEL = 0 (Note 6)		117		ps_{P-P}
		BWSEL = 1 (Note 6)		49		
LOS, $\overline{LOS}$ Transition Time		10% to 90% rise/fall time (Notes 2, 7)	5		350	ns
LOS, $\overline{LOS}$ Response Time		Figure 1 (Note 2)	1		20	µs
LOS, $\overline{LOS}$ Hysteresis		20 × log ($V_{DEASSERT}/V_{ASSERT}$), V_{TH} = 6mV_{P-P} (Note 8)	2		8	dB
		V_{TH} = 30mV_{P-P} (Notes 2, 8)	4		8	
LOS Assert (V_{LOS}) Range		330Ω < R_{TH} < 2.0kΩ (Notes 2, 8)	8		30	mV
LOS Assert (V_{LOS}) Error		330Ω < R_{TH} < 2.0kΩ (Notes 2, 8)	-30		+30	%
Squelch Input Current					100	µA
Single-Ended Input Resistance	R_{IN}	IN+, IN- to V_{CC}	40	50	60	Ω
Data Input VSWR		f < 2GHz (Note 2)			2.5	
Differential Output Resistance	R_{OUT}	OUT+ to OUT- (MAX3274)	80	100	120	Ω
CML Output Voltage	V_{OUT}	SQUELCH = 0 (Note 4)	900	1200	1600	mV_{P-P}
		SQUELCH = 1, V_{IN} < V_{TH} (Note 4)			30	
Data Output Levels		SQUELCH = 1, V_{IN} < V_{TH} (Note 4)	V_{CC} - 0.1		V_{CC}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Output Edge Speed		20% to 80%, BWSEL = 0 (Notes 2, 5)		170	220	ps_{P-P}
		20% to 80%, BWSEL = 1 (Notes 2, 5)		105	140	
LOS Current Sink		LOS asserted	1.0			mA
		LOS not asserted, V_{CC} = 0, 4.7kΩ pullup to +5.5V	0		10	µA
$\overline{LOS}$ Current Sink		LOS not asserted	1.0			mA
		LOS asserted, V_{CC} = 0, 4.7kΩ pullup to +5.5V	0		10	µA
LOS, $\overline{LOS}$ Output Low Voltage		LOS, $\overline{LOS}$ sink current = 1mA			0.5	V
Supply Noise Tolerance		10kHz ≤ f < 1MHz (Note 9)		40		mV_{P-P}
		1MHz ≤ f < 50MHz (Note 9)		20		

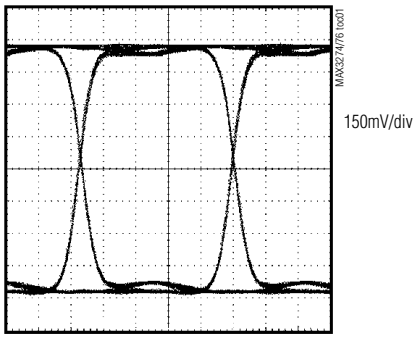
Note 1: Measured with a ≤-50dBm input signal on a network analyzer.
Note 2: Specifications are guaranteed by design and characterization.
Note 3: Using 2^7 - 1 PRBS pattern. The input bandwidth is limited to 0.75 × (selected data rate) by a 4th-order Bessel Thompson filter.
Note 4: Using a K28.5 pattern at the selected bit rate. Measured differentially into a matched external load.
Note 5: Using a K28.7 or equivalent pattern at the selected bit rate. Measured over the entire input voltage range.
Note 6: Total jitter is estimated as TJ = DJ + 14 x RJ, where DJ is the peak-to-peak deterministic jitter, and RJ is the RMS random jitter.
Note 7: LOS (open collector) is connected to a +5.5V supply through a 4.7kΩ external resistor.
Note 8: Using K28.7 or equivalent pattern at selected bit rate.
Note 9: Total jitter, deterministic jitter, LOS hysteresis, LOS assert performance verified.

Dual-Rate Fibre Channel Limiting Amplifier

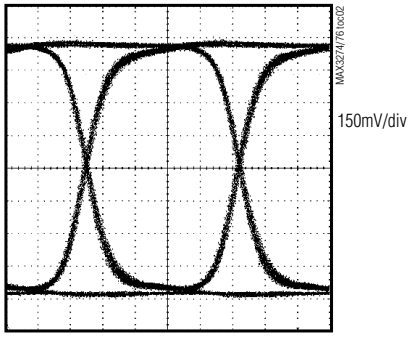
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

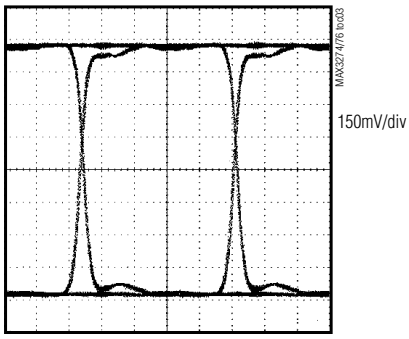
INPUT = 1.2V$_{P-P}$, 2^7 - 1 PRBS, BWSEL = 1



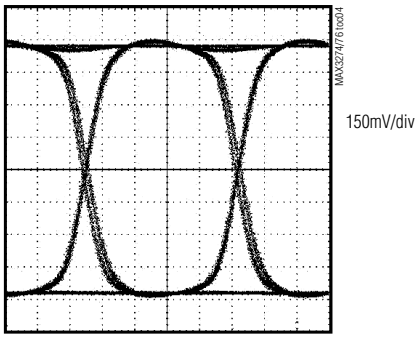
INPUT = 10mV$_{P-P}$, 2^7 - 1 PRBS, BWSEL = 1



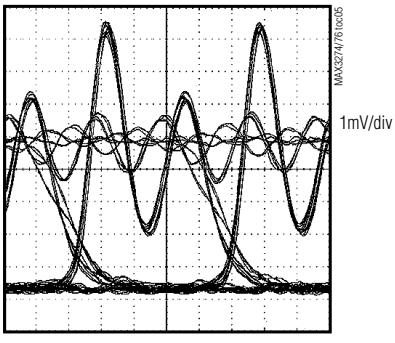
INPUT = 1.2V$_{P-P}$, 2^7 - 1 PRBS, BWSEL = 0



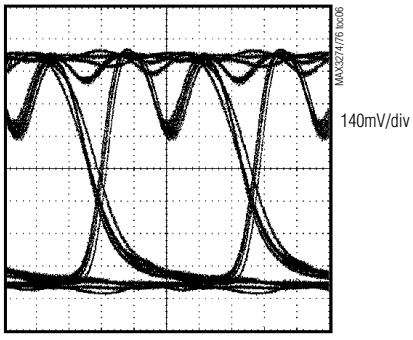
INPUT = 10mV$_{P-P}$, 2^7 - 1 PRBS, BWSEL = 0



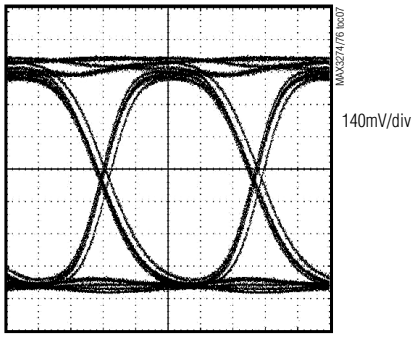
INPUT RELAXATION OSCILLATION (RO) OF LEGACY FIBRE CHANNEL TRANSMITTERS (INPUT = K28.5, 1.0625Gbps)



BWSEL = 1 RO NOT SUPPRESSED



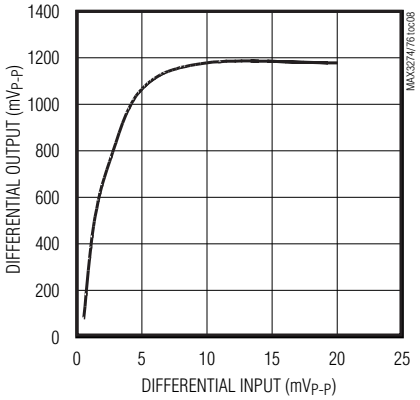
BWSEL = 0 RO FULLY SUPPRESSED



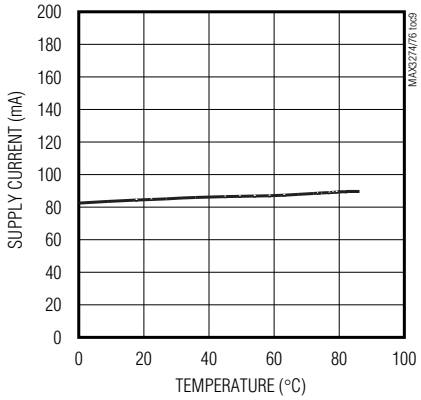
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

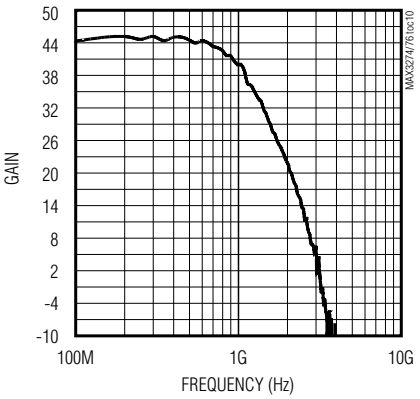
TRANSFER FUNCTION



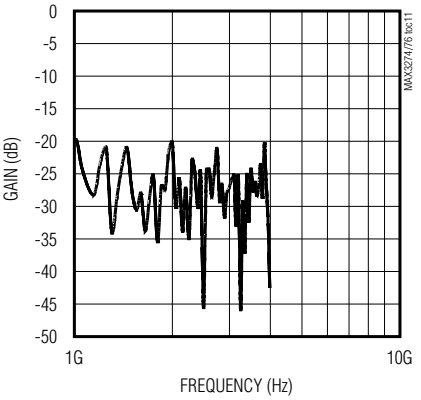
SUPPLY CURRENT vs. TEMPERATURE



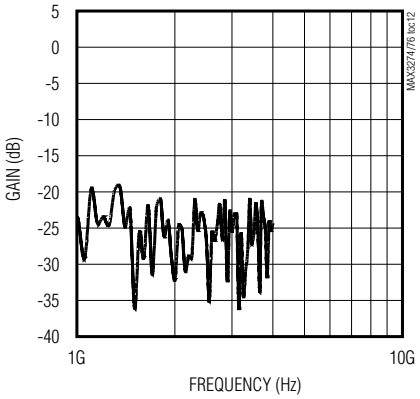
FORWARD DIFFERENTIAL GAIN (INPUT LEVEL of -60dBm, BWSEL = 0)



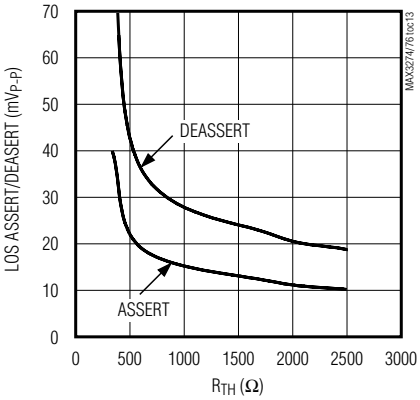
INPUT DIFFERENTIAL RETURN GAIN (SIGNAL LEVEL of -60dBm)



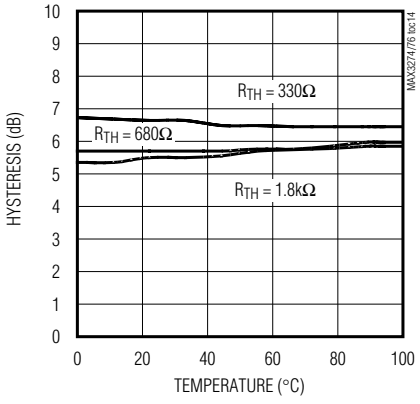
OUTPUT DIFFERENTIAL RETURN GAIN (SIGNAL LEVEL of -60dBm)



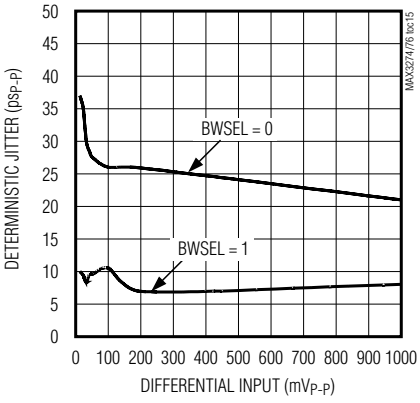
ASSERT/DEASSERT LEVELS vs. R_{TH} (BWSEL = 1, 2.125Gbps, K28.5)



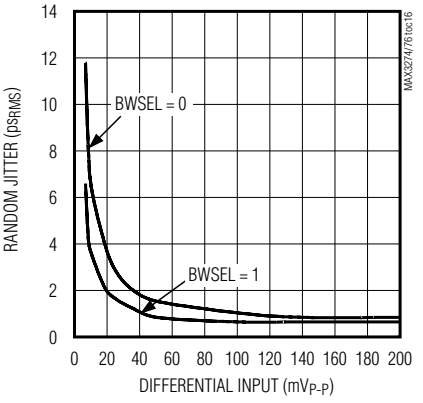
LOS HYSTERESIS vs. TEMPERATURE (BWSEL = 1, 2.125Gbps, K28.5)



DETERMINISTIC JITTER



RANDOM JITTER



Dual-Rate Fibre Channel Limiting Amplifier

Pin Description

PIN	NAME	FUNCTION
1	IN+	Noninverted Data Input
2	IN-	Inverted Data Input
3, 7, 10	V_{CC}	Supply Voltage
4	BWSEL	Bandwidth Select Pin. When BWSEL is set to a TTL-low level or left open, a 4th-order Bessel Thompson filter suppresses relaxation oscillations from legacy CD laser transmitters. Connect BWSEL to a TTL-high for operation above 1.0625Gbps.
5	TEST	Test Pin Should Be Connected to Ground
6	SQUELCH	Squelch Input. The squelch function is disabled when SQUELCH is set to a TTL-low. When SQUELCH is set to a TTL-high level, and LOS is asserted, the data outputs (OUT+ and OUT-) are forced to static levels.
8, 13, 16	GND	Supply Ground
9	TH	Loss-of-Signal Threshold. A resistor connected from this pin to ground sets the input signal level at which the loss-of-signal (LOS) outputs are asserted. See the *Typical Operating Characteristics* and *Design Procedure* sections for more information.
11	OUT-	Inverted Data Output
12	OUT+	Noninverted Data Output
14	$\overline{LOS}$	Inverted Loss-of-Signal Output. $\overline{LOS}$ is high when the level of the input signal is above the preset threshold set by the TH pin. $\overline{LOS}$ is asserted low when the input signal level drops below the threshold.
15	LOS	Loss-of-Signal Output. LOS is low when the level of the input signal is above the preset threshold set by the TH pin. LOS is asserted high when the input signal level drops below the threshold.
EP	Exposed Pad	Ground. The exposed paddle must be soldered to the circuit board ground for proper thermal and electrical performance.

Detailed Description

Figure 2 is a functional diagram of the MAX3274 limiting amplifier. Typical gain is 46dB. A linear input drives a bandwidth selector. An offset correction loop with lowpass filtering ensures low deterministic jitter. An integrated RMS signal detector monitors for loss-of-signal conditions. The output buffer provides a limited CML output signal.

Input Buffer

The MAX3274 input buffer (Figure 3) provides a 100Ω input impedance between IN+ and IN-. DC-coupling the inputs is not recommended; doing so prevents proper functioning of DC offset correction circuitry.

Signal Detect and Loss-of-Signal

An RMS signal detector looks at the signal from the input buffer and compares it to a threshold set by a resistor at pin TH. The status of the signal-detect information appears at the LOS outputs. These are open-collector outputs and require external pullup resistors connected to the host power supply. The LOS outputs are high impedance when the power supply to the MAX3274 is 0V. ESD protection on the dual-rate limiting amplifiers' LOS outputs do not forward-bias when the power supply of the MAX3274 is 0V or below the host power supply.

Offset Correction

A low-frequency feedback loop is integrated into the limiting amplifiers to reduce input offset and thereby minimize duty-cycle distortion. For proper operation, the input must be externally AC-coupled. The offset correction circuit has been optimized for the Fibre Channel character set, disparity rules, and 8b/10b data encoding. This dictates an average data input mark density of 50% and a maximum run length of five consecutive identical digits (CID) or bits.

CML Output Buffer

The MAX3274 CML outputs (Figure 4) provide high tolerance to impedance mismatches and inductive connectors. The output current is approximately 24mA. The squelch function is enabled when SQUELCH is set to a TTL-high level or connected to V_{CC}. The squelch function holds OUT+ and OUT- at a static voltage when the input signal level drops below the loss-of-signal threshold. The output buffer can be AC- or DC-coupled to the load. For DC operation, the load must be terminated to V_{CC} of the MAX3274.

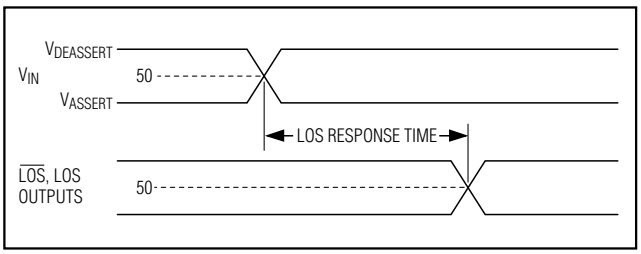


Figure 1. LOS Response Time

Design Procedure

Programming the LOS Assert Threshold

External resistor R_{TH} programs the loss-of-signal threshold. See the LOS Threshold vs. R_{TH} graph in the *Typical Operating Characteristics* section. R_{TH} can be estimated by $R_{TH} = 15 / V_{TH}$, where V_{TH} is the peak-to-peak differential input assert level.

Selecting the AC-Coupling Capacitors

The input and output AC-coupling capacitors (C_{IN}, C_{OUT}) should be selected to minimize the receiver's deterministic jitter. Lowering the low-frequency cutoff reduces deterministic jitter. The low-frequency cutoff can be determined by:

$$f_C = \frac{1}{2\pi \times C \times (R_L + R_S)}$$

where R_L is the single-ended load impedance and R_S is the single-ended source impedance. C_{IN}, C_{OUT} = 0.1µF is recommended.

Applications Information

Optical Hysteresis

In an optical receiver, the electrical power change at the limiting amplifier is 2 times the optical power change. For example, if a receiver's optical input power (χ) increases by a factor of 2, and the preamplifier is linear, then the voltage input to the limiting amplifier also increases by a factor of 2. The optical power change is 10log ($2\chi/\chi$) = 10log(2) = 3dB. At the limiting amplifier, the electrical power change is:

$$10\log\frac{(2V_{IN})^2 / R_{IN}}{V_{IN}^2 / R_{IN}} = 10\log\left(2^2\right) = 20\log(2) = 6\text{dB}$$

The typical voltage hysteresis for the MAX3274 is 6dB. This provides an optical hysteresis of 3dB.

Dual-Rate Fibre Channel Limiting Amplifier

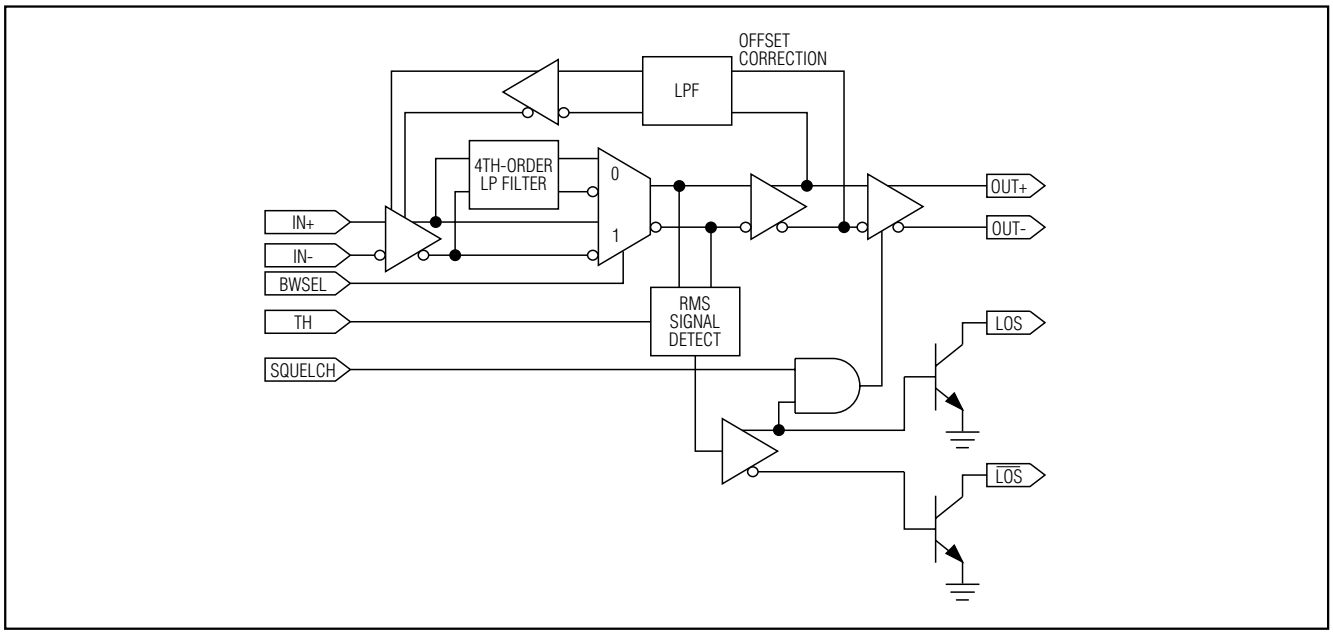


Figure 2. Functional Diagram of the MAX3274 Limiting Amplifier

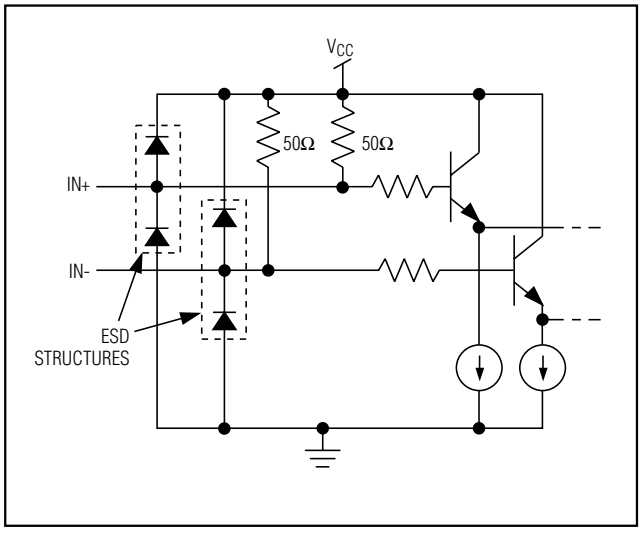


Figure 3. Input Circuit

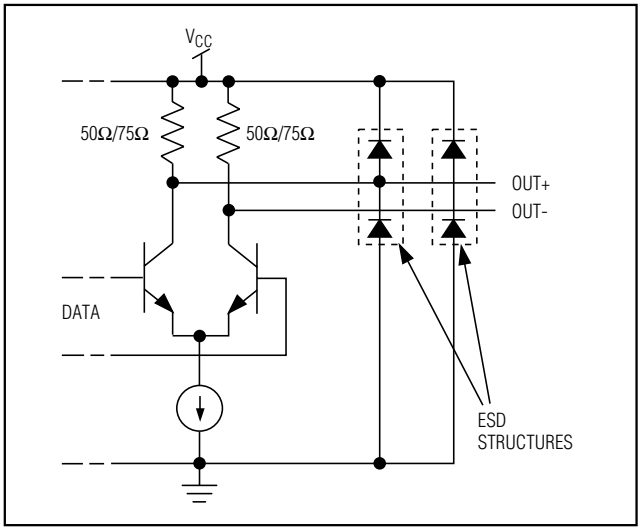
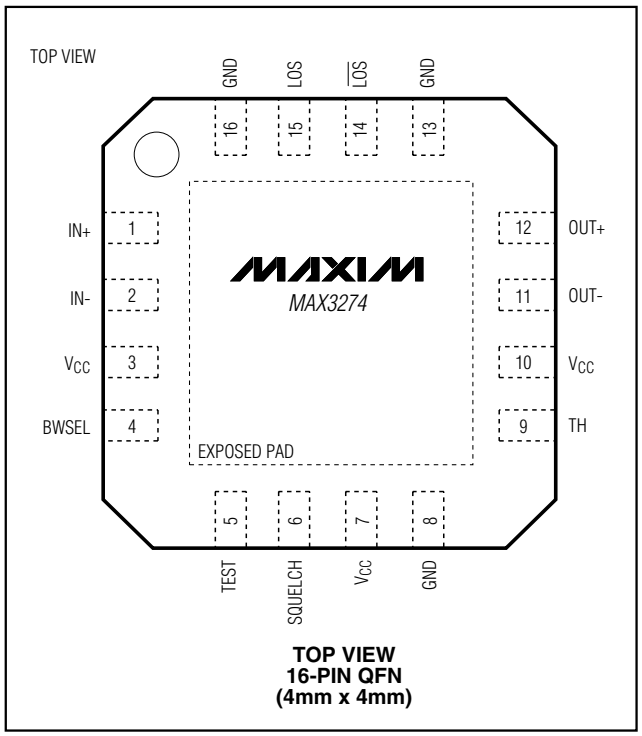


Figure 4. CML Output Circuit

Dual-Rate Fibre Channel Limiting Amplifier

Pin Configuration



TOP VIEW
16-PIN QFN
(4mm x 4mm)

Chip Information

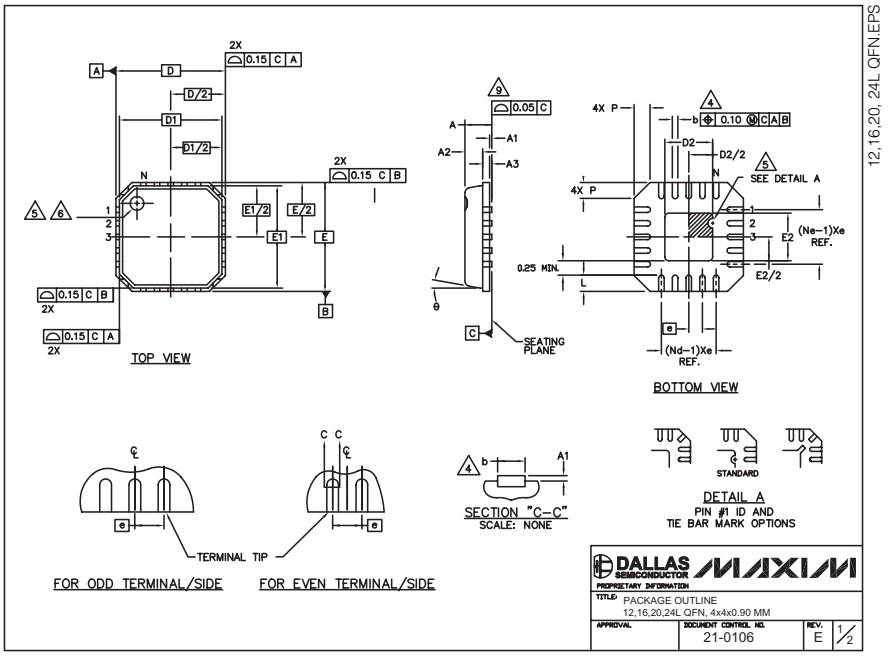
DEVICE COUNT: 2855

TRANSISTOR COUNT: 1310

PROCESS: BiPOLAR: SiGe, SOI

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. THIS PACKAGE OUTLINE APPLIES TO PUNCHED QFN (STEPPED SIDES).

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ	0°	–	12°	
P	0.24	0.42	0.60	

SYMBOL	PITCH VARIATION A MIN.	NOM.	MAX.	NOTE	SYMBOL	PITCH VARIATION B MIN.	NOM.	MAX.	NOTE	SYMBOL	PITCH VARIATION C MIN.	NOM.	MAX.	NOTE	SYMBOL	PITCH VARIATION D MIN.	NOM.	MAX.	NOTE
e	0.80 BSC				e	0.65 BSC				e	0.50 BSC				e	0.50 BSC			
N		12		3	N		16		3	N		20		3	N		24		3
Nd		3		3	Nd		4		3	Nd		5		3	Nd		6		3
Ne		3		3	Ne		4		3	Ne		5		3	Ne		6		3
L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.30	0.40	0.50	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

PKG. CODE	EXPOSED PAD VARIATION D2 MIN.	NOM.	MAX.	E2 MIN.	NOM.	MAX.
G1244-2	1.95	2.10	2.25	1.95	2.10	2.25
G1644-1	1.95	2.10	2.25	1.95	2.10	2.25
G2044-3	1.95	2.10	2.25	1.95	2.10	2.25
G2044-4	1.55	1.70	1.85	1.55	1.70	1.85
G2444-1	1.95	2.10	2.25	1.95	2.10	2.25

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN, 4x4x0.90 MM
APPROVAL
DOCUMENT CONTROL NO. 21-0106
REV. E
2/2

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