



+3.3V, 622Mbps, SDH/SONET 8:1 Serializer with Clock Synthesis and TTL Inputs

MAX3690

General Description

The MAX3690 serializer is ideal for converting 8-bit-wide, 77Mbps parallel data to 622Mbps serial data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts TTL clock and data inputs, and delivers a 3.3V differential PECL serial-data output. A fully integrated PLL synthesizes an internal 622MHz serial clock from a low-speed crystal reference clock (77.76MHz, 51.84MHz, or 38.88MHz).

The MAX3690 is available in the extended-industrial temperature range (-40°C to +85°C) in a 32-pin TQFP package.

Applications

622Mbps SDH/SONET Transmission Systems

622Mbps ATM/SONET Access Nodes

Add/Drop Multiplexers

Digital Cross Connects

Features

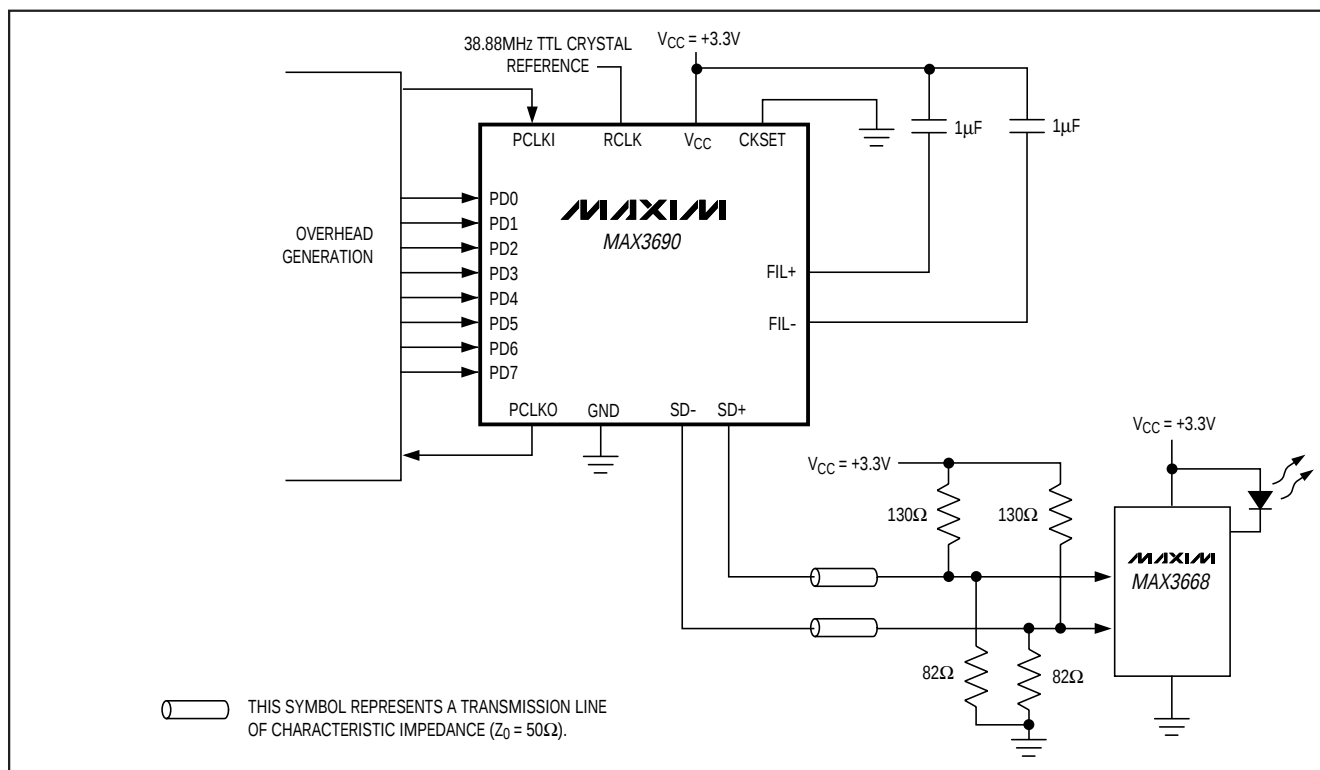
- ◆ Selectable Reference Clock Frequency: 77.76MHz, 51.84MHz, or 38.88MHz
- ◆ Single +3.3V Supply
- ◆ 77Mbps (8-bit) Parallel to 622Mbps Serial Conversion
- ◆ Clock Synthesis for 622Mbps Serial Data
- ◆ 200mW Power
- ◆ TTL Parallel Clock and Data Inputs
- ◆ Differential 3.3V PECL Serial-Data Output

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3690ECJ	-40°C to +85°C	32 TQFP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)	Continuous Power Dissipation ($T_A = +85^\circ\text{C}$)
VCC -0.5V to +5V	TQFP (derate 10.2mW/ $^\circ\text{C}$ above $+85^\circ\text{C}$) 663mW
All Inputs, FIL-, FIL+, PCLKO -0.5V to (VCC + 0.5V)	Operating Temperature Range -40°C to $+85^\circ\text{C}$
Output Current	Storage Temperature Range -60°C to $+160^\circ\text{C}$
PECL Outputs (SD $\pm$) 50mA	Lead Temperature (soldering, 10sec) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(VCC = +3.0V to +3.6V, PECL loads = $50\Omega \pm 1\%$ to (VCC - 2V), $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at VCC = +3.3V, $T_A = +25^\circ\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I _{CC}	PECL outputs unterminated		60	100	mA
CKSET Input Current	I _{CKSET}	CKSET = 0 or V _{CC}			500	μA
PECL OUTPUTS (SD±)						
Output High Voltage	V _{OH}	T _A = 0°C to +85°C	V _{CC} - 1.025	V _{CC} - 0.88		V
		T _A = -40°C	V _{CC} - 1.085	V _{CC} - 0.88		
Output Low Voltage	V _{OL}	T _A = 0°C to +85°C	V _{CC} - 1.81	V _{CC} - 1.62		V
		T _A = -40°C	V _{CC} - 1.83	V _{CC} - 1.555		
TTL INPUTS AND OUTPUTS (PCLKI, RCLK, PCKO, PD_)						
Input High Voltage	V _{IH}		2.0			V
Input Low Voltage	V _{IL}				0.8	V
Input High Current	I _{IH}	V _{IN} = V _{CC}	-10		10	μA
Input Low Current	I _{IL}	V _{IN} = 0	-10		10	μA
Output High Voltage	V _{OH}	I _{OH} = 400μA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = -400μA			0.44	V

AC ELECTRICAL CHARACTERISTICS

(VCC = +3.0V to +3.6V, PECL loads = $50\Omega \pm 1\%$ to (VCC - 2V), all TTL thresholds set to VCC/2, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at VCC = +3.3V, $T_A = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Rate	f _{CLK}			622.08		MHz
Parallel Data Setup Time	t _{SU}		1200			ps
Parallel Data Hold Time	t _H		1000			ps
Allowable Parallel Clock Output to Parallel Clock Input Delay	t _{SKEW}		0		5.0	ns
Output Random Jitter	Φ_0				11	psRMS
PECL Differential Output Rise/Fall Time	t _R , t _F	20% to 80%		200		ps
TTL Output Rise Time	t _R	C _{LOAD} = 15pF, V _{OUT} = 0.8V to 2.0V		650		ns
TTL Output Fall Time	t _F	C _{LOAD} = 15pF, V _{OUT} = 0.8V to 2.0V		550		ns

Note 1: AC characteristics guaranteed by design and characterization.

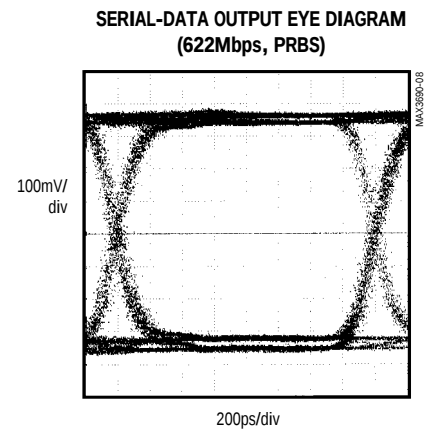
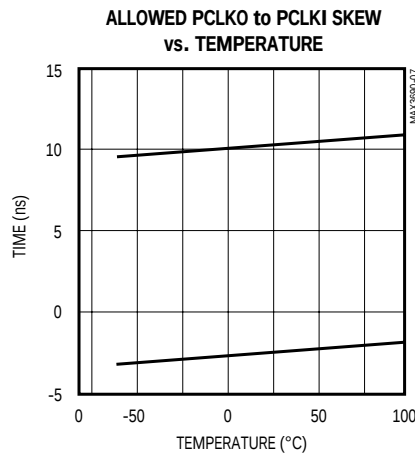
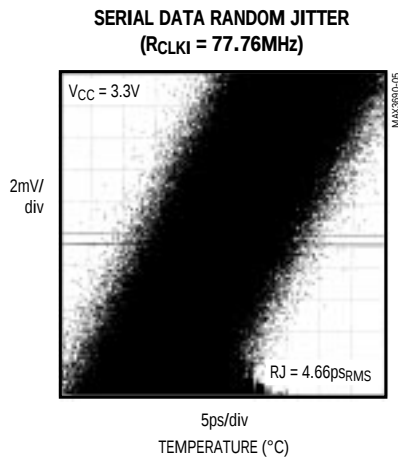
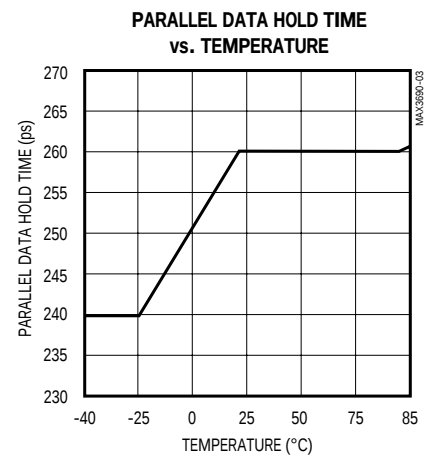
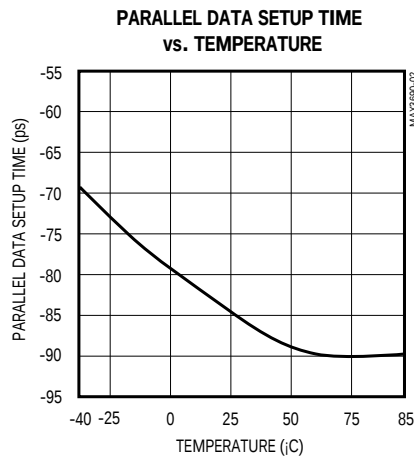
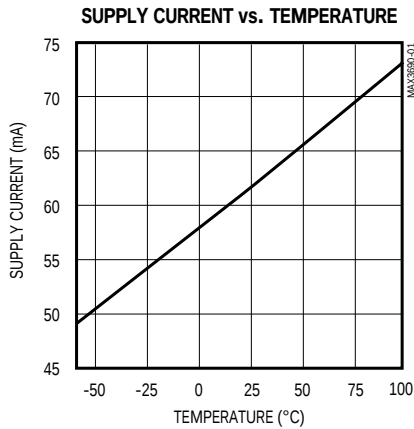
Note 2: All TTL thresholds set to VCC / 2.

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Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

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Pin Description

PIN	NAME	FUNCTION
1–8	PD0–PD7	TTL Parallel-Data Inputs. Data is clocked in on the PCLKI signal's positive transition.
9, 10, 17, 18, 19, 24, 25, 26, 31, 32	GND	Ground
11	PCLKO	TTL Parallel-Clock Output. Use positive transition of PCLKO to clock the overhead management circuit.
12, 13, 16, 21, 28, 29	VCC	+3.3V Supply Voltage
14	SD-	Inverting PECL Serial-Data Output
15	SD+	Noninverting PECL Serial-Data Output
20	CKSET	Reference Clock Rate Programming Pin. CKSET = open: Reference clock rate = 77.76MHz CKSET = 20k Ω to GND: Reference clock rate = 51.84MHz CKSET = GND: Reference clock rate = 38.88MHz
22	FIL-	Filter Capacitor Input. Connect a 1 μ F capacitor between FIL- and VCC.
23	FIL+	Filter Capacitor Input. Connect a 1 μ F capacitor between FIL+ and VCC.
27	RCLK	TTL Reference-Clock Input. Connect a crystal reference clock (77.76MHz, 51.84MHz or 38.88MHz) to the RCLK input. The active edge is the positive transitioning edge.
30	PCLKI	TTL Parallel-Clock Input. Connect the incoming parallel-data-clock signal to the PCLKI input. The active edge is the positive transitioning edge.

Detailed Description

The MAX3690 serializer comprises an 8-bit parallel input register, an 8-bit shift register, control and timing logic, a PECL output buffer, TTL input/output buffers, and a frequency-synthesizing PLL (consisting of a phase/frequency detector, loop filter/amplifier, voltage-controlled oscillator, and programmable prescaler). This device converts 8-bit-wide, 77Mbps parallel data to 622Mbps serial data (Figure 1).

The PLL synthesizes an internal 622MHz reference used to clock the output shift register. This clock is generated by locking onto the external crystal reference clock signal (RCLK) operating at either 77.76MHz, 51.84MHz, or 38.88MHz. The incoming par-

allel data is clocked into the MAX3690 on the rising transition of the parallel-clock-input signal (PCLKI). The control and timing logic ensure proper operation if the parallel-input register is latched within a window of time that is defined with respect to the parallel-clock-output signal (PCLKO). PCLKO is the synthesized 622MHz internal serial-clock signal divided by eight. Parallel-clock output to parallel-clock-input delay (skew) must be observed. Figure 2 shows the timing diagram.

PECL Outputs

The serial-data PECL outputs (SD+, SD-) require 50 Ω DC termination to (VCC - 2V). See the *Alternative PECL-Output Termination* section.

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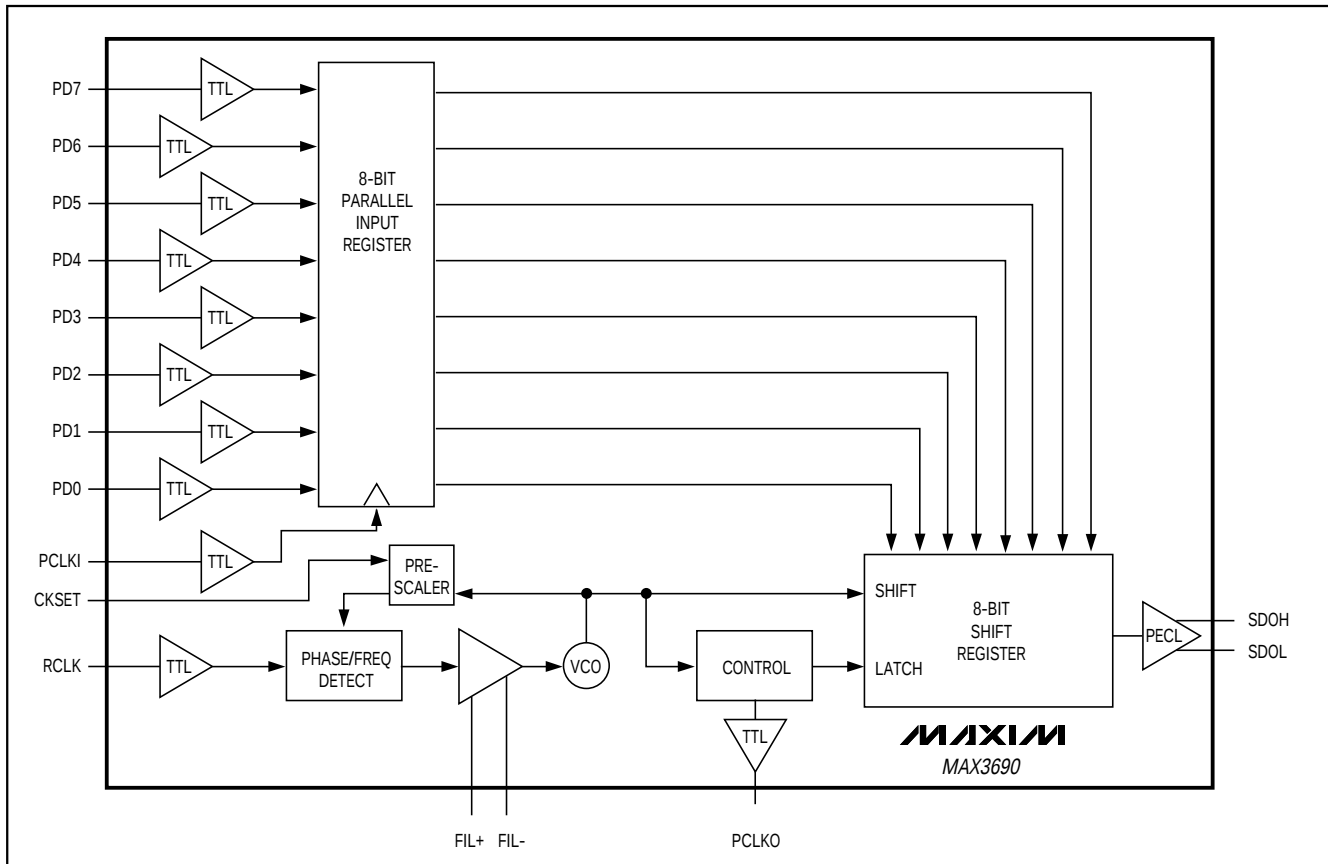


Figure 1. Functional Diagram

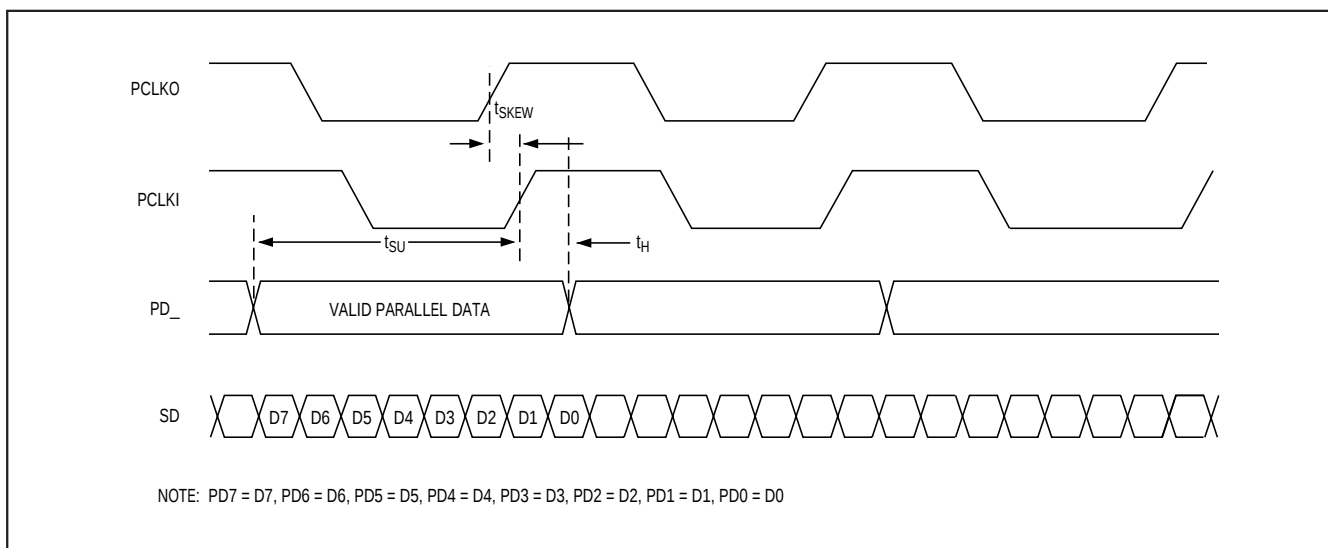


Figure 2. Timing Diagram

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Applications Information

Alternative PECL-Output Termination

Figure 3 shows alternative PECL-output-termination methods. Use Thevenin-equivalent termination when a ($V_{CC} - 2V$) termination voltage is not available. If AC coupling is necessary, be sure that the coupling capacitor is placed following the 50Ω or Thevenin-equivalent DC termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3690 data outputs.

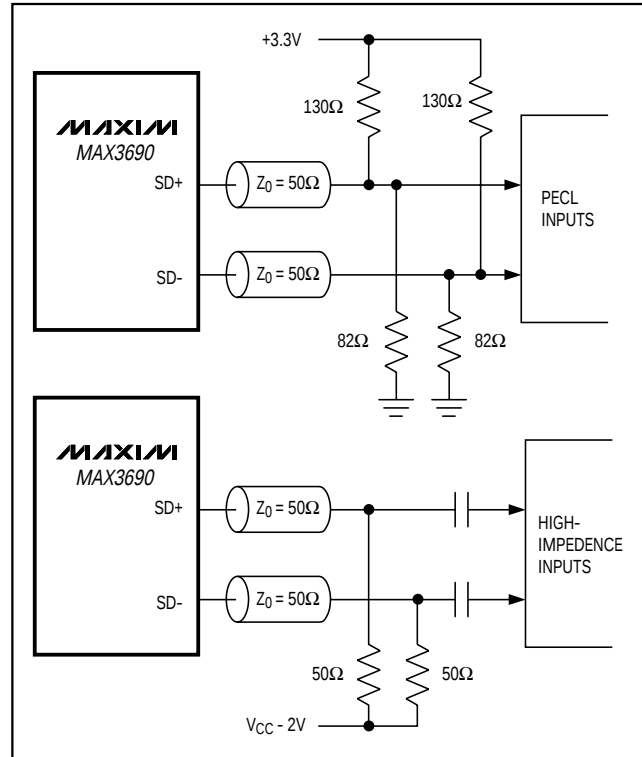
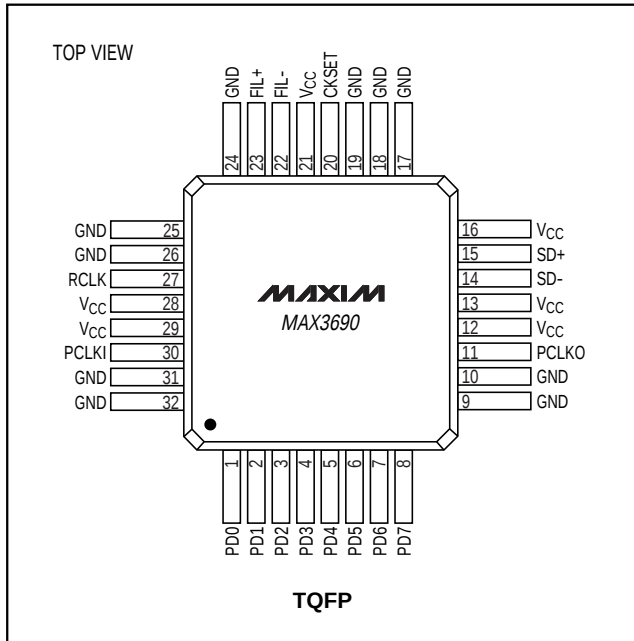


Figure 3. Alternative PECL-Output Termination

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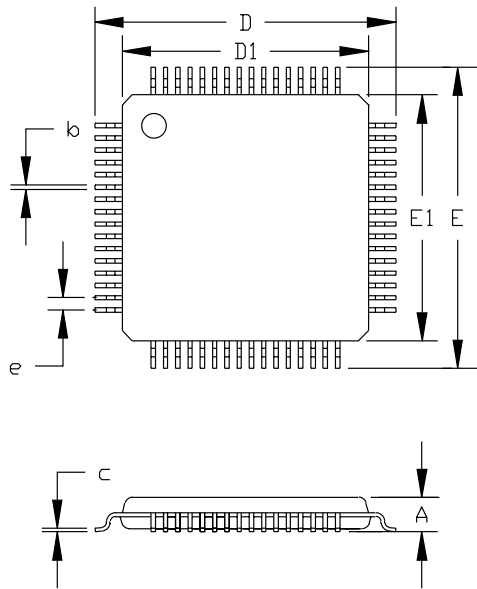
Pin Configuration



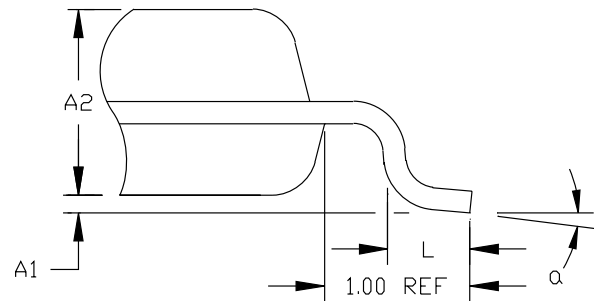
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Package Information



JEDEC VARIATION						
	BC		BE		BJ	
	32 LEAD		48 LEAD		64 LEAD	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60	---	1.60
A ₁	0.05	0.15	0.05	0.15	0.05	0.15
A ₂	1.35	1.45	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10	12.00	BSC.
D ₁	7.00	BSC.	7.00	BSC.	10.00	BSC.
E	8.90	9.10	8.90	9.10	12.00	BSC.
E ₁	7.00	BSC.	7.00	BSC.	10.00	BSC.
e	0.8	BSC.	0.5	BSC.	0.5	BSC.
L	0.45	0.75	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°	0°	7°



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC, BE AND BJ.

MAXIM			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, TQFP			
APPROVAL	DOCUMENT CONTROL NO.	REV	1/1
	21-0054	C	

TOPPOLEPS

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