19-1207; Rev 0; 3/97

EVALUATION KIT AVAILABLE

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

General Description

The MAX3691 serializer is ideal for converting 4-bit-wide, 155Mbps parallel data to 622Mbps serial data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts low-voltage differential-signal (LVDS) clock and data inputs for interfacing with high-speed digital circuitry, and delivers a 3.3V PECL serial-data output. A fully integrated PLL synthesizes an internal 622Mbps serial clock from a 155.52MHz reference clock.

The MAX3691 is available in the extended-industrial temperature range (-40°C to +85°C), in a 32-pin TQFP package.

Applications

622Mbps SDH/SONET Transmission Systems

622Mbps ATM/SONET Access Nodes

Add/Drop Multiplexers

Digital Cross Connects

Features

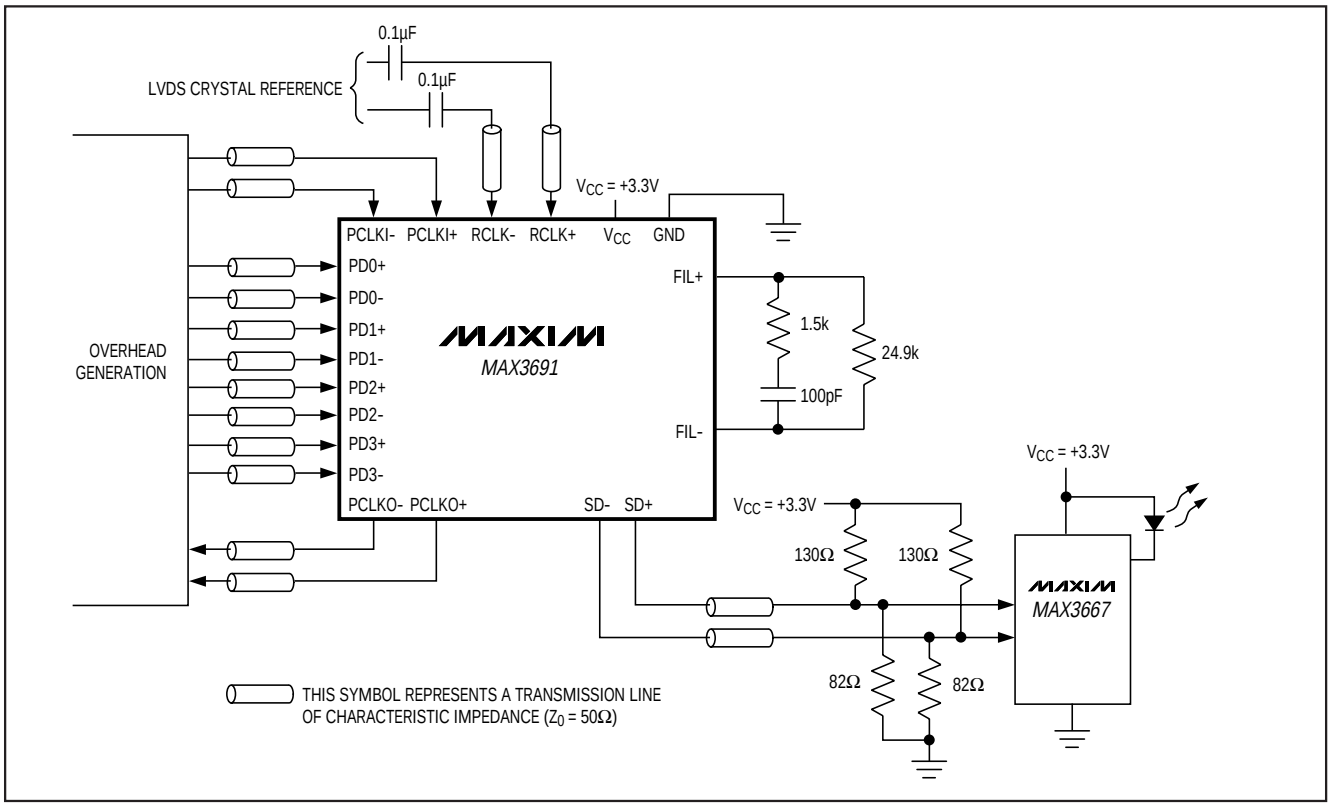
- **Single +3.3V Supply**
- **155Mbps Parallel to 622Mbps Serial Conversion**
- **215mW Power**
- **LVDS Parallel Clock and Data Inputs**
- **Differential 3.3V PECL Serial-Data Output**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3691ECJ	-40°C to +85°C	32 TQFP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} .....-0.5V to 5V
- All Inputs.....-0.5V to (V_{CC} + 0.5V)

Output Current
- LVDS Outputs (PCLKO±).....10mA
- PECL Outputs (SD±).....50mA

Continuous Power Dissipation (T_A = +85°C)
- TQFP (derate 10.20mW/°C above +85°C).....663mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential LVDS loads = 100Ω ±1%, PECL loads = 50Ω ±1% to (V_{CC} - 2V), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	PECL outputs unterminated	38	65	100	mA
PECL OUTPUTS (SD±)						
Output High Voltage	V_{OH}	T_A = +25°C to +85°C	V_{CC} - 1.03		V_{CC} - 0.88	V
		T_A = -40°C	V_{CC} - 1.08		V_{CC} - 0.88	
Output Low Voltage	V_{OL}	T_A = +25°C to +85°C	V_{CC} - 1.81		V_{CC} - 1.62	V
		T_A = -40°C	V_{CC} - 1.95		V_{CC} - 1.62	
LVDS INPUTS AND OUTPUTS (PCLKI±, RCLK±, PCLKO±, PD_±)						
Input Voltage Range	V_I	Differential input voltage = 100mV	0		2.4	V
Differential Input Threshold	V_{IDTH}	Common-mode voltage = 50mV	-100		100	mV
Threshold Hysteresis	V_{HYST}			70		mV
Differential Input Resistance	R_{IN}		85	100	115	Ω
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	V_{OD}		250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	ΔV_{OD}				25	mV
Output Offset Voltage	V_{OS}	T_A = +25°C	1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	ΔV_{OS}				25	mV
Single-Ended Output Resistance	R_O		40	70	140	Ω
Change in Magnitude of Single-Ended Output Resistance for Complementary States	ΔR_O			±1	±10	%

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential LVDS load = 100Ω ±1%, PECL loads = 50Ω ±1% to (V_{CC} - 2V) T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V.) (Note 1)

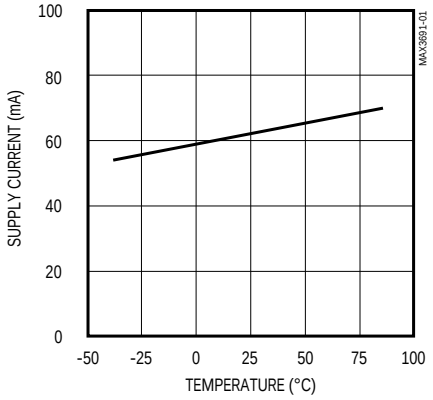
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Rate	f_{SCLK}			622.08		MHz
Parallel Data-Setup Time	t_{SU}		200			ps
Parallel Data-Hold Time	t_H		600			ps
PCLKO to PCLKI Skew	t_{SKEW}		-0.7		+3.3	ns
Output Jitter	Φ_0	T_A = -40°C to +85°C (Note 2)			13	ps_{RMS}
PECL Differential Output Rise/Fall Time	t_R, t_F			400		ps

Note 1: AC characteristics guaranteed by design and characterization.
Note 2: Assumes a 50% duty cycle ±5%.

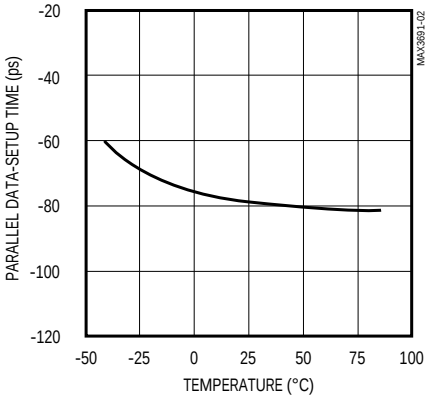
Typical Operating Characteristics

(V_{CC} = +3.0V to +3.6V, differential LVDS loads = 100Ω, unless otherwise noted.)

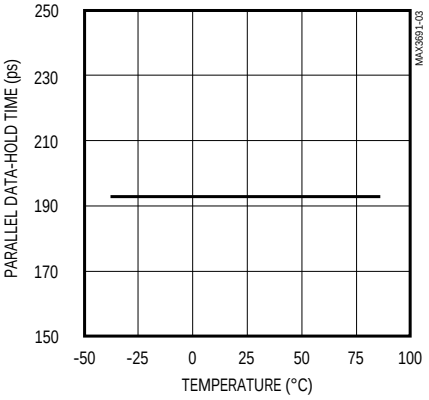
SUPPLY CURRENT vs. TEMPERATURE



PARALLEL DATA-SETUP TIME vs. TEMPERATURE



PARALLEL DATA-HOLD TIME vs. TEMPERATURE

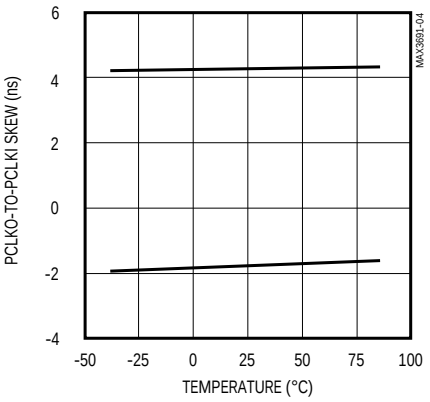


+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

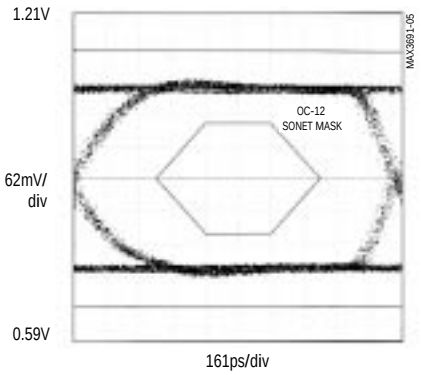
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, differential LVDS loads = 100Ω, unless otherwise noted.)

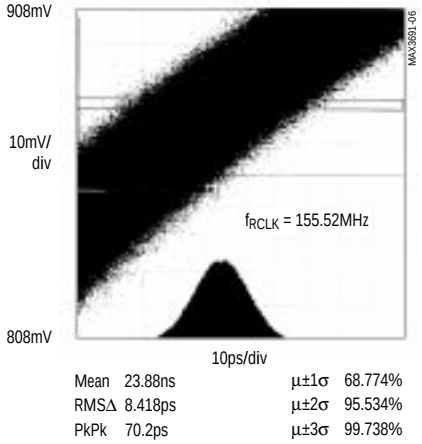
PCLKO-to-PCLKI SKEW vs. TEMPERATURE



SERIAL-DATA OUTPUT EYE DIAGRAM (622Mbps, 2^7-1 PRBS)



SERIAL-DATA OUTPUT JITTER



Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7	PD0+ to PD3+	Noninverting LVDS Parallel Data Inputs. Data is clocked in on the PCLKI signal's positive transition.
2, 4, 6, 8	PD0- to PD3-	Inverting LVDS Parallel Data Inputs. Data is clocked in on the PCLKI signal's positive transition.
9, 17, 18, 19, 24, 25, 32	GND	Ground
10	PCLKO-	Inverting LVDS Parallel-Clock Output. Use PCLKO to clock the overhead management circuit.
11	PCLKO+	Noninverting LVDS Parallel-Clock Output. Use PCLKO to clock the overhead management circuit.
12, 13, 16, 20, 21, 28, 29	V_{CC}	+3.3V Supply Voltage
14	SD-	Inverting PECL Serial-Data Output
15	SD+	Noninverting PECL Serial-Data Output
22	FIL-	Filter Capacitor Input. See *Typical Operating Circuit* for external-component connections.
23	FIL+	Filter Capacitor Input. See *Typical Operating Circuit* for external-component connections.
26	RCLK+	Noninverting LVDS Reference Clock Input. Connect (AC couple) a crystal reference clock (155.52MHz) to the RCLK inputs.
27	RCLK-	Inverting LVDS Reference Clock Input. Connect (AC couple) a crystal reference clock (155.52MHz) to the RCLK inputs.
30	PCLKI+	Noninverting LVDS Parallel Clock Input. Connect the incoming parallel-data-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.
31	PCLKI-	Inverting LVDS Parallel Clock Input. Connect the incoming parallel-data-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.

Detailed Description

The MAX3691 serializer comprises a 4-bit parallel input register, a 4-bit shift register, control and timing logic, a PECL output buffer, LVDS input/output buffers, and a frequency-synthesizing PLL (consisting of a phase/frequency detector, loop filter/amplifier, and voltage-controlled oscillator). This device converts 4-bit-wide, 155Mbps data to 622Mbps serial data (Figure 1).

The PLL synthesizes an internal 622Mbps reference used to clock the output shift register. This clock is generated by locking onto the external 155.52MHz reference-clock signal (RCLK).

The incoming parallel data is clocked into the MAX3691 on the rising transition of the parallel-clock-input signal (PCLKI). The control and timing logic ensure proper operation if the parallel-input register is latched within a window of time that is defined with respect to the parallel-clock-output signal (PCLKO). PCLKO is the synthesized 622Mbps internal serial-clock signal divided by four. The allowable PCLKO-to-PCLKI skew is -0.7ns to +3.3ns. This defines a timing window at about the PCLKO rising edge, during which a PCLKI rising edge may occur. Figure 2 is the timing diagram.

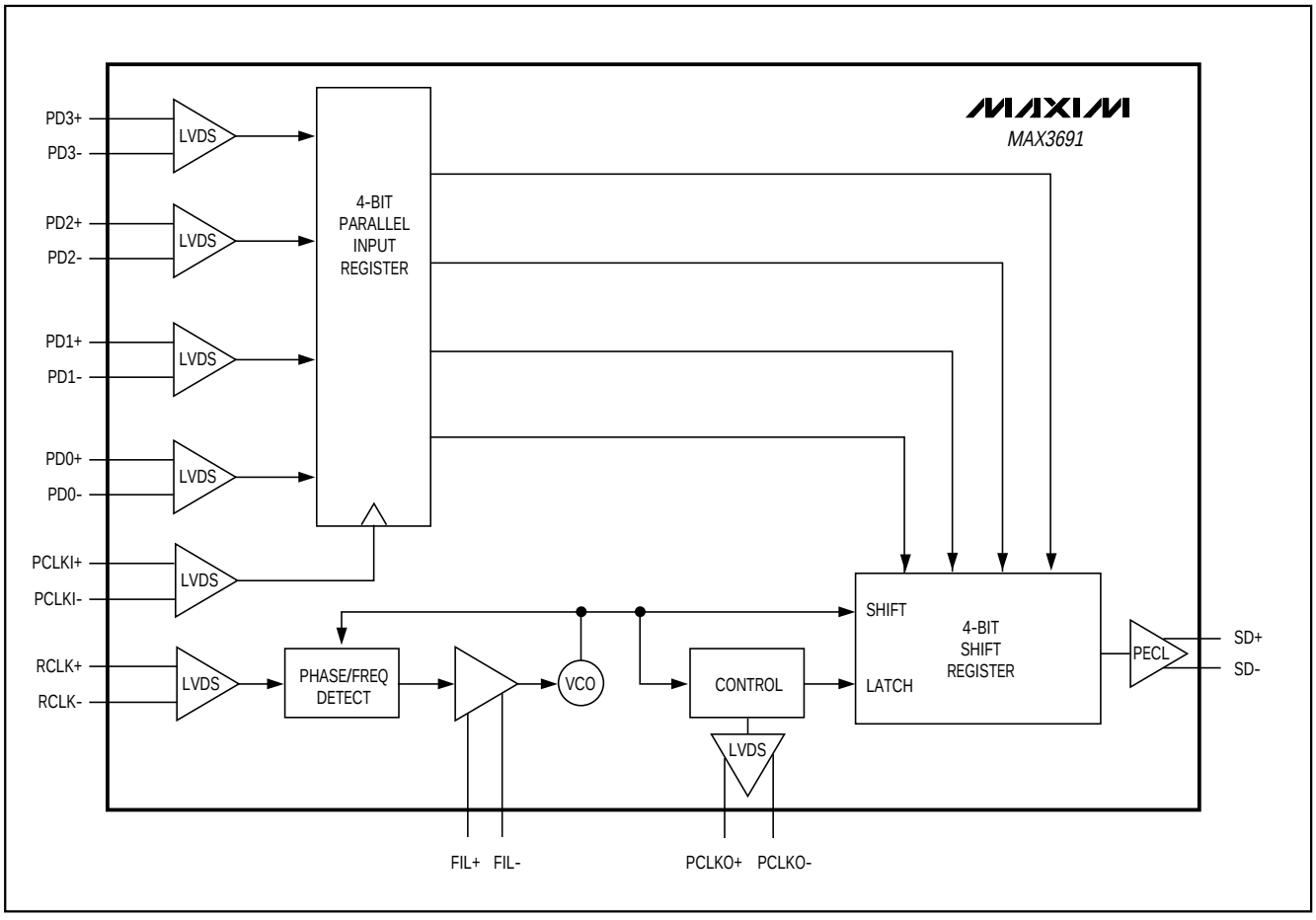


Figure 1. Functional Diagram

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

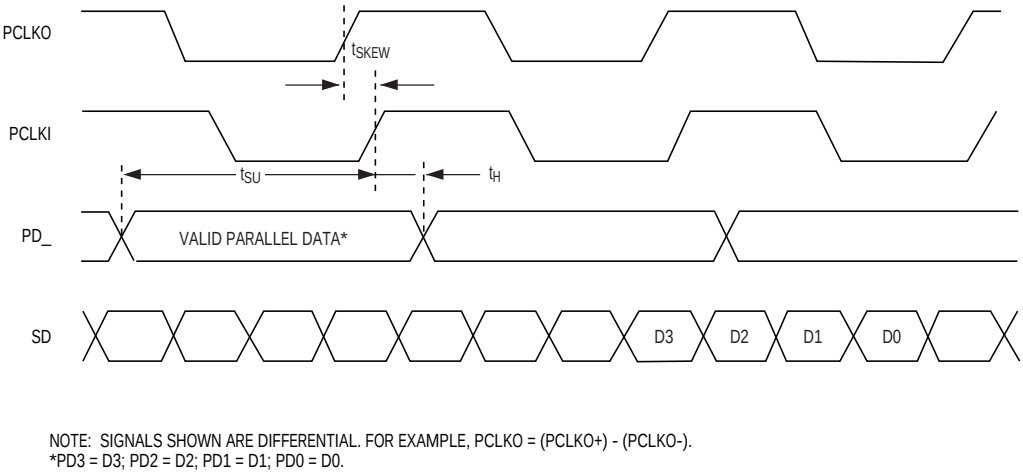


Figure 2. Timing Diagram

Low-Voltage Differential-Signal (LVDS) Inputs and Outputs

The MAX3691 features LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 250mV–400mV differential low-voltage swings to achieve fast transition times, minimized power dissipation, and noise immunity.

For proper operation, the parallel-clock LVDS outputs (PCLKO+, PCLKO-) require 100Ω differential DC termination between the inverting and noninverting outputs. Do not terminate these outputs to ground.

The parallel data and parallel clock LVDS inputs (PD_+, PD_-, PCLKI+, PCLKI-) are internally terminated with 100Ω differential input resistance, and therefore do not require external termination.

PECL Outputs

The serial-data PECL outputs (SD+, SD-) require 50Ω DC termination to (V_{CC} - 2V). See the *Alternative PECL-Output Termination* section.

Applications Information

Alternative PECL-Output Termination

Figure 3 shows alternative PECL output-termination methods. Use Thevenin-equivalent termination when a (V_{CC} - 2V) termination voltage is not available. If AC coupling is necessary, be sure that the coupling capacitor is placed following the 50Ω or Thevenin-equivalent DC termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3691 clock and data inputs and outputs.

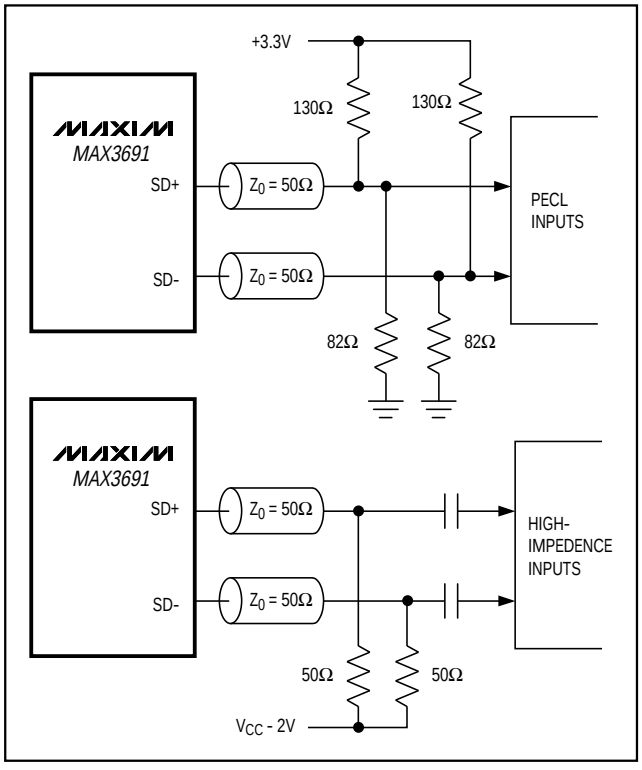
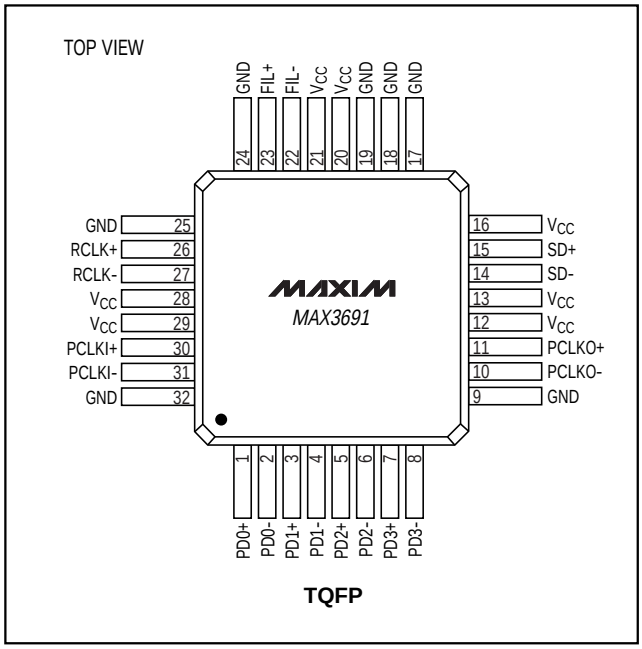


Figure 3. Alternative PECL-Output Termination

Pin Configuration

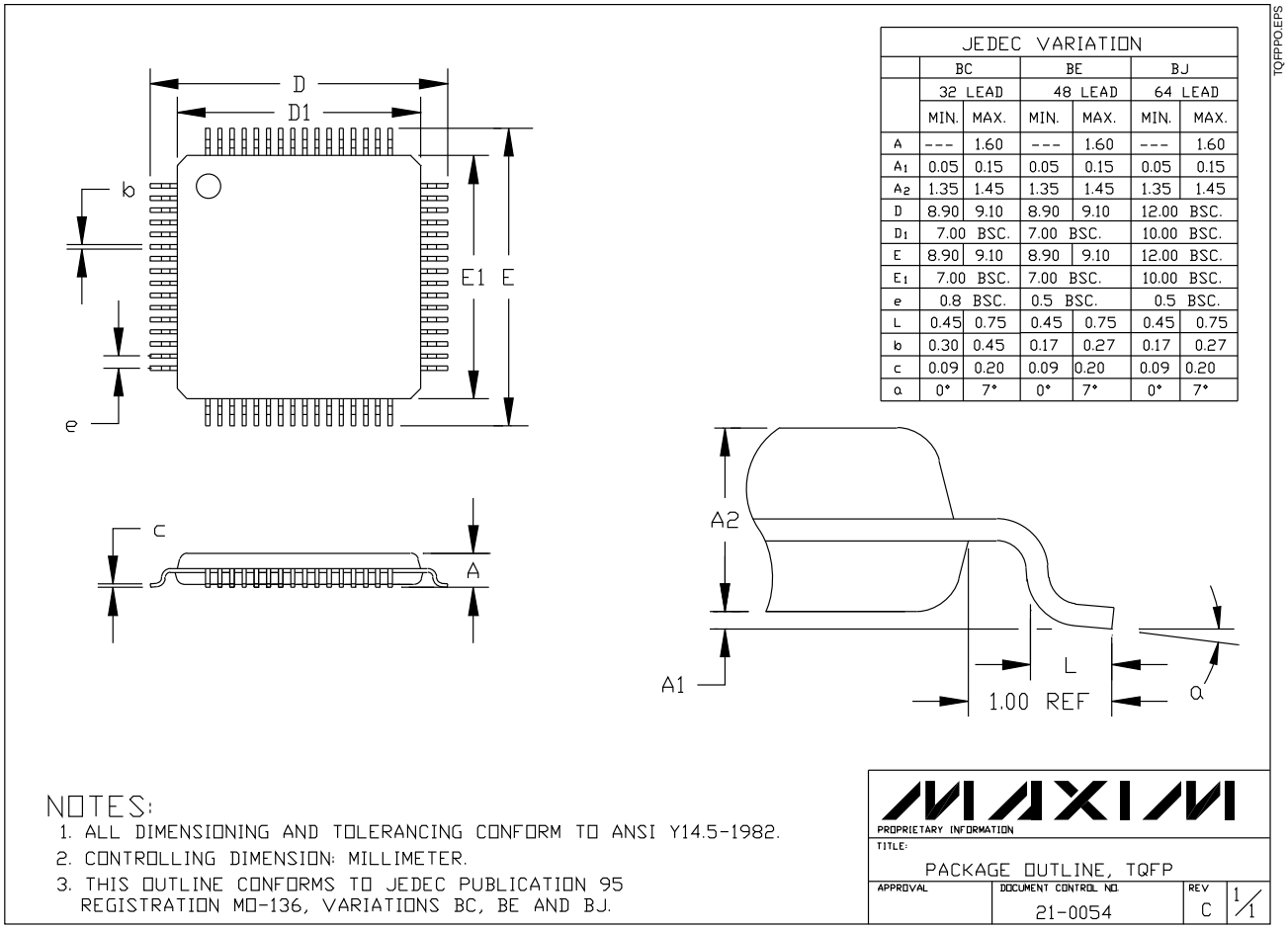


Chip Information

TRANSISTOR COUNT: 1633

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

Package Information



JEDEC VARIATION	BC		BE		BJ	
	32 LEAD		48 LEAD		64 LEAD	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10	12.00 BSC.	
D_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
E	8.90	9.10	8.90	9.10	12.00 BSC.	
E_1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
e	0.8 BSC.		0.5 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°	0°	7°

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC, BE AND BJ.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TQFP
APPROVAL | DOCUMENT CONTROL NO. 21-0054 | REV C | 1/1