



High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

General Description

The MAX4230–MAX4234 single/dual/quad, high-output-drive CMOS op amps feature 200mA of peak output current, rail-to-rail input, and output capability from a single 2.7V to 5.5V supply. These amplifiers exhibit a high slew rate of 10V/ μ s and a gain-bandwidth product (GBWP) of 10MHz. The MAX4230–MAX4234 can drive typical headset levels (32 Ω), as well as bias an RF power amplifier (PA) in wireless handset applications.

The MAX4230 comes in a tiny 5-pin SC70 package and the MAX4231, single with shutdown, is offered in the 6-pin SC70 package. The dual op-amp MAX4233 is offered in the space-saving 10-bump UCSP™, providing the smallest footprint area for a dual op amp with shutdown.

These op amps are designed to be part of the PA control circuitry, biasing RF PAs in wireless headsets. The MAX4231/MAX4233 offer a $\overline{\text{SHDN}}$ feature that drives the output low. This ensures that the RF PA is fully disabled when needed, preventing unconverted signals to the RF antenna.

The MAX4230 family offers low offsets, wide bandwidth, and high-output drive in a tiny 2.1mm x 2.0mm space-saving SC70 package. These parts are offered over the automotive temperature range (-40°C to +125°C).

Applications

RF PA Biasing Controls in Handset Applications
 Portable/Battery-Powered Audio Applications
 Portable Headphone Speaker Drivers (32 Ω)
 Audio Hands-Free Car Phones (Kits)
 Laptop/Notebook Computers/TFT Panels
 Sound Ports/Cards
 Set-Top Boxes
 Digital-to-Analog Converter Buffers
 Transformer/Line Drivers
 Motor Drivers

Selector Guide appears at end of data sheet.

Pin Configurations appear at end of data sheet.

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Features

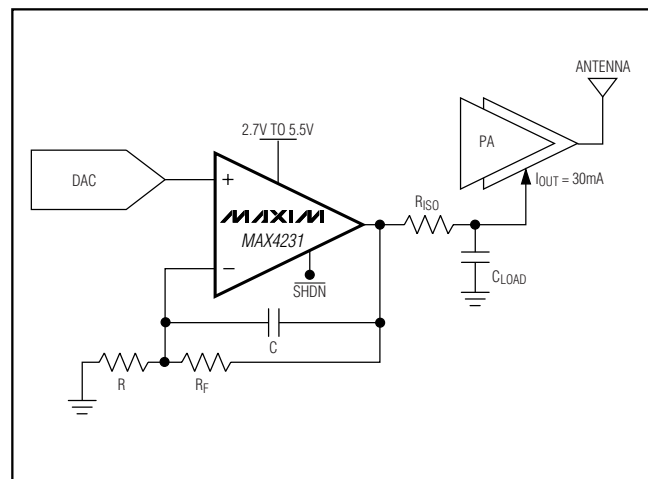
- ◆ 30mA Output Drive Capability
- ◆ Rail-to-Rail Input and Output
- ◆ 1.1mA Supply Current per Amplifier
- ◆ 2.7V to 5.5V Single-Supply Operation
- ◆ 10MHz Gain-Bandwidth Product
- ◆ High Slew Rate: 10V/ μ s
- ◆ 100dB Voltage Gain ($R_L = 100k\Omega$)
- ◆ 85dB Power-Supply Rejection Ratio
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ Unity-Gain Stable for Capacitive Loads to 780pF
- ◆ Low-Power Shutdown Mode Reduces Supply Current to <1 μ A
- ◆ Available in 5-Pin SC70 Package (MAX4230)
- ◆ Available in 10-Bump UCSP Package (MAX4233)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4230AXK-T	-40°C to +125°C	5 SC70-5	ACS
MAX4230AUK-T	-40°C to +125°C	5 SOT23-5	ABZZ
MAX4231AXT-T	-40°C to +125°C	6 SC70-6	ABA
MAX4231AUT-T	-40°C to +125°C	6 SOT23-6	AAUV

Ordering Information continued at end of data sheet.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS})	6V	8-Pin μ MAX (derate 4.5mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	362mW
All Other Pins	$(V_{SS} - 0.3V) + (V_{DD} + 0.3V)$	10-Pin μ MAX (derate 5.6mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	444mW
Output Short-Circuit Duration to V_{DD} or V_{SS} (Note 1)	1s	10-Bump UCSP (derate 6.1mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	484mW
Continuous Power Dissipation ($T_A = +70^{\circ}$ C)		14-Pin TSSOP (derate 9.1mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	727mW
5-Pin SC70 (derate 3.1mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	247mW	14-Pin SO (derate 8.3mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	667mW
5-Pin SOT23 (derate 7.1mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	571mW	Operating Temperature Range	-40 $^{\circ}$ C to +125 $^{\circ}$ C
6-Pin SC70 (derate 3.1mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	245mW	Junction Temperature	+150 $^{\circ}$ C
6-Pin SOT23 (derate 8.7mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	696mW	Storage Temperature Range	-65 $^{\circ}$ C to +150 $^{\circ}$ C
8-Pin SOT23 (derate 8.9mW/ $^{\circ}$ C above +70 $^{\circ}$ C)	714mW	Lead Temperature (soldering, 10s)	+300 $^{\circ}$ C

Note 1: Package power dissipation should also be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{SHDN} = V_{DD}$, $T_A = +25^{\circ}$ C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS		
Operating Supply Voltage Range	V_{DD}	Inferred from PSRR test	2.7		5.5	V		
Input Offset Voltage	V_{OS}			0.85	± 6	mV		
Input Bias Current	I_B	$V_{CM} = V_{SS}$ to V_{DD}		50		pA		
Input Offset Current	I_{OS}	$V_{CM} = V_{SS}$ to V_{DD}		50		pA		
Input Resistance	R_{IN}			1000		M Ω		
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test	V_{SS}		V_{DD}	V		
Common-Mode Rejection Ratio	CMRR	$V_{SS} < V_{CM} < V_{DD}$	52	70		dB		
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 2.7V$ to 5.5V	73	85		dB		
Shutdown Output Impedance	R_{OUT}	$V_{SHDN} = 0V$ (Note 3)		10		Ω		
Output Voltage in Shutdown	$V_{OUT(SHDN)}$	$V_{SHDN} = 0V$, $R_L = 200\Omega$ (Note 3)		68	120	mV		
Large-Signal Voltage Gain	A_{VOL}	$V_{SS} + 0.20 < V_{OUT} < V_{DD} - 0.20V$	$R_L = 100k\Omega$		100	dB		
			$R_L = 2k\Omega$	85	98			
			$R_L = 200\Omega$	74	80			
Output Voltage Swing	V_{OUT}	$R_L = 32\Omega$	$V_{DD} - V_{OH}$		400	500	mV	
			$V_{OL} - V_{SS}$		360	500		
		$R_L = 200\Omega$	$V_{DD} - V_{OH}$		80	120		
			$V_{OL} - V_{SS}$		70	120		
		$R_L = 2k\Omega$	$V_{DD} - V_{OH}$		8	14		
			$V_{OL} - V_{SS}$		7	14		
Output Source/Sink Current		$V_{OUT} = 0.15V$ to $(V_{DD} - 0.15V)$	7	10		mA		
Output Voltage with Current Load		$I_L = 10mA$	$V_{DD} = 2.7V$	$V_{DD} - V_{OH}$		128	200	mV
				$V_{OL} - V_{SS}$		112	175	
		$I_L = 30mA$	$V_{DD} = 5V$	$V_{DD} - V_{OH}$		240	320	
				$V_{OL} - V_{SS}$		224	300	

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{\overline{SHDN}} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Supply Current (per Amplifier)	I_{DD}	$V_{DD} = 5.5V$, $V_{CM} = V_{DD}/2$		1.2	2.3	mA
		$V_{DD} = 2.7V$, $V_{CM} = V_{DD}/2$		1.1	2.0	
Shutdown Supply Current (per Amplifier) (Note 3)	$I_{DD}(\overline{SHDN})$	$V_{\overline{SHDN}} = 0V$, $R_L = \infty$	$V_{DD} = 5.5V$	0.5	1	μA
			$V_{DD} = 2.7V$	0.1	1	
\overline{SHDN} Logic Threshold		Shutdown mode (Note 3)		$V_{SS} + 0.3$		V
		Normal mode (Note 3)		$V_{DD} - 0.3$		
\overline{SHDN} Input Bias Current		$V_{SS} < V_{\overline{SHDN}} < V_{DD}$ (Note 3)		50		pA

DC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{\overline{SHDN}} = V_{DD}$, $T_A = -40$ to $+125^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Supply Voltage Range	V_{DD}	Inferred from PSRR test	2.7		5.5	V	
Input Offset Voltage	V_{OS}				± 8	mV	
Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$			± 3		$\mu V/^\circ C$	
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test	V_{SS}		V_{DD}	V	
Common-Mode Rejection Ratio	CMRR	$V_{SS} < V_{CM} < V_{DD}$	46			dB	
Power-Supply Rejection Ratio	PSRR	$V_{DD} = 2.7V$ to $5.5V$	70			dB	
Output Voltage in Shutdown	$V_{OUT}(\overline{SHDN})$	$V_{\overline{SHDN}} < 0V$, $R_L = 200\Omega$ (Note 3)			150	mV	
Large-Signal Voltage Gain	A_{VOL}	$V_{SS} + 0.2V < V_{DD} - 0.2V$	$R_L = 2k\Omega$	76		dB	
			$R_L = 200\Omega$	67			
Output Voltage Swing	V_{OUT}	$R_L = 32\Omega$, $T_A = +85^\circ C$	$V_{DD} - V_{OH}$		650	mV	
			$V_{OL} - V_{SS}$		650		
		$R_L = 200\Omega$	$V_{DD} - V_{OH}$		150		
			$V_{OL} - V_{SS}$		150		
		$R_L = 2k\Omega$	$V_{DD} - V_{OH}$		20		
			$V_{OL} - V_{SS}$		20		
Output Source/Sink Current		$V_{OUT} = 0.15V$ to $(V_{DD} - 0.15V)$	4			mA	
Output Voltage with Current Load		$I_L = 10mA$	$V_{DD} = 2.7V$	$V_{DD} - V_{OH}$		250	mV
				$V_{OL} - V_{SS}$		230	
		$I_L = 30mA$, $T_A = -40^\circ C$ to $+85^\circ C$	$V_{DD} = 5V$	$V_{DD} - V_{OH}$		400	
				$V_{OL} - V_{SS}$		370	

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{SHDN} = V_{DD}$, $T_A = -40$ to $+125^\circ C$, unless otherwise noted.) (Note 2)

Quiescent Supply Current (per Amplifier)	I_{DD}	$V_{DD} = 5.5V$, $V_{CM} = V_{DD}/2$	2.8	mA	
		$V_{DD} = 2.7V$, $V_{CM} = V_{DD}/2$	2.5		
Shutdown Supply Current (per Amplifier) (Note 3)	$I_{DD}(SHDN)$	$V_{SHDN} < 0V$, $R_L = \infty$	$V_{DD} = 5.5V$	2.0	μA
			$V_{DD} = 2.7V$	2.0	

AC ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = (V_{DD}/2)$, $R_L = \infty$ connected to $(V_{DD}/2)$, $V_{SHDN} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP	$V_{CM} = V_{DD}/2$		10		MHz
Full-Power Bandwidth	FPBW	$V_{OUT} = 2V_{P-P}$, $V_{DD} = 5V$		0.8		MHz
Slew Rate	SR			10		V/ μ s
Phase Margin	PM			70		Degrees
Gain Margin	GM			15		dB
Total Harmonic Distortion Plus Noise	THD+N	$f = 10kHz$, $V_{OUT} = 2V_{P-P}$, $A_{VCL} = 1V/V$		0.0005		%
Input Capacitance	C_{IN}			8		pF
Voltage Noise Density	e_n	$f = 1kHz$		15		nV/ \sqrt{Hz}
		$f = 10kHz$		12		
Channel-to-Channel Isolation		$f = 1kHz$, $R_L = 100k\Omega$		125		dB
Capacitive-Load Stability		$A_{VCL} = 1V/V$, no sustained oscillations		780		pF
Shutdown Time	t_{SHDN}	(Note 3)		1		μ s
Enable Time from Shutdown	t_{ENABLE}	(Note 3)		1		μ s
Power-Up Time	t_{ON}			5		μ s

Note 2: All units 100% tested at $+25^\circ C$. All temperature limits are guaranteed by design.

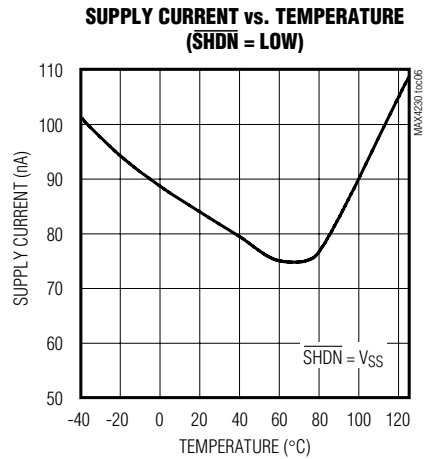
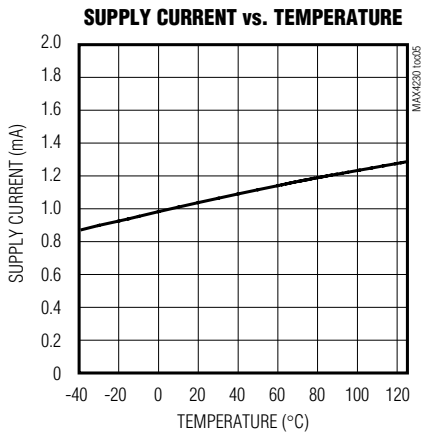
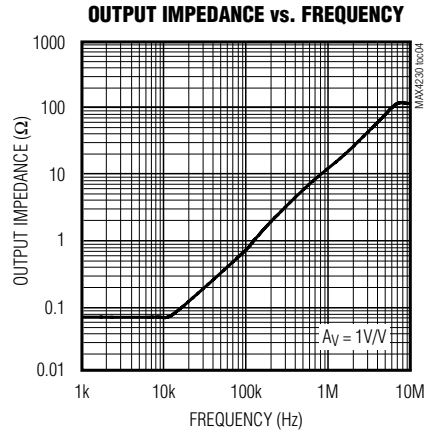
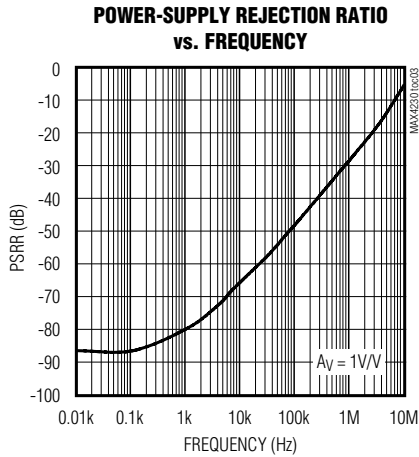
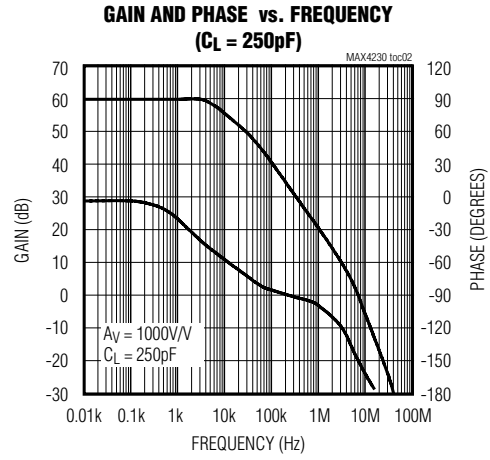
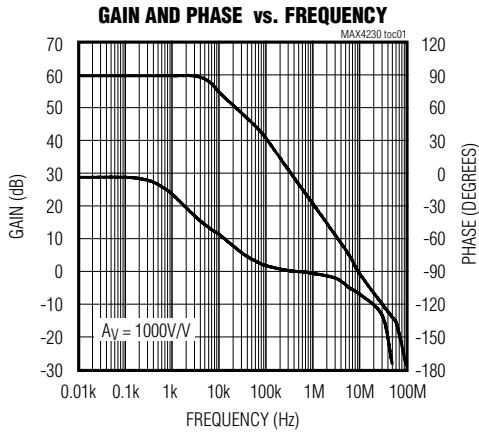
Note 3: SHDN logic parameters are for MAX4231/MAX4233 only.

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Typical Operating Characteristics

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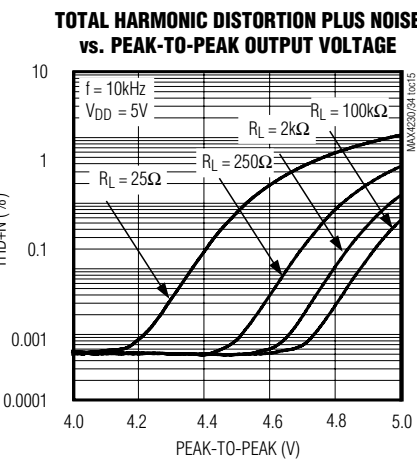
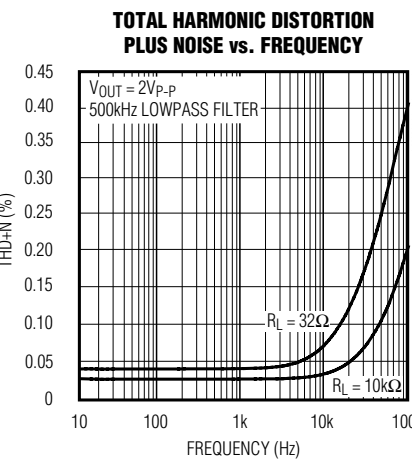
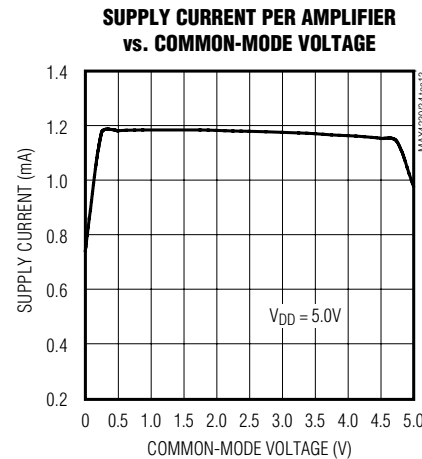
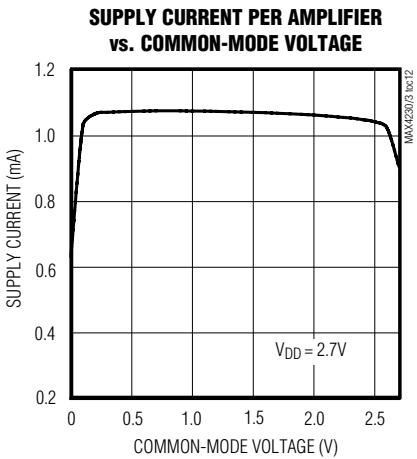
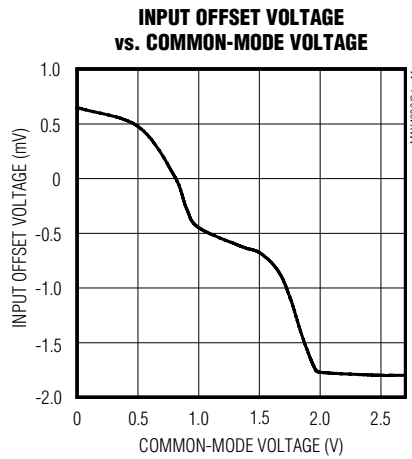
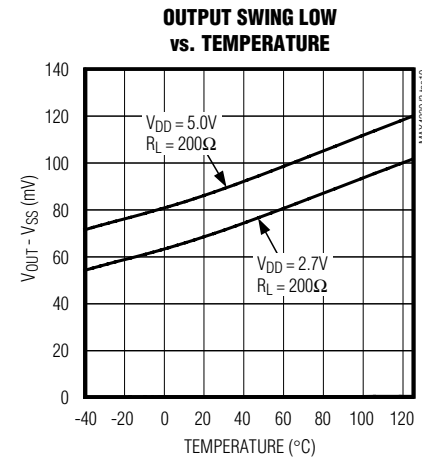
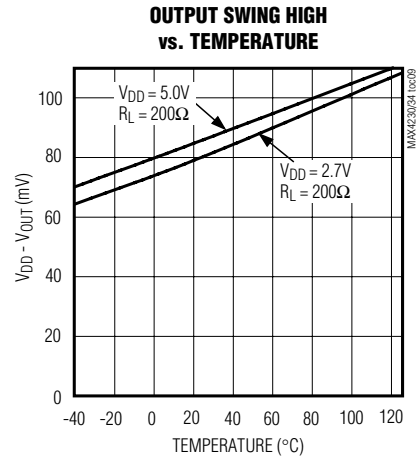
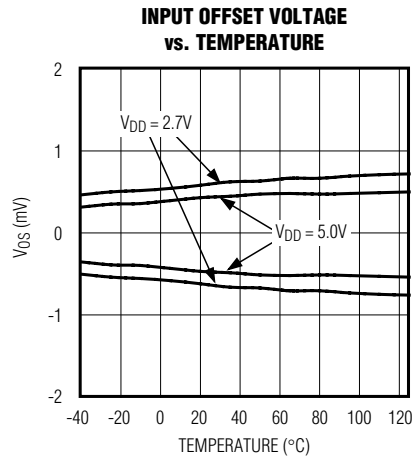
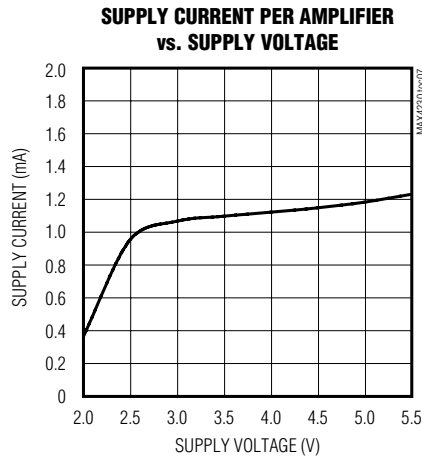
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High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Typical Operating Characteristics (continued)

($V_{DD} = 2.7V$, $V_{SS} = 0V$, $V_{CM} = V_{DD}/2$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$, connected to $V_{DD}/2$, $V_{SHDN} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.)



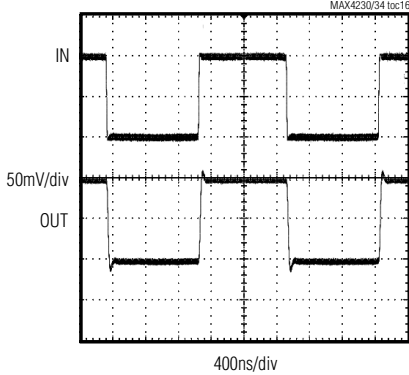
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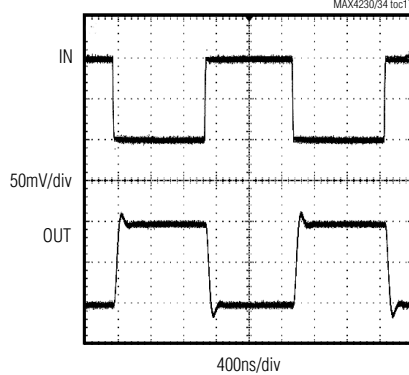
Typical Operating Characteristics (continued)

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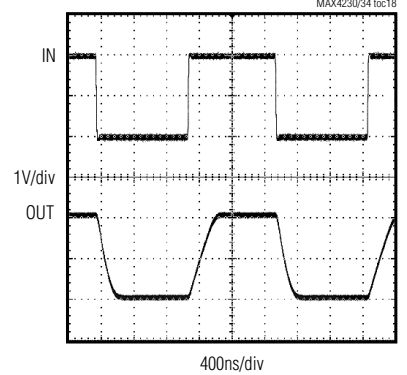
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



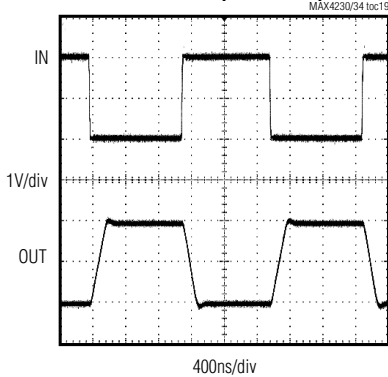
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



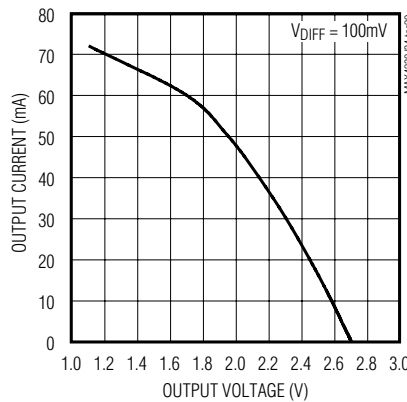
LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



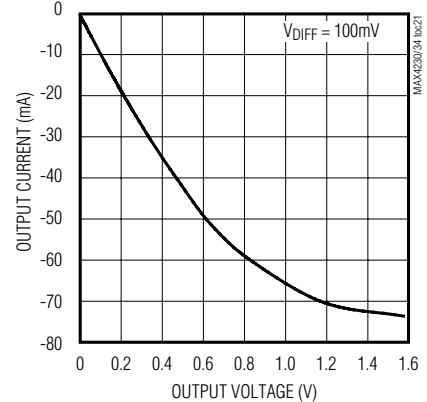
LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



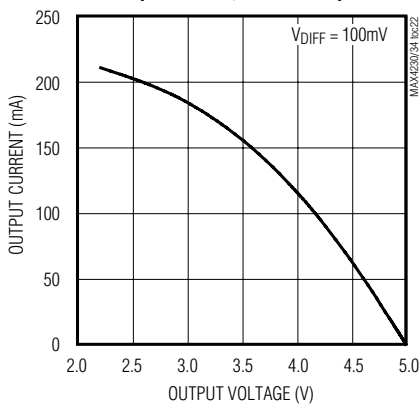
OUTPUT CURRENT vs. OUTPUT VOLTAGE (SOURCING, $V_{DD} = 2.7V$)



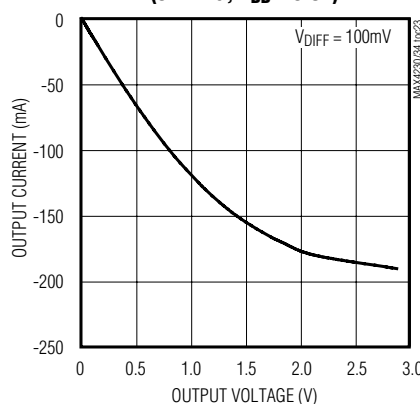
OUTPUT CURRENT vs. OUTPUT VOLTAGE (SINKING, $V_{DD} = 2.7V$)



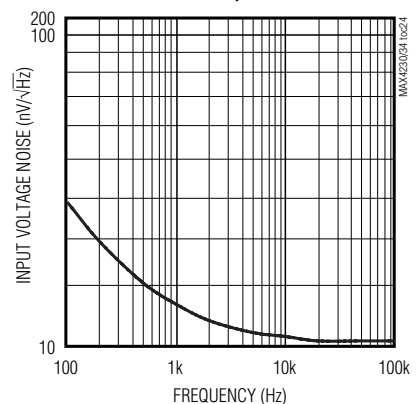
OUTPUT CURRENT vs. OUTPUT VOLTAGE (SOURCING, $V_{DD} = 5.0V$)



OUTPUT CURRENT vs. OUTPUT VOLTAGE (SINKING, $V_{DD} = 5.0V$)



INPUT VOLTAGE NOISE vs. FREQUENCY



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Pin Description

PIN						NAME	FUNCTION
MAX4230 SOT23/ SC70	MAX4231 SOT23/ SC70	MAX4232 SOT23/ μ MAX	MAX4233 μ MAX	MAX4233 UCSP	MAX4234 TSSOP/ SO		
1	1	—	—	—	—	IN+	Noninverting Input
2	2	4	4	B4	11	V _{SS}	Negative Supply Input. Connect to ground for single-supply operation.
3	3	—	—	—	—	IN-	Inverting Input
4	4	—	—	—	—	OUT	Amplifier Output
5	6	8	10	B1	4	V _{DD}	Positive Supply Input
—	5	—	5, 6	C4, A4	—	$\overline{\text{SHDN}}$, $\overline{\text{SHDN1}}$, $\overline{\text{SHDN2}}$	Shutdown Control. Tie to high for normal operation.
—	—	3	3	C3	3	IN1+	Noninverting Input to Amplifier 1
—	—	2	2	C2	2	IN1-	Inverting Input to Amplifier 1
—	—	1	1	C1	1	OUT1	Amplifier 1 Output
—	—	5	7	A3	5	IN2+	Noninverting Input to Amplifier 2
—	—	6	8	A2	6	IN2-	Inverting Input to Amplifier 2
—	—	7	9	A1	7	OUT2	Amplifier 2 Output
—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Input to Amplifiers 3 and 4
—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Input to Amplifiers 3 and 4
—	—	—	—	—	8, 14	OUT3, OUT4	Amplifiers 3 and 4 Outputs

Detailed Description

Rail-to-Rail Input Stage

The MAX4230-MAX4234 CMOS operational amplifiers have parallel-connected N- and P-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The N-channel stage is active for common-mode input voltages typically greater than (V_{SS} + 1.2V), and the P-channel stage is active for common-mode input voltages typically less than (V_{DD} - 1.2V).

Applications Information

Package Power Dissipation

Warning: Due to the high output current drive, this op amp can exceed the absolute maximum power-dissipation rating. As a general rule, as long as the peak current is less than or equal to 40mA, the maximum package

power dissipation is not exceeded for any of the package types offered. There are some exceptions to this rule, however. The absolute maximum power-dissipation rating of each package should always be verified using the following equations. The equation below gives an approximation of the package power dissipation:

$$P_{C(DISS)} \cong V_{RMS} I_{RMS} \cos \theta$$

where:

V_{RMS} = RMS voltage from V_{DD} to V_{OUT} when sourcing current and RMS voltage from V_{OUT} to V_{SS} when sinking current.

I_{RMS} = RMS current flowing out of or into the op amp and the load.

θ = phase difference between the voltage and the current. For resistive loads, $\cos \theta = 1$.

High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

MAX4230-MAX4234

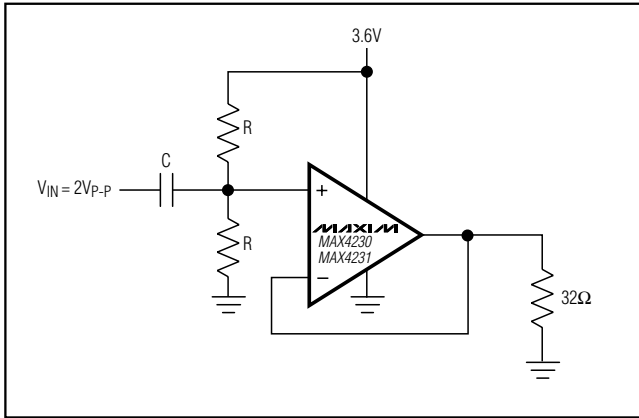


Figure 1. MAX4230/MAX4231 Used in Single-Supply Operation Circuit Example

For example, the circuit in Figure 1 has a package power dissipation of 196mW:

$$\begin{aligned} V_{RMS} &\cong (V_{DD} - V_{DC}) + \frac{V_{PEAK}}{\sqrt{2}} \\ &= 3.6V - 1.8V + \frac{1.0V}{\sqrt{2}} = 2.507V_{RMS} \\ I_{RMS} &\cong I_{DC} + \frac{I_{PEAK}}{\sqrt{2}} = \frac{1.8V}{32\Omega} + \frac{1.0V/32\Omega}{\sqrt{2}} \\ &= 78.4mA_{RMS} \end{aligned}$$

where:

V_{DC} = the DC component of the output voltage.

I_{DC} = the DC component of the output current.

V_{PEAK} = the highest positive excursion of the AC component of the output voltage.

I_{PEAK} = the highest positive excursion of the AC component of the output current.

Therefore:

$$\begin{aligned} P_{IC(DISS)} &= V_{RMS} I_{RMS} \cos \theta \\ &= 196mW \end{aligned}$$

Adding a coupling capacitor improves the package power dissipation because there is no DC current to the load, as shown in Figure 2:

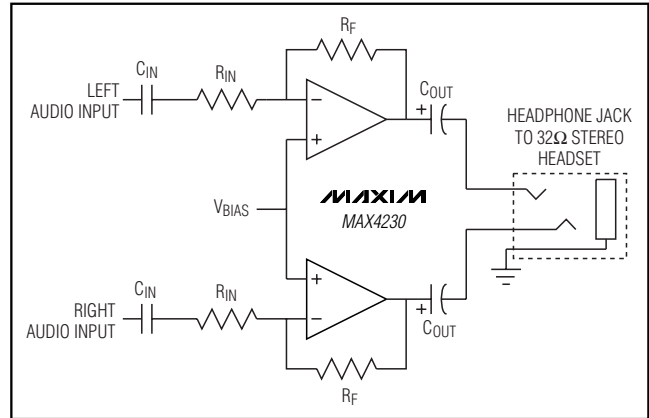


Figure 2. Circuit Example: Adding a Coupling Capacitor Greatly Reduces Power Dissipation of its Package

$$\begin{aligned} V_{RMS} &\cong \frac{V_{PEAK}}{\sqrt{2}} \\ &= \frac{1.0V}{\sqrt{2}} = 0.707V_{RMS} \\ I_{RMS} &\cong I_{DC} + \frac{I_{PEAK}}{\sqrt{2}} = 0A + \frac{1.0V/32\Omega}{\sqrt{2}} \\ &= 22.1mA_{RMS} \end{aligned}$$

Therefore:

$$\begin{aligned} P_{IC(DISS)} &= V_{RMS} I_{RMS} \cos \theta \\ &= 15.6mW \end{aligned}$$

If the configuration in Figure 1 were used with all four of the MAX4234 amplifiers, the absolute maximum power-dissipation rating of this package would be exceeded (see the *Absolute Maximum Ratings* section).

60mW Single-Supply Stereo Headphone Driver

Two MAX4230/MAX4231s can be used as a single-supply, stereo headphone driver. The circuit shown in Figure 2 can deliver 60mW per channel with 1% distortion from a single 5V supply.

The input capacitor (C_{IN}), in conjunction with R_{IN} , forms a highpass filter that removes the DC bias from the incoming signal. The -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

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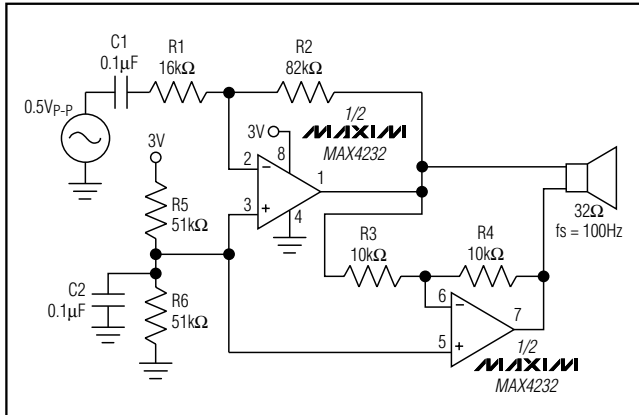


Figure 3. Dual MAX4230/MAX4231 Bridge Amplifier for 200mW at 3V

Choose gain-setting resistors R_{IN} and R_F according to the amount of desired gain, keeping in mind the maximum output amplitude. The output coupling capacitor, C_{OUT} , blocks the DC component of the amplifier output, preventing DC current flowing to the load. The output capacitor and the load impedance form a highpass filter with the -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

For a 32 Ω load, a 100 μ F aluminum electrolytic capacitor gives a low-frequency pole at 50Hz.

Bridge Amplifier

The circuit shown in Figure 3 uses a dual MAX4230 to implement a 3V, 200mW amplifier suitable for use in size-constrained applications. This configuration eliminates the need for the large coupling capacitor required by the single op-amp speaker driver when single-supply operation is necessary. Voltage gain is set to 10V/V; however, it can be changed by adjusting the 82k Ω resistor value.

Rail-to-Rail Input Stage

The MAX4230-MAX4234 CMOS op amps have parallel-connected N- and P-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The N-channel stage is active for common-mode input voltages typically greater than ($V_{SS} + 1.2V$), and the P-channel stage is active for common-mode input voltages typically less than ($V_{DD} - 1.2V$).

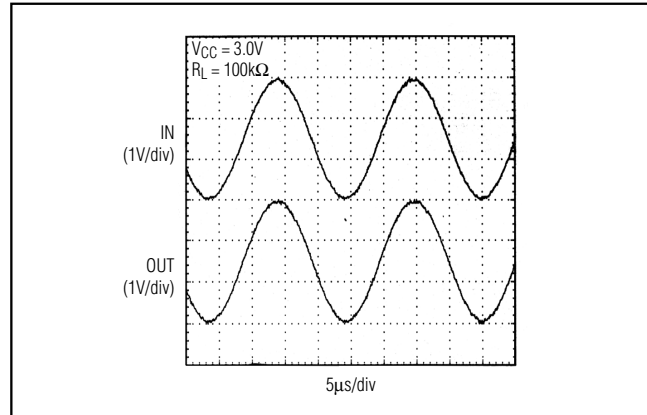


Figure 4. Rail-to-Rail Input/Output Range

Rail-to-Rail Output Stage

The minimum output is within millivolts of ground for single-supply operation, where the load is referenced to ground (V_{SS}). Figure 4 shows the input voltage range and the output voltage swing of a MAX4230 connected as a voltage follower. The maximum output voltage swing is load dependent; however, it is guaranteed to be within 500mV of the positive rail ($V_{DD} = 2.7V$) even with maximum load (32 Ω to ground).

The MAX4230-MAX4234 incorporate a smart short-circuit protection feature. When V_{OUT} is shorted to V_{DD} or V_{SS} , the device detects a fault condition and limits the output current, therefore protecting the device and the application circuit. If V_{OUT} is shorted to any voltage other than V_{DD} or V_{SS} , the smart short-circuit protection is not activated. When the smart short circuit is not active, the output currents can exceed 200mA (see *Typical Operating Characteristics*.)

Input Capacitance

One consequence of the parallel-connected differential input stages for rail-to-rail operation is a relatively large input capacitance C_{IN} (5pF typ). This introduces a pole at frequency $(2\pi R' C_{IN})^{-1}$, where R' is the parallel combination of the gain-setting resistors for the inverting or noninverting amplifier configuration (Figure 5). If the pole frequency is less than or comparable to the unity-gain bandwidth (10MHz), the phase margin is reduced, and the amplifier exhibits degraded AC performance through either ringing in the step response or sustained oscillations. The pole frequency is 10MHz when $R' = 2k\Omega$. To maximize stability, $R' \ll 2k\Omega$ is recommended.

High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

MAX4230-MAX4234

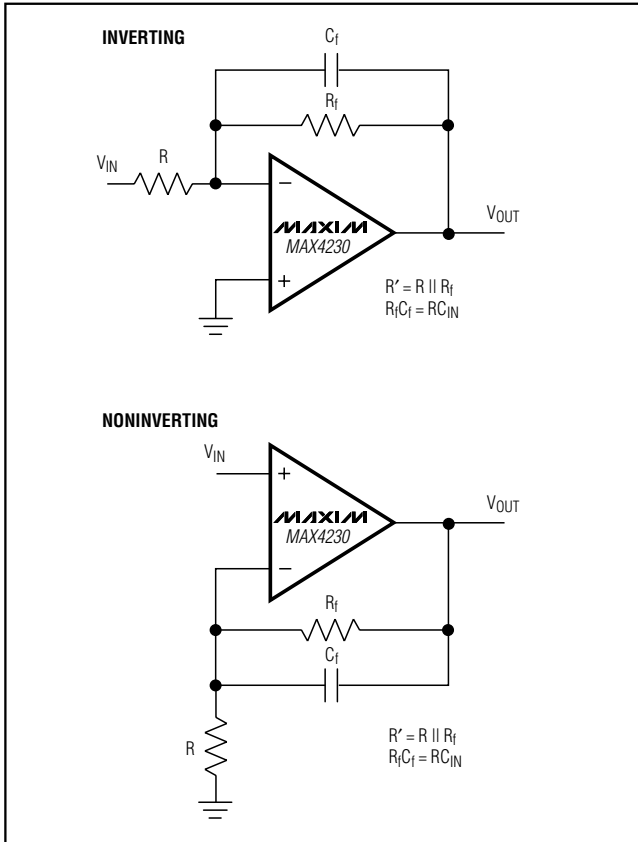


Figure 5. Inverting and Noninverting Amplifiers with Feedback Compensation

To improve step response when $R' > 2k\Omega$, connect small capacitor C_f between the inverting input and output. Choose C_f as follows:

$$C_f = 8(R / R_f) \text{ [pf]}$$

where R_f is the feedback resistor and R is the gain-setting resistor (Figure 5).

Driving Capacitive Loads

The MAX4230-MAX4234 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 780pF. Figure 6 is a graph of the stable operating region for various capacitive loads vs. resistive loads. Figures 7 and 8 show the transient response with excessive capacitive loads (1500pF), with and without the addition of an isolation resistor in series with the output. Figure 9 shows a typical noninverting capacitive-load-driving circuit in the unity-gain configuration.

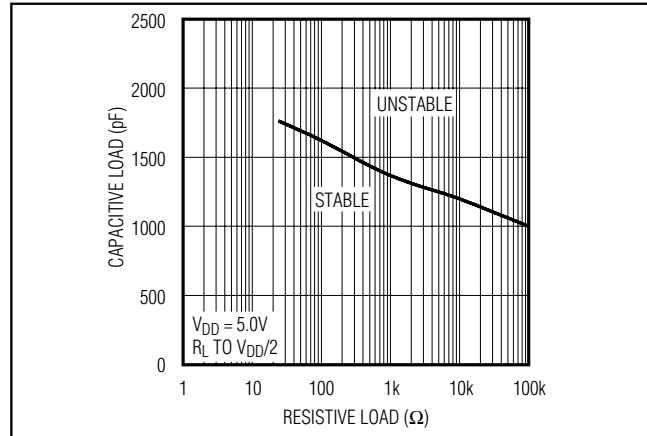


Figure 6. Capacitive-Load Stability

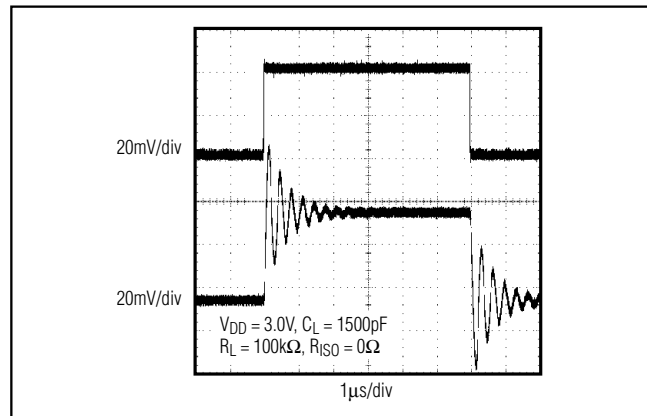


Figure 7. Small-Signal Transient Response with Excessive Capacitive Load

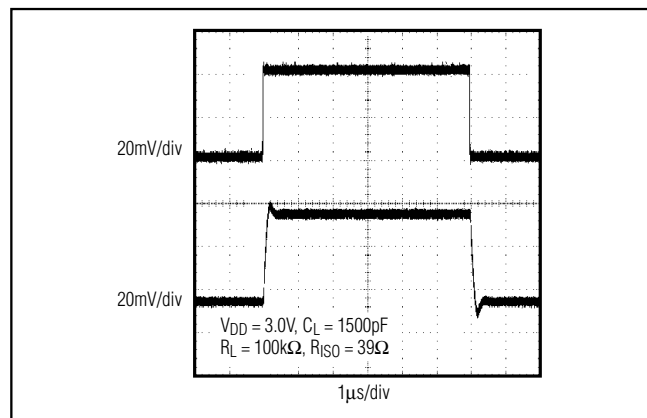


Figure 8. Small-Signal Transient Response with Excessive Capacitive Load with Isolation Resistor

High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

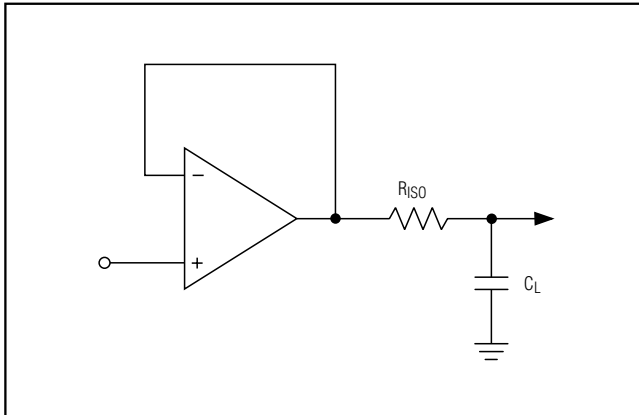


Figure 9. Capacitive-Load-Driving Circuit

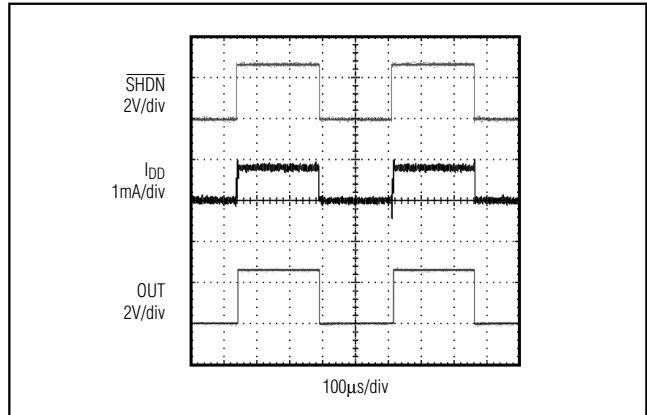


Figure 11. Shutdown Enable/Disable Supply Current

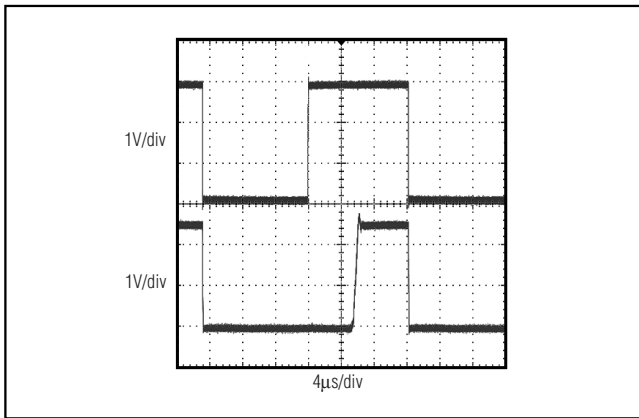


Figure 10. Shutdown Output Voltage Enable/Disable

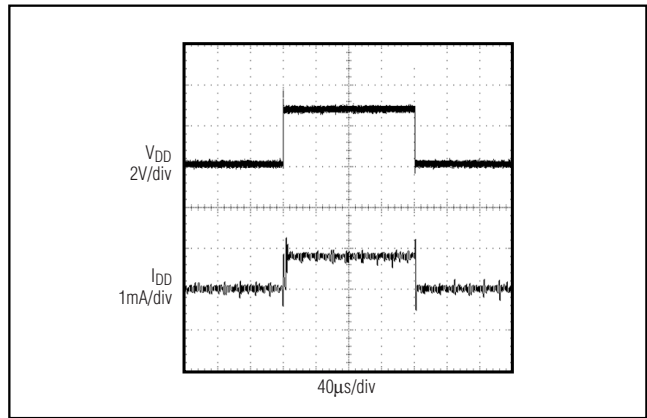


Figure 12. Power-Up/Down Supply Current

The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

Power-Up and Shutdown Modes

The MAX4231/MAX4233 have a shutdown option. When the shutdown pin ($\overline{\text{SHDN}}$) is pulled low, supply current drops to 0.5 μ A per amplifier ($V_{\text{DD}} = 2.7\text{V}$), the amplifiers are disabled, and their outputs are driven to V_{SS} . Since the outputs are actively driven to V_{SS} in shutdown, any pullup resistor on the output causes a current drain from the supply. Pulling $\overline{\text{SHDN}}$ high enables the amplifier. In the dual MAX4233, the two amplifiers shut down independently. Figure 10 shows the MAX4231's output voltage to a shutdown pulse. The MAX4231-MAX4234 typically settle within 5 μ s after power-up. Figures 11 and 12 show I_{DD} to a shutdown plus and voltage power-up cycle.

Selector Guide

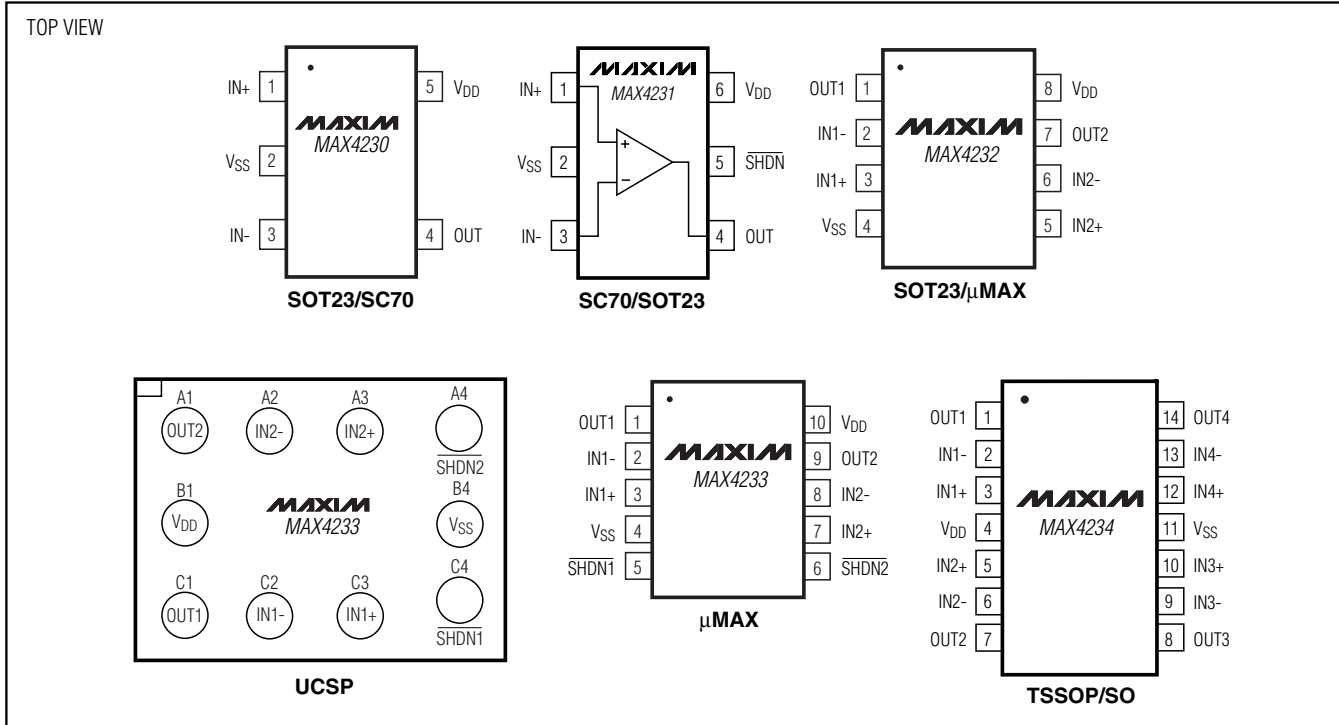
PART	AMPS PER PACKAGE	SHUTDOWN MODE
MAX4230	Single	—
MAX4231	Single	Yes
MAX4232	Dual	—
MAX4233	Dual	Yes
MAX4234	Quad	—

When exiting shutdown, there is a 6 μ s delay before the amplifier's output becomes active (Figure 10).

High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Pin Configurations

MAX4230-MAX4234



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4232AKA-T	-40°C to +125°C	8 SOT23-8	AAKW
MAX4232AUA	-40°C to +125°C	8 μ MAX	—
MAX4233AUB	-40°C to +125°C	10 μ MAX	—
MAX4233ABC-T	-40°C to +125°C	10 UCSP-10	ABE
MAX4234AUD	-40°C to +125°C	14 TSSOP	—
MAX4234ASD	-40°C to +125°C	14 SO	—

Chip Information

MAX4230 TRANSISTOR COUNT: 230
 MAX4231 TRANSISTOR COUNT: 230
 MAX4232 TRANSISTOR COUNT: 462
 MAX4233 TRANSISTOR COUNT: 462
 MAX4234 TRANSISTOR COUNT: 924

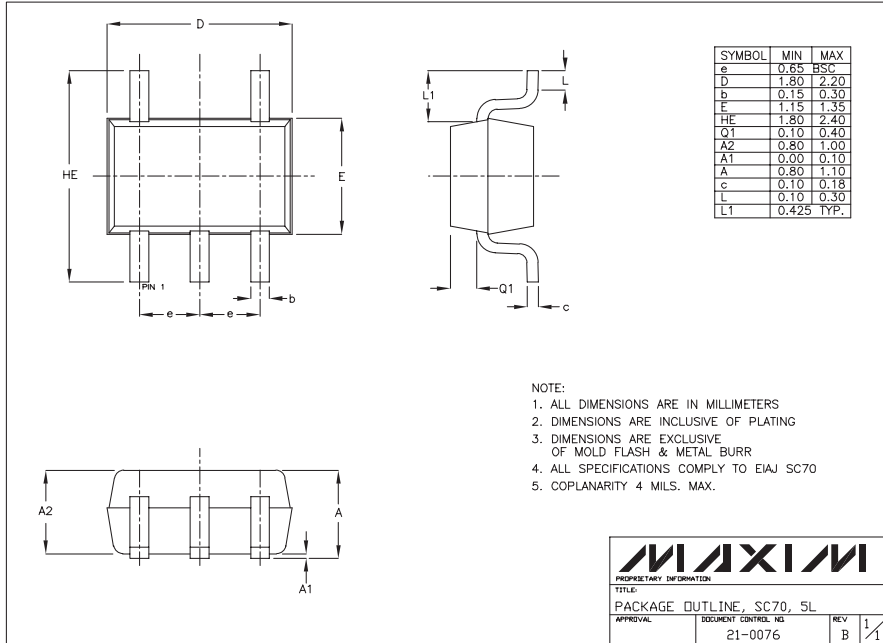
Power Supplies and Layout

The MAX4230-MAX4234 can operate from a single 2.7V to 5.5V supply, or from dual ± 1.35 V to ± 2.5 V supplies. For single-supply operation, bypass the power supply with a 0.1 μ F ceramic capacitor. For dual-supply operation, bypass each supply to ground. Good layout improves performance by decreasing the amount of stray capacitance at the op amps' inputs and outputs. Decrease stray capacitance by placing external components close to the op amps' pins, minimizing trace and lead lengths.

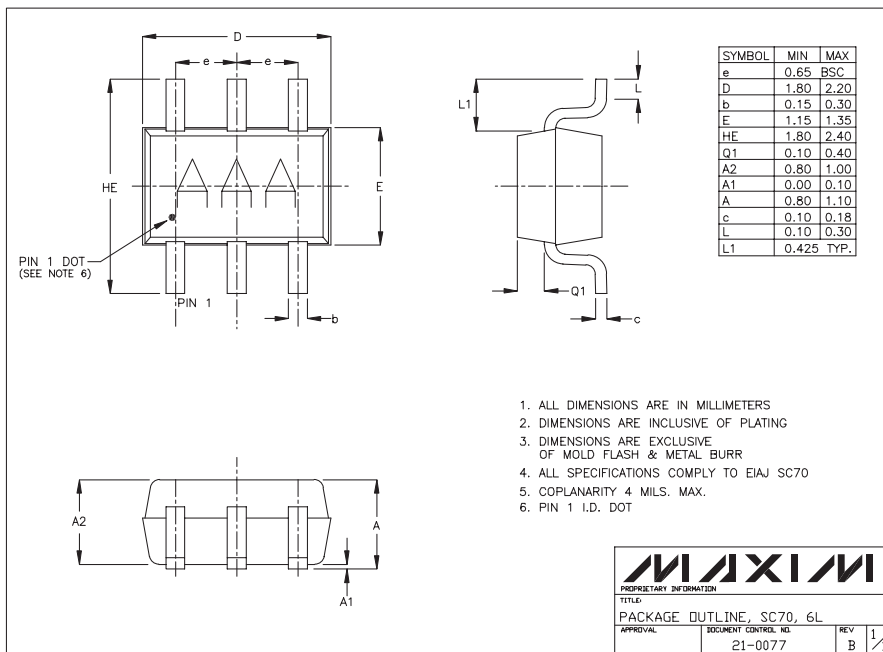
High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



SC70, 5L EPS



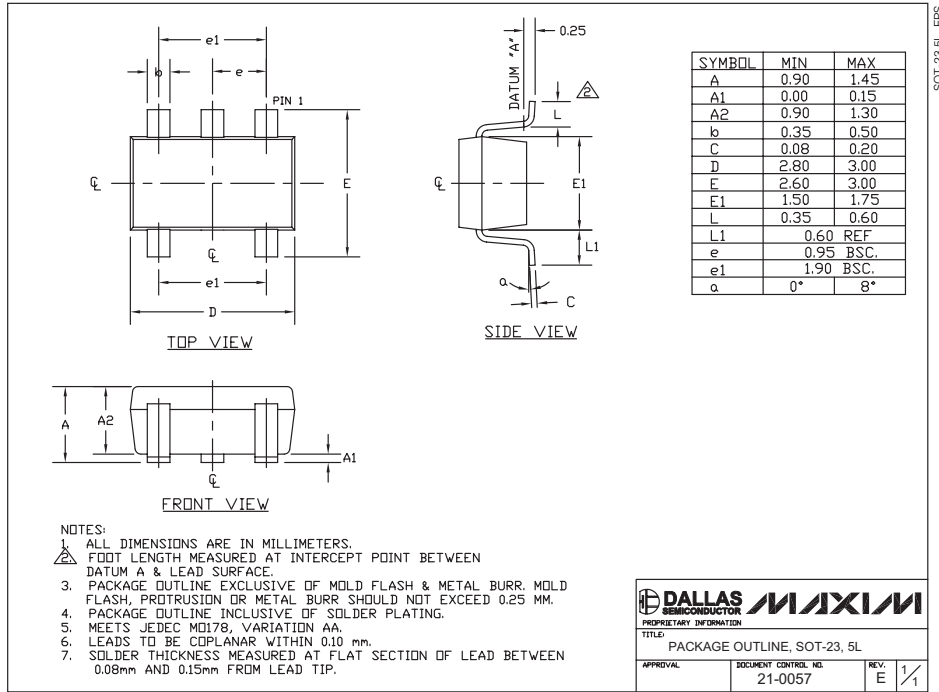
SC70, 6L EPS

High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

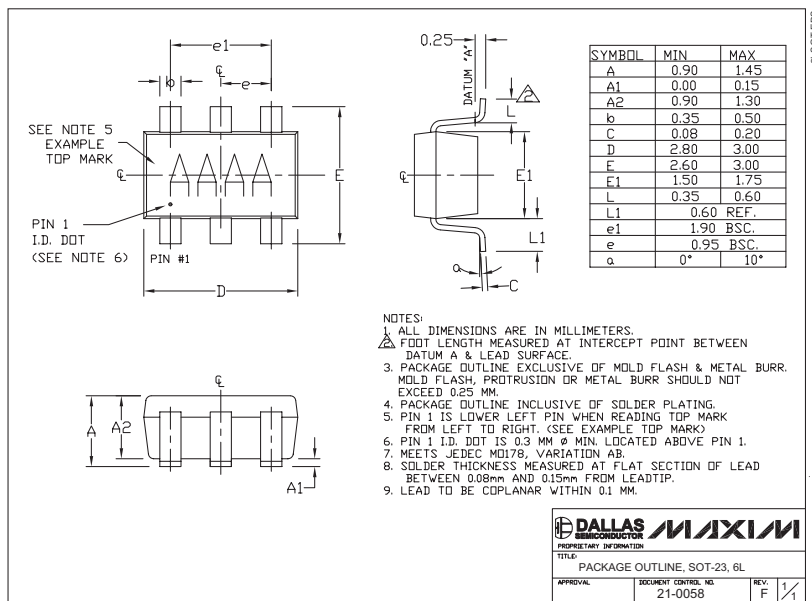
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX4230-MAX4234



SOT-23 5L EPS

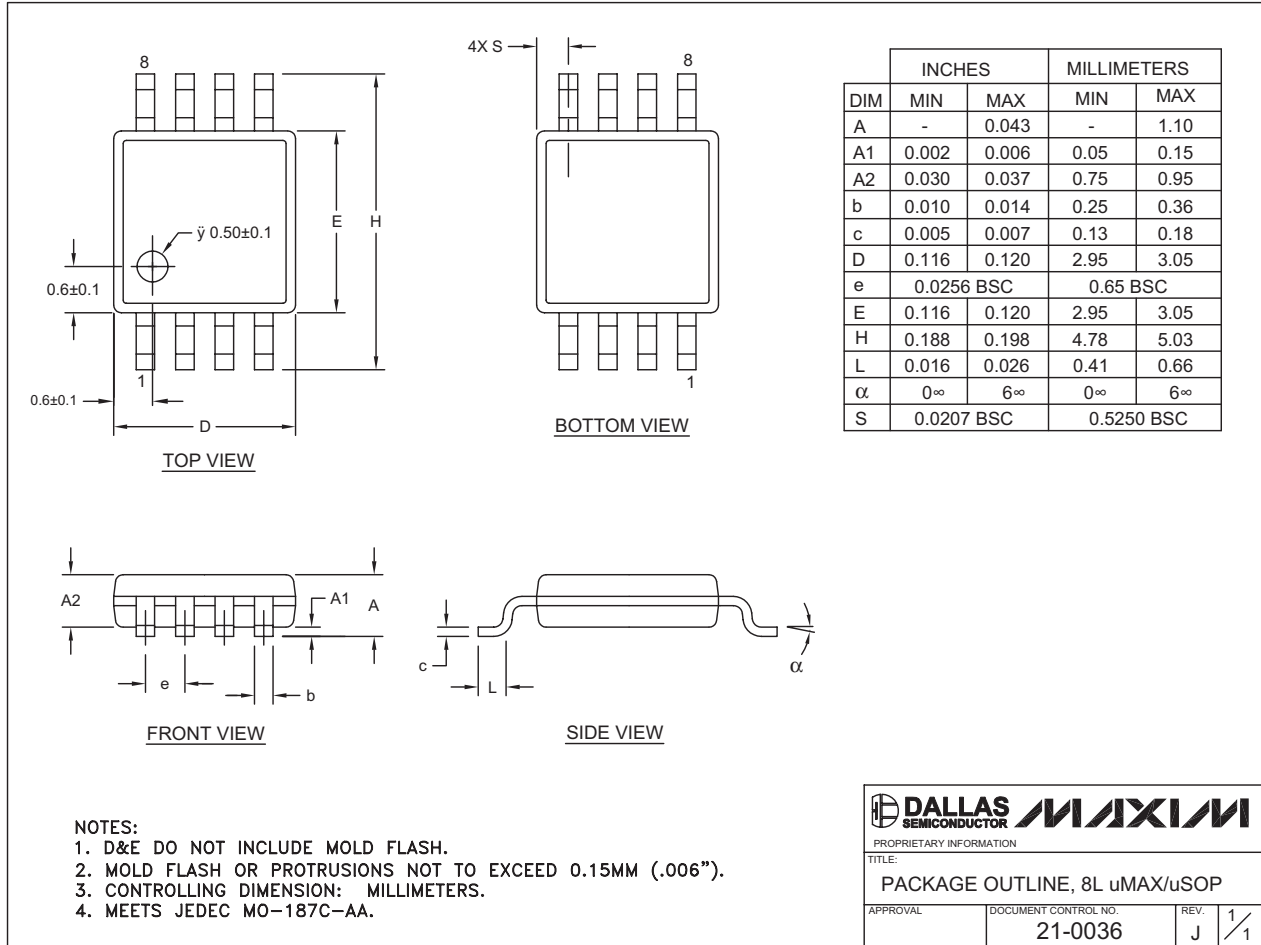


SOT-23 6L EPS

High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



8LUMAXD.EPS

High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX4230-MAX4234

SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.60
L2	0.25 BSC.	
e	0.65 BSC.	
e1	1.95 REF.	
θ	0 $^{\circ}$	8 $^{\circ}$

NOTE:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- Δ FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
- PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
- PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
- COPLANARITY 4 MILS. MAX.
- PIN 1 I.D. DOT IS 0.3 MM $\dot{\gamma}$ MIN. LOCATED ABOVE PIN 1.
- SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
- MEETS JEDEC MO178.

DETAIL "A"

SEATING PLANE [C] GAUGE PLANE

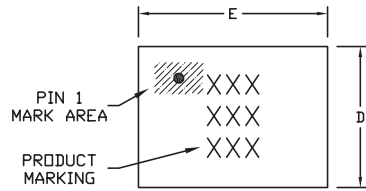
SOT23-8L EPS

<small>PROPRIETARY INFORMATION</small>		
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY		
<small>APPROVAL</small> _____	<small>DOCUMENT CONTROL NO.</small> 21-0078	<small>REV.</small> D 1/1

High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

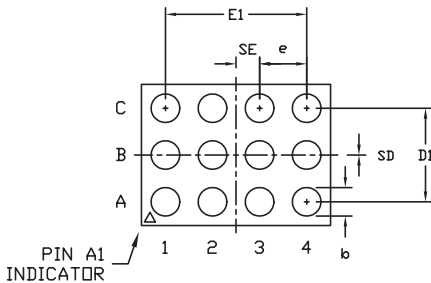


TOP VIEW

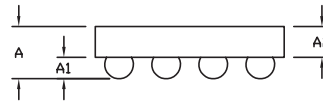
COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3

- NOTES:
 1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

PROPRIETARY INFORMATION		
TITLE: PACKAGE OUTLINE, 4x3 UCSP		
APPROVAL	DOCUMENT CONTROL NO. 21-0104	REV. F 1/1

12L UCSP 4x3 EFS

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