

MAXIM**Ultra-Small, +1.8V, μ Power,
Rail-to-Rail I/O Op Amps****General Description**

The MAX4291/MAX4292/MAX4294 family of micropower operational amplifiers operates from a +1.8V to +5.5V single supply or $\pm 0.9V$ to $\pm 2.75V$ dual supplies and has Rail-to-Rail[®] input/output capabilities. These amplifiers provide a 500kHz gain-bandwidth product and 120dB open-loop voltage gain while using only 100 μ A of supply current per amplifier. The combination of low input offset voltage ($\pm 400\mu V$) and high-open-loop gain makes them suitable for low-power/low-voltage high-precision applications.

The MAX4291/MAX4292/MAX4294 have an input common-mode range that extends to each supply rail, and their outputs typically swing within 20mV of the rails with a 2k Ω load. Although the minimum operating voltage is specified at +1.8V, these devices typically operate down to +1.5V. The combination of ultra-low-voltage operation, rail-to-rail inputs/output, and low-power consumption makes these devices ideal for any portable/two-cell battery-powered system.

The single MAX4291 is offered in an ultra-small 5-pin SC70 package and the dual MAX4292 is offered in a space-saving 8-pin μ MAX package.

Applications

2-Cell Battery-Operated Systems
 Portable Electronic Equipment
 Battery-Powered Instrumentation
 Digital Scales
 Strain Gauges
 Sensor Amplifiers
 Cellular Phones

Selector Guide

PART	AMPLIFIERS PER PACKAGE	PIN-PACKAGE
MAX4291	1	5-pin SC70/SOT23
MAX4292	2	8-pin μ MAX/SO
MAX4294	4	14-pin SO/TSSOP

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

MAXIM

Maxim Integrated Products 1

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 For small orders, phone 1-800-835-8769.**

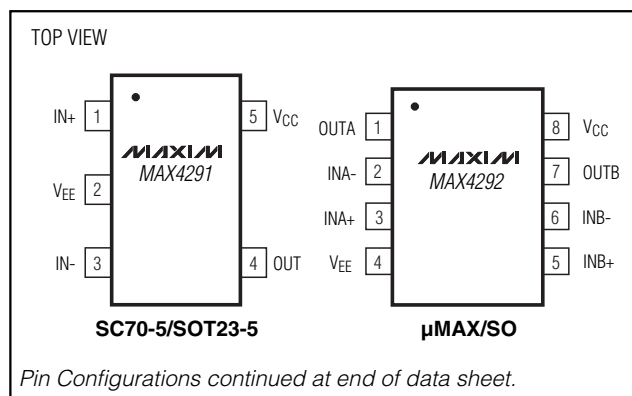
Features

- ◆ Ultra-Low Voltage Operation—Guaranteed Down to +1.8V
- ◆ 100 μ A Supply Current per Amplifier
- ◆ 500kHz Gain-Bandwidth Product
- ◆ 120dB Open-Loop Voltage Gain ($R_L = 100k\Omega$)
- ◆ 0.017% THD + Noise at 1kHz
- ◆ Rail-to-Rail Input Common-Mode Range
- ◆ Rail-to-Rail Output Drives 2k Ω Load
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ Unity-Gain Stable for Capacitive Loads up to 100pF
- ◆ 400 μ V Input Offset Voltage
- ◆ Single Available in Ultra-Small 5-Pin SC70
Dual Available in Space-Saving 8-Pin μ MAX

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX4291EXK-T	-40°C to +85°C	5 SC70-5	AAD
MAX4291EUK-T	-40°C to +85°C	5 SOT23-5	ADML
MAX4292EUA*	-40°C to +85°C	8 μ MAX	—
MAX4292ESA*	-40°C to +85°C	8 SO	—
MAX4294ESD*	-40°C to +85°C	14 SO	—
MAX4294EUD*	-40°C to +85°C	14 TSSOP	—

*Future product—contact factory for availability.

Pin Configurations

MAX4291/MAX4292/MAX4294

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}).....+6V	8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
All Other Pins($V_{CC} + 0.3V$) to ($V_{EE} - 0.3V$)	14-Pin SO (derate 8.33mW/°C above +70°C)667mW
Output Short-Circuit Duration.....Continuous	14-Pin TSSOP (derate 6.3mW/°C above +70°C)500mW
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	Operating Temperature Range.....-40°C to +85°C
5-Pin SC70 (derate 2.5mW/°C above +70°C)200mW	Junction Temperature+150°C
5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW	Storage Temperature Range-65°C to +150°C
8-Pin μ MAX (derate 4.10mW/°C above +70°C).....330mW	Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +1.8V$ to +5.5V, $V_{EE} = V_{CM} = 0$, $V_{OUT} = V_{CC} / 2$, $R_L = 100k\Omega$ connected to $V_{CC} / 2$, $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from PSRR test	1.8		5.5	V
Quiescent Supply Current (per Amplifier)	I_Q	$V_{CC} = 1.8V$		100	210	μA
		$V_{CC} = 5.0V$		110	225	
Input Offset Voltage	V_{OS}	MAX4291EXK, MAX4291EUK		± 400	± 2500	μV
		MAX4292EUA, MAX4294EUD		± 400	± 1500	
		MAX4292ESA, MAX4294ESD		± 400	± 1500	
Input Bias Current	I_B	$V_{CC} = 5.0V$, $0 \leq V_{CM} \leq 5.0V$		± 15	± 55	nA
Input Offset Current	I_{OS}	$V_{CC} = 5.0V$, $0 \leq V_{CM} \leq 5.0V$		± 1	± 7	nA
Differential Input Resistance	R_{IN}	$ V_{IN+} - V_{IN-} < 10mV$		0.75		$M\Omega$
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test	0		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	Tested for $0 \leq V_{CM} \leq 1.8V$, $V_{CC} = 1.8V$	MAX4291EXK, MAX4291EUK	50	80	dB
			MAX4292EUA, MAX4294EUD	65	85	
			MAX4292ESA, MAX4294ESD	65	85	
		Tested for $0 \leq V_{CM} \leq 5.0V$, $V_{CC} = 5.0V$	MAX4291EXK, MAX4291EUK	60	90	dB
			MAX4292EUA, MAX4294EUD	70	90	
			MAX4292ESA, MAX4294ESD	70	90	
Power-Supply Rejection Ratio	PSRR	MAX4291EXK, MAX4291EUK	80	100	dB	
		MAX4292EUA, MAX4294EUD	80	100		
		MAX4292ESA, MAX4294ESD	80	100		

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

MAX4291/MAX4292/MAX4294

ELECTRICAL CHARACTERISTICS

($V_{CC} = +1.8V$ to $+5.5V$, $V_{EE} = V_{CM} = 0$, $V_{OUT} = V_{CC} / 2$, $R_L = 100k\Omega$ connected to $V_{CC} / 2$, $T_A = +25^\circ C$, unless otherwise noted.)
(Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A_V	$V_{CC} = 1.8V$	$R_L = 100k\Omega$, $0.015V \leq V_{OUT} \leq V_{CC} - 0.015V$	80	120		dB
			$R_L = 2k\Omega$, $0.1V \leq V_{OUT} \leq V_{CC} - 0.1V$	80	110		
		$V_{CC} = 5.0V$	$R_L = 100k\Omega$, $0.015V \leq V_{OUT} \leq V_{CC} - 0.015V$	80	130		
			$R_L = 2k\Omega$, $0.1V \leq V_{OUT} \leq V_{CC} - 0.1V$	80	120		
Output Voltage Swing High	V_{OH}	Specified as $ V_{CC} - V_{OH} $	$R_L = 100k\Omega$ to $V_{CC} / 2$		2	20	mV
			$R_L = 2k\Omega$ to $V_{CC} / 2$		15	40	
Output Voltage Swing Low	V_{OL}	Specified as $ V_{EE} - V_{OL} $	$R_L = 100k\Omega$ to $V_{CC} / 2$		3	15	mV
			$R_L = 2k\Omega$ to $V_{CC} / 2$		18	40	
Output Short-Circuit Current	$I_{OUT(SC)}$	Sourcing or sinking			20		mA
Channel-to-Channel Isolation	CHISO	Specified at $f = 10kHz$ (MAX4292/MAX4294 only)			100		dB
Gain Bandwidth Product	GBW				500		kHz
Phase Margin	ϕ_M				65		degrees
Gain Margin	G_M				12		dB
Slew Rate	SR				0.2		V/ μs
Input Voltage Noise Density	e_n	$f = 10kHz$			70		nV/ \sqrt{Hz}
Input Current Noise Density	i_n	$f = 10kHz$			0.05		pA/ \sqrt{Hz}
Capacitive-Load Stability		$A_{VCL} = +1V/V$, no sustained oscillations			100		pF

ELECTRICAL CHARACTERISTICS

($V_{CC} = +1.8V$ to $+5.5V$, $V_{EE} = V_{CM} = 0$, $V_{OUT} = V_{CC} / 2$, $R_L = 100k\Omega$ connected to $V_{CC} / 2$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from PSRR test	1.8		5.5	V
Quiescent Supply Current (per Amplifier)	I_Q	$V_{CC} = 1.8V$			240	μA
		$V_{CC} = 5.0V$			270	
Input Offset Voltage	V_{OS}	MAX4291EXK, MAX4291EUK			± 3000	μV
		MAX4292EUA, MAX4294EUD			± 1500	
		MAX4292ESA, MAX4294ESD			± 1500	

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

ELECTRICAL CHARACTERISTICS

($V_{CC} = +1.8V$ to $+5.5V$, $V_{EE} = V_{CM} = 0$, $V_{OUT} = V_{CC} / 2$, $R_L = 100k\Omega$ connected to $V_{CC} / 2$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage Drift	TCV _{OS}				1.2		$\mu V/^\circ C$
Input Bias Current	I _B	$V_{CC} = 5.0V$, $0 \leq V_{CM} \leq 5.0V$				± 80	nA
Input Offset Current	I _{OS}	$V_{CC} = 5.0V$, $0 \leq V_{CM} \leq 5.0V$				± 10	nA
Input Common-Mode Voltage Range	V _{CM}	Inferred from CMRR test		0		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	Tested for $0 \leq V_{CM} \leq 1.8V$, $V_{CC} = 1.8V$	MAX4291EXK, MAX4291EUK	50			dB
			MAX4292EUA, MAX4294EUD	60			
			MAX4292ESA, MAX4294ESD	60			
		Tested for $0 \leq V_{CM} \leq 5.0V$, $V_{CC} = 5.0V$	MAX4291EXK, MAX4291EUK	60			dB
			MAX4292EUA, MAX4294EUD	65			
			MAX4292ESA, MAX4294ESD	65			
Power-Supply Rejection Ratio	PSRR	MAX4291EXK, MAX4291EUK		78			dB
		MAX4292EUA, MAX4294EUD		80			
		MAX4292ESA, MAX4294ESD		80			
Large-Signal Voltage Gain	A _v	$V_{CC} = 1.8V$	$R_L = 100k\Omega$, $0.015V \leq V_{OUT} \leq V_{CC} - 0.015V$	80			dB
			$R_L = 2k\Omega$, $0.1V \leq V_{OUT} \leq V_{CC} - 0.1V$	80			
		$V_{CC} = 5.0V$	$R_L = 100k\Omega$, $0.015V \leq V_{OUT} \leq V_{CC} - 0.015V$	80			
			$R_L = 2k\Omega$, $0.1V \leq V_{OUT} \leq V_{CC} - 0.1V$	80			
Output Voltage Swing High	V _{OH}	Specified as $ V_{CC} - V_{OH} $	$R_L = 100k\Omega$ to $V_{CC} / 2$			20	mV
			$R_L = 2k\Omega$ to $V_{CC} / 2$			40	
Output Voltage Swing Low	V _{OL}	Specified as $ V_{EE} - V_{OL} $	$R_L = 100k\Omega$ to $V_{CC} / 2$			15	mV
			$R_L = 2k\Omega$ to $V_{CC} / 2$			40	

Note 1: All devices are 100% tested at $T_A = +25^\circ C$. All temperature limits are guaranteed by design.

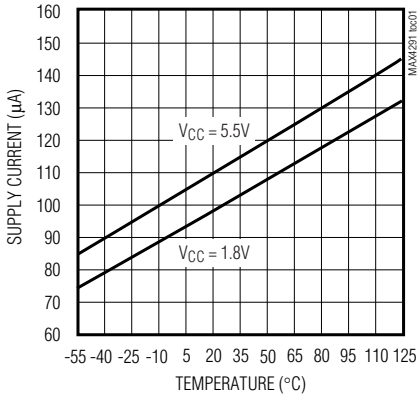
Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

Typical Operating Characteristics

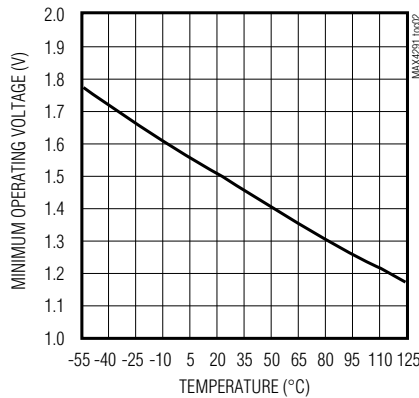
($V_{CC} = +2.4V$, $V_{EE} = V_{CM} = 0$, $V_{OUT} = V_{CC} / 2$, no load, $T_A = +25^\circ C$, unless otherwise noted.)

MAX4291/MAX4292/MAX4294

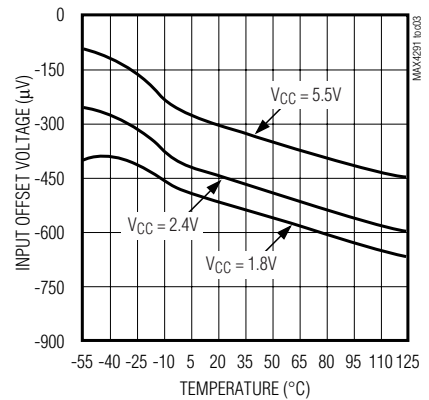
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



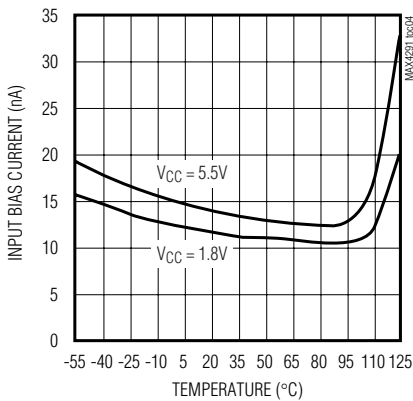
MINIMUM OPERATING VOLTAGE vs. TEMPERATURE (PSRR $\geq 80dB$)



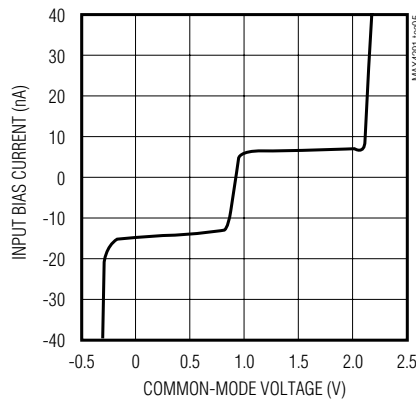
INPUT OFFSET VOLTAGE vs. TEMPERATURE



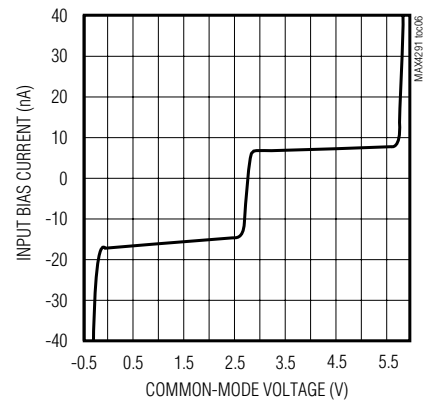
INPUT BIAS CURRENT vs. TEMPERATURE



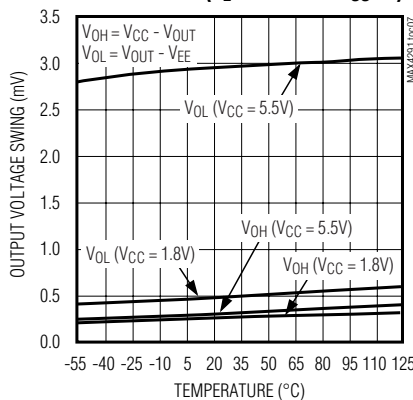
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE ($V_{CC} = 1.8V$)



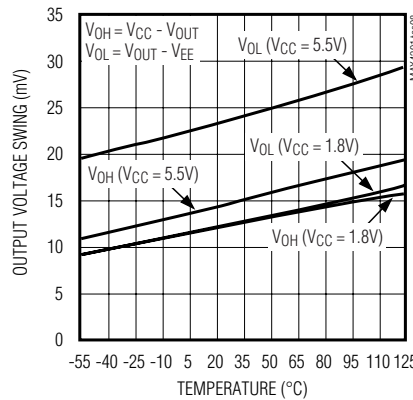
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE ($V_{CC} = 5.5V$)



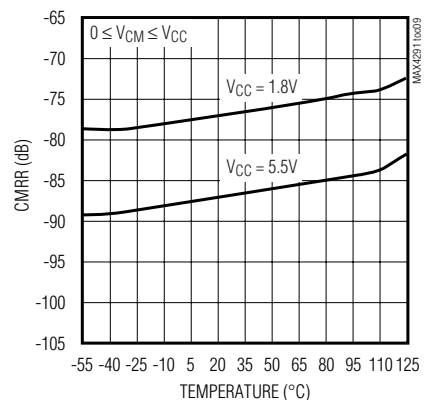
OUTPUT VOLTAGE SWING vs. TEMPERATURE ($R_L = 100k\Omega$ to $V_{CC} / 2$)



OUTPUT VOLTAGE SWING vs. TEMPERATURE ($R_L = 2k\Omega$ to $V_{CC} / 2$)



COMMON-MODE REJECTION RATIO vs. TEMPERATURE

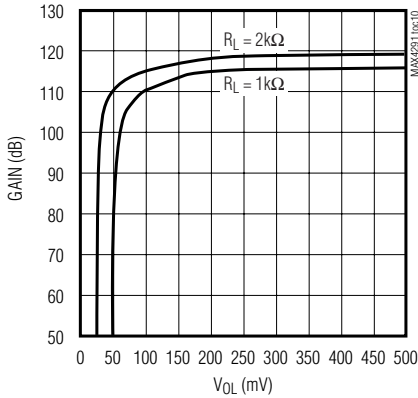


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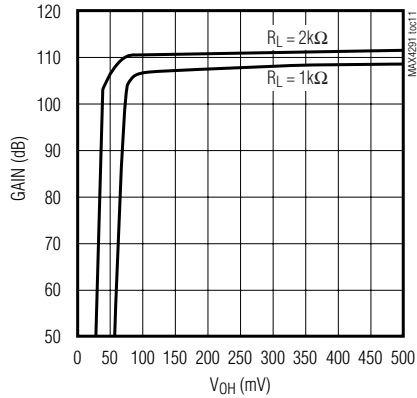
Typical Operating Characteristics (continued)

($V_{CC} = +2.4V$, $V_{EE} = V_{CM} = 0$, $V_{OUT} = V_{CC} / 2$, no load, $T_A = +25^\circ C$, unless otherwise noted.)

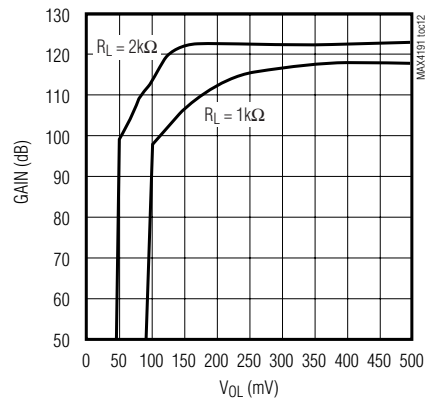
OPEN-LOOP GAIN vs. OUTPUT SWING LOW
($V_{CC} = +1.8V$, R_L CONNECTED TO V_{CC})



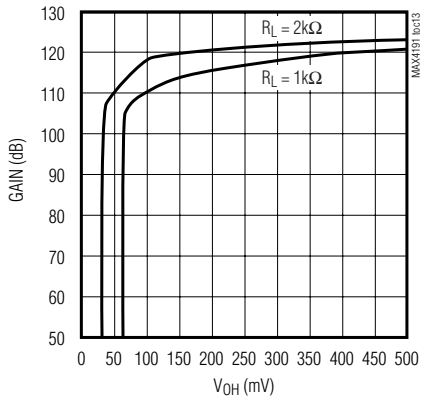
OPEN-LOOP GAIN vs. OUTPUT SWING HIGH
($V_{CC} = +1.8V$, R_L CONNECTED TO V_{EE})



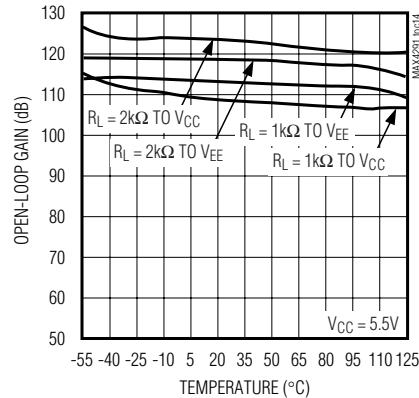
OPEN-LOOP GAIN vs. OUTPUT SWING LOW
($V_{CC} = +5.5V$, R_L CONNECTED TO V_{CC})



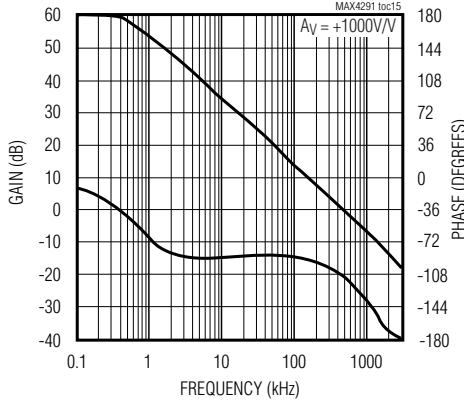
OPEN-LOOP GAIN vs. OUTPUT SWING HIGH
($V_{CC} = +5.5V$, R_L CONNECTED TO V_{EE})



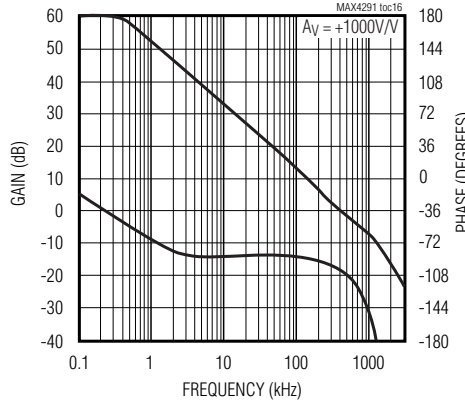
OPEN-LOOP GAIN vs. TEMPERATURE



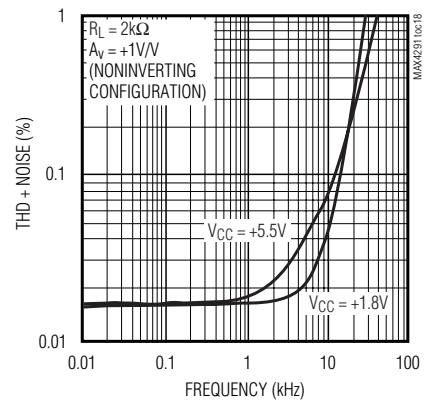
GAIN AND PHASE vs. FREQUENCY
($C_L = 0$)



GAIN AND PHASE vs. FREQUENCY
($C_L = 100pF$)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY

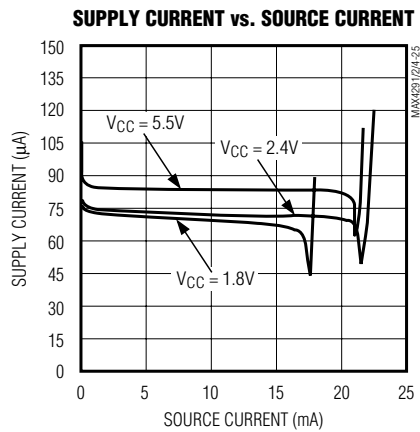
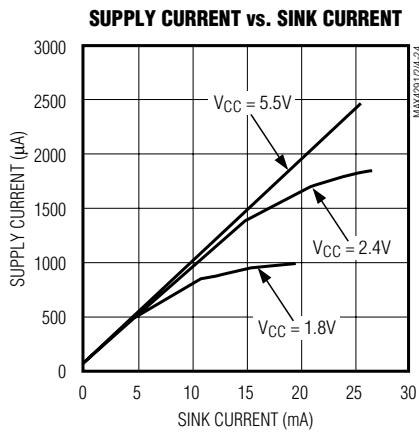
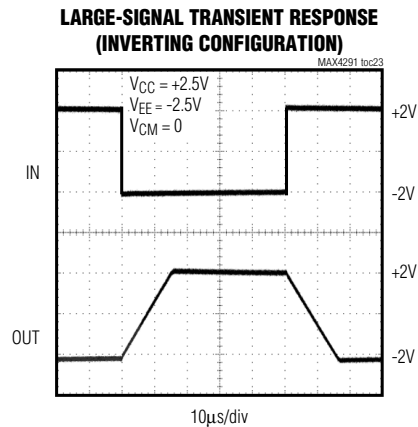
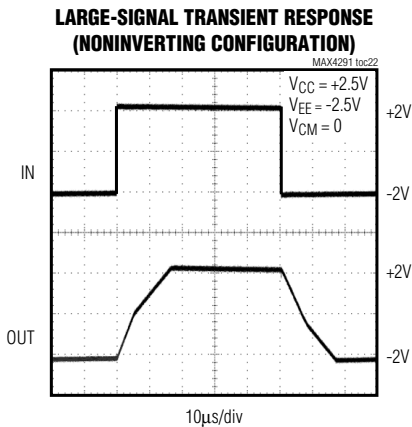
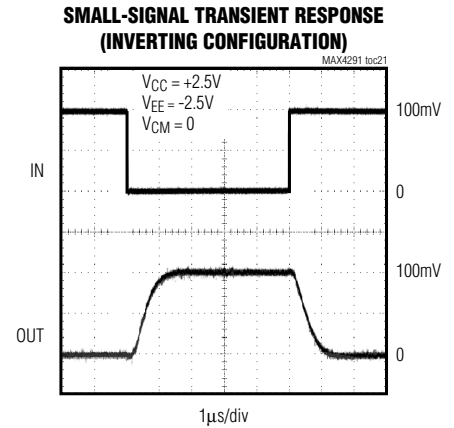
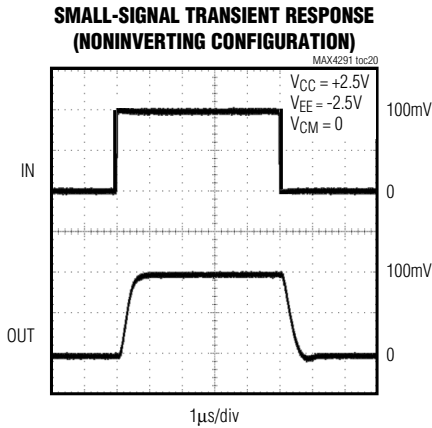
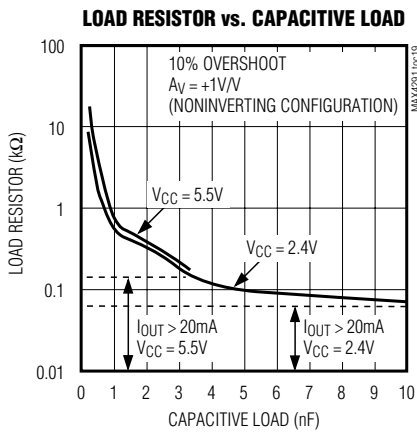


Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

Typical Operating Characteristics (continued)

($V_{CC} = +2.4V$, $V_{EE} = V_{CM} = 0$, $V_{OUT} = V_{CC} / 2$, no load, $T_A = +25^\circ C$, unless otherwise noted.)

MAX4291/MAX4292/MAX4294



Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

Pin Description

PIN			NAME	FUNCTION
MAX4291	MAX4292	MAX4294		
1	–	–	IN+	Noninverting Input
2	4	11	VEE	Negative Supply. Connect to ground for single-supply operation.
3	–	–	IN-	Inverting Input
4	–	–	OUT	Amplifier Output
5	8	4	VCC	Positive Supply
–	1, 7	1, 7	OUTA, OUTB	Outputs for Amplifiers A and B
–	2, 6	2, 6	INA-, INB-	Inverting Inputs to Amplifiers A and B
–	3, 5	3, 5	INA+, INB+	Noninverting Inputs to Amplifiers A and B
–	–	8, 14	OUTC, OUTD	Outputs for Amplifiers C and D
–	–	9, 13	INC-, IND-	Inverting Inputs to Amplifiers C and D
–	–	10, 12	INC+, IND+	Noninverting Inputs to Amplifiers C and D

Detailed Description

Rail-to-Rail Input Stage

The MAX4291/MAX4292/MAX4294 have rail-to-rail inputs and output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages, which operate together to provide a common-mode range extending to both supply rails. The crossover region of these two pairs occurs halfway between VCC and VEE. The input offset voltage is typically $\pm 400\mu\text{V}$. Low operating supply voltage, low supply current, rail-to-rail common-mode input range, and rail-to-rail outputs make this family of operational amplifiers (op amps) an excellent choice for precision or general-purpose, low-voltage, battery-powered systems.

Since the input stage consists of NPN and PNP pairs, the input bias current changes polarity as the common-mode voltage passes through the crossover region. Match the effective impedance seen by each input to reduce the offset error caused by input bias currents flowing through external source impedances (Figures 1a and 1b).

The combination of high source impedance plus input capacitance (amplifier input capacitance plus stray capacitance) creates a parasitic pole that produces an underdamped signal response. Reducing input capacitance or placing a small capacitor across the feedback resistor improves response in this case.

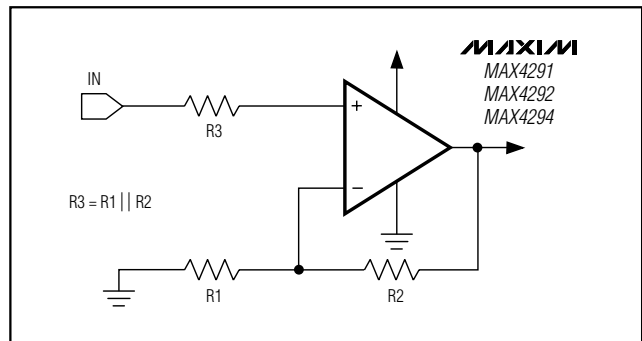


Figure 1a. Minimizing Offset Error Due to Input Bias Current (Noninverting)

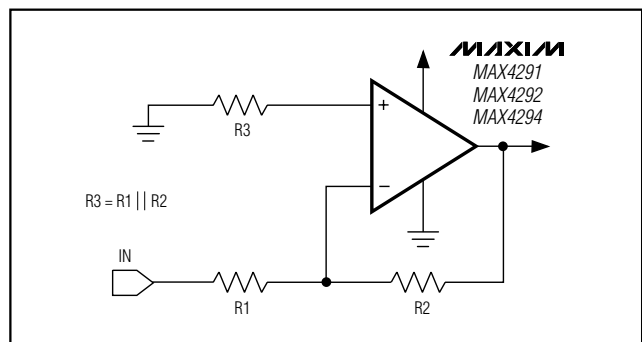


Figure 1b. Minimizing Offset Error Due to Input Bias Current (Inverting)

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

Table 1. MAX4291 Characteristics with Typical Battery Systems

BATTERY TYPE	RECHARGE-ABLE	V _{FRESH} (V)	V _{END-OF-LIFE} (V)	CAPACITY, AA SIZE (mA-h)	MAX4291 OPERATING TIME IN NORMAL MODE (h)
Alkaline (2 cells)	No	3.0	1.8	2000	20,000
Nickel-Cadmium (2 cells)	Yes	2.4	1.8	750	7500
Lithium-Ion (1 cell)	Yes	3.5	2.7	1000	10,000
Nickel-Metal-Hydride (2 cells)	Yes	2.4	1.8	1000	10,000

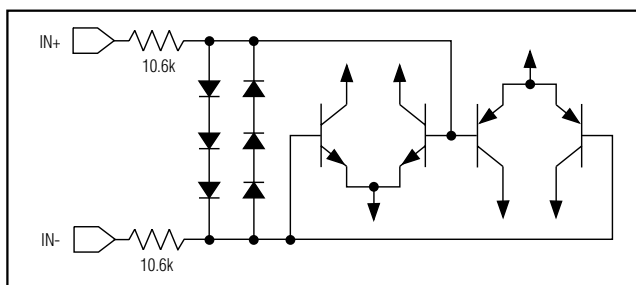


Figure 2. Input Protection Circuit

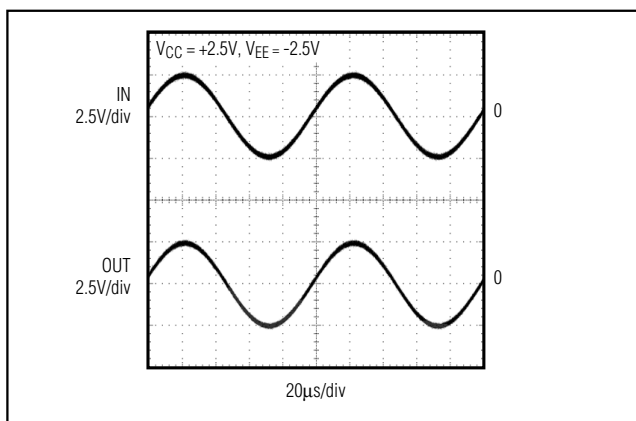


Figure 3. Rail-to-Rail Input/Output Voltage Range

The MAX4291/MAX4292/MAX4294 family's inputs are protected from large differential input voltages by internal 10.6k Ω series resistors and back-to-back triple-diode stacks across the inputs (Figure 2). For differential input voltages (much less than 1.8V), input resistance is typically 0.75M Ω . For differential input voltages greater than 1.8V, input resistance is around 21.2k Ω , and the input bias current can be approximated by the following equation:

$$I_{BIAS} = \frac{(V_{DIFF} - 1.8V)}{21.2k\Omega}$$

In the region where the differential input voltage approaches 1.8V, the input resistance decreases exponentially from 0.75M Ω to 21.2k Ω as the diode block begins to conduct. Conversely, the bias current increases with the same curve.

In unity-gain configuration, high slew rate input signals may capacitively couple to the output through the triple-diode stacks.

Rail-to-Rail Output Stage

The MAX4291/MAX4292/MAX4294 output stage can drive up to a 2k Ω load and still swing to within 20mV of the rails. Figure 3 shows the output voltage swing of a MAX4291 configured as a unity-gain buffer, powered from a $\pm 2.5V$ supply. The output for this setup typically swings from (V_{EE} + 3mV) to (V_{CC} - 2mV) with a 100k Ω load.

Applications Information

Power-Supply Considerations

The MAX4291/MAX4292/MAX4294 operate from a single +1.8V to +5.5V supply (or dual $\pm 0.9V$ to $\pm 2.75V$ supplies) and consume only 100 μA of supply current per amplifier. A high power-supply rejection ratio of 80dB allows the amplifiers to be powered directly off a decaying battery voltage, simplifying design and extending battery life.

The MAX4291/MAX4292/MAX4294 are ideally suited for use with most battery-powered systems. Table 1 lists a variety of typical battery types showing voltage when fresh, voltage at end-of-life, capacity, and approximate operating time from a MAX4291 (assuming nominal conditions).

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

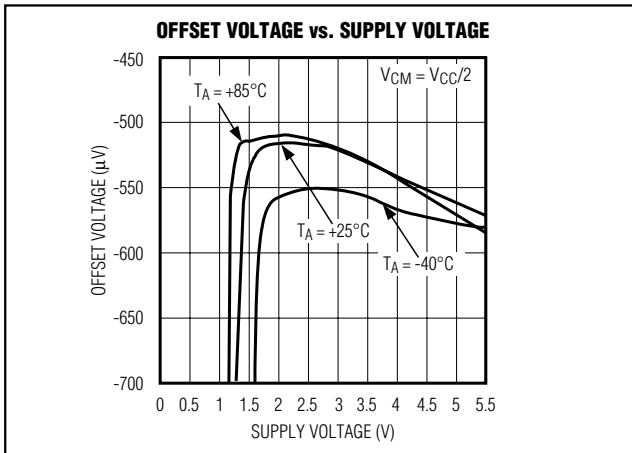


Figure 4. Offset Voltage vs. Supply Voltage

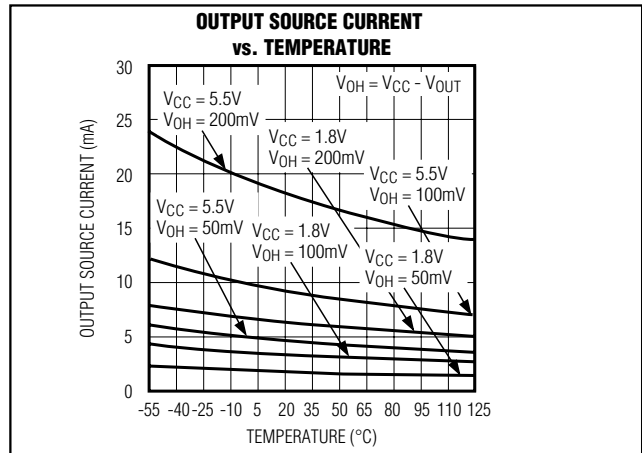


Figure 6a. Output Source Current vs. Temperature

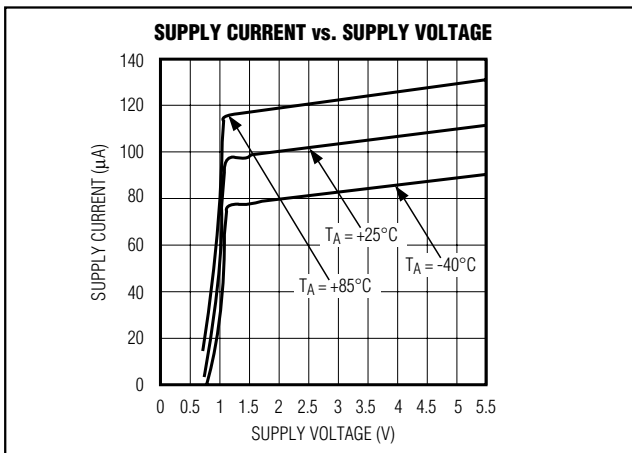


Figure 5. Supply Current vs. Supply Voltage

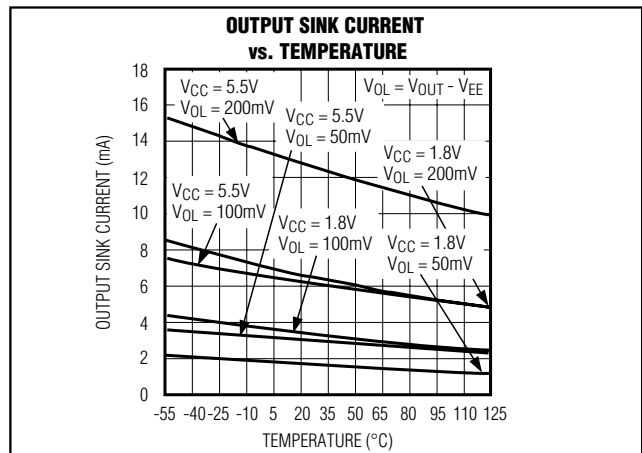


Figure 6b. Output Sink Current vs. Temperature

Although the amplifiers are fully guaranteed over temperature for operation down to a +1.8V single supply, even lower voltage operation is possible in practice. Figures 4 and 5 show the offset voltage and supply current as a function of supply voltage and temperature.

Load-Driving Capability

The MAX4291/MAX4292/MAX4294 are fully guaranteed over temperature and supply voltage range to drive a maximum resistive load of $2k\Omega$ to $V_{CC}/2$, although heavier loads can be driven in many applications. The rail-to-rail output stage of the amplifier can be modeled as a current source when driving the load toward V_{CC} , and as a current sink when driving the load toward V_{EE} . The limit of this current source/sink varies with supply voltage, ambient temperature, and lot-to-lot variations of the units.

Figures 6a and 6b show the typical current source and sink capabilities of the MAX4291/MAX4292/MAX4294 family as a function of supply voltage and ambient temperature. The contours on the graph depict the output current value, based on driving the output voltage to within 50mV, 100mV, and 200mV of either power-supply rail.

For example, a MAX4291 running from a single +1.8V supply, operating at $T_A = +25^\circ\text{C}$ can source 3.5mA to within 100mV of V_{CC} and is capable of driving a 485 Ω load resistor to V_{EE} :

$$R_L = \frac{(1.8V - 0.1V)}{3.5mA} = 485\Omega \text{ to } V_{EE}$$

The same application can drive a 220k Ω load resistor when terminated in $V_{CC}/2$ (+0.9V in this case).

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

MAX4291/MAX4292/MAX4294

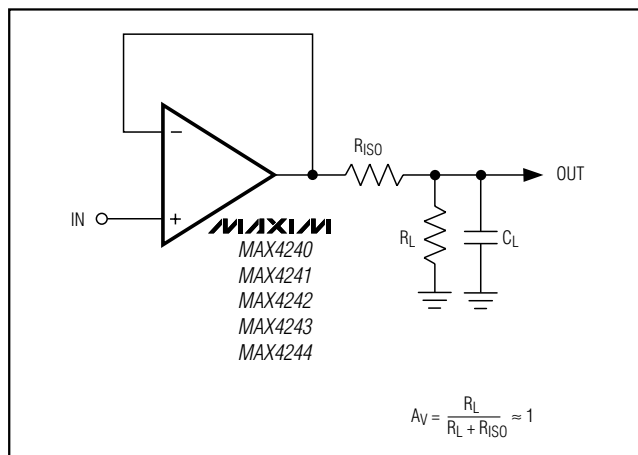


Figure 7a. Using a Resistor to Isolate a Capacitive Load from the Op Amp

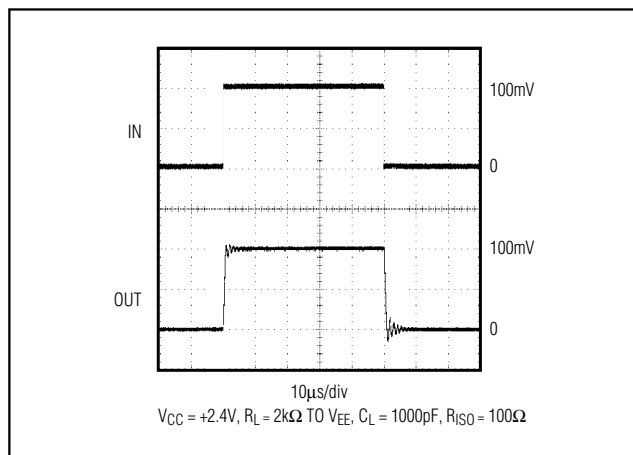


Figure 7c. Pulse Response with Isolating Resistor (100 Ω)

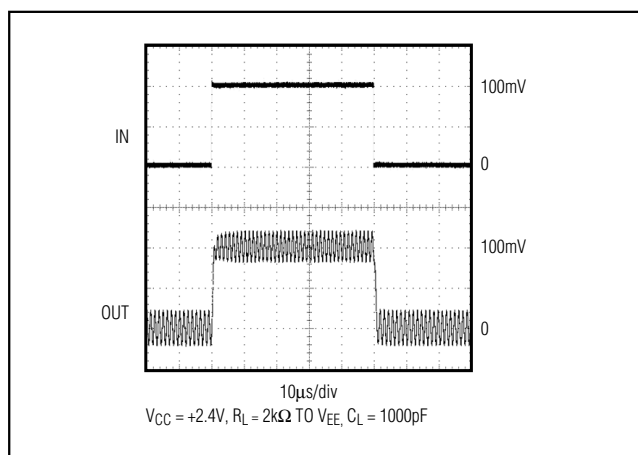


Figure 7b. Pulse Response Without Isolating Resistor

Driving Capacitive Loads

The MAX4291/MAX4292/MAX4294 are unity-gain stable for loads up to 100pF (see the Load Resistor vs. Capacitive Load graph in the *Typical Operating Characteristics*). Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load (Figure 7). Note that this alternative results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the load resistor.

Power-Supply Bypassing and Layout

The MAX4291/MAX4292/MAX4294 family operates from either a single +1.8V to +5.5V supply or dual $\pm 0.9V$ to $\pm 2.75V$ supplies. For single-supply operation, bypass the power supply with a 100nF capacitor to V_{EE} (in this case GND). For dual-supply operation, both the V_{CC}

and the V_{EE} supplies should be bypassed to ground with separate 100nF capacitors.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close as possible to the op amp. Surface-mount components are an excellent choice.

Using the MAX4291/MAX4292/MAX4294 as Comparators

Although optimized for use as operational amplifiers, the MAX4291/MAX4292/MAX4294 can also be used as rail-to-rail I/O comparators. Typical propagation delay depends on the input overdrive voltage, as shown in Figure 8. External hysteresis can be used to minimize the risk of output oscillation. The positive feedback circuit, shown in Figure 9, causes the input threshold to change when the output voltage changes state. The two thresholds create a hysteresis band that can be calculated by the following equations:

$$V_{HYST} = V_{HI} - V_{LO}$$

$$V_{HI} = \left[1 + \frac{R1}{R2} + \frac{R1}{R_{HYST}} \right] V_{REF}$$

$$V_{LO} = V_{HI} - \left(\frac{R1}{R_{HYST}} \right) V_{CC}$$

When the output of the comparator is low, the supply current increases. The output stage has biasing circuitry to monitor the output current. When the amplifier is

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

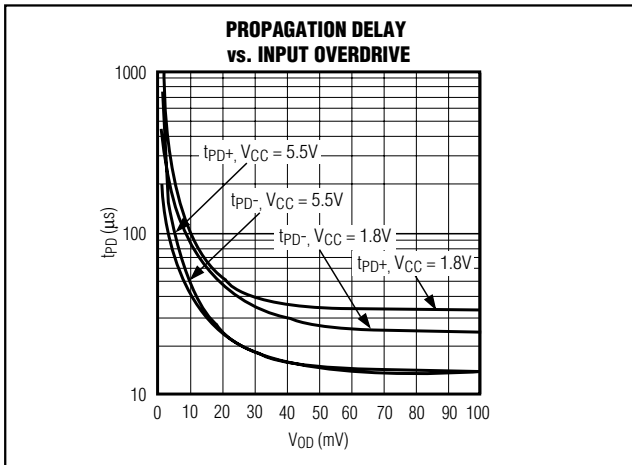


Figure 8. Propagation Delay vs. Input Overdrive

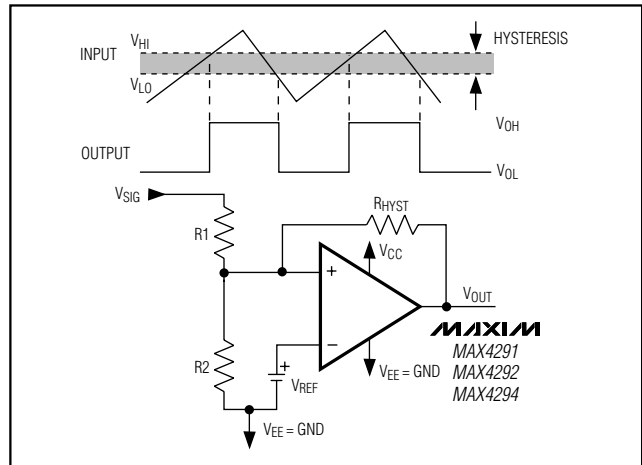


Figure 9. Hysteresis Comparator Circuit

used as a comparator, the output stage is overdriven and the current through the biasing circuitry increases to maximum. For the MAX4291, typical supply currents increase to 1.5mA with $V_{CC} = 1.8V$ and to 9mA when $V_{CC} = 5.0V$ (Figure 10).

Using the MAX4291/MAX4292/MAX4294 as Low-Power Current Monitors

The MAX4291/MAX4292/MAX4294 are ideal for applications powered from a two-cell battery stack. Figure 11 shows an application circuit in which the MAX4291 is used for monitoring the current of a two-cell battery stack. In this circuit, a current load is applied, and the voltage drop at the battery terminal is sensed.

The voltage on the load side of the battery stack is equal to the voltage at the emitter of Q1 due to the feedback loop containing the op amp. As the load current increases, the voltage drop across R1 and R2 increases. Thus, R2 provides a fraction of the load current (set by the ratio of R1 and R2) that flows into the emitter of the PNP transistor. Neglecting PNP base current, this current flows into R3, producing a ground-referenced voltage proportional to the load current. To minimize errors, scale R1 to give a voltage drop that is large enough in comparison to the op amp's V_{OS} .

Calculate the output voltage of the application using the following equation:

$$V_{OUT} = \left[I_{LOAD} \times \left(\frac{R1}{R2} \right) \right] \times R3$$

For a 1V output and a current load of 50mA, the choice of resistors can be $R1 = 2\Omega$, $R2 = 100k\Omega$, and $R3 = 1M\Omega$.

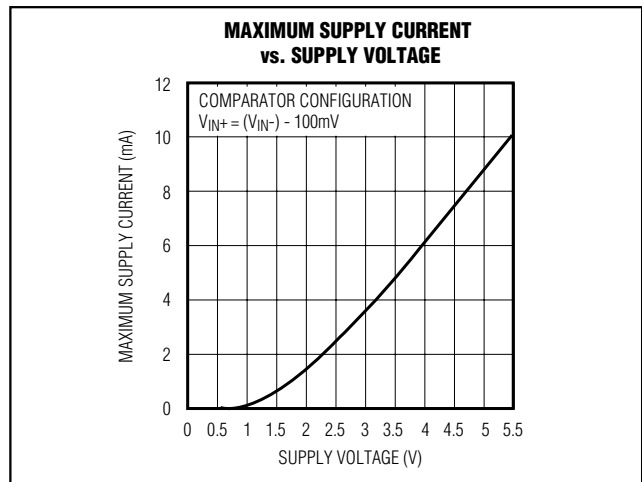


Figure 10. Maximum Supply Current vs. Supply Voltage

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

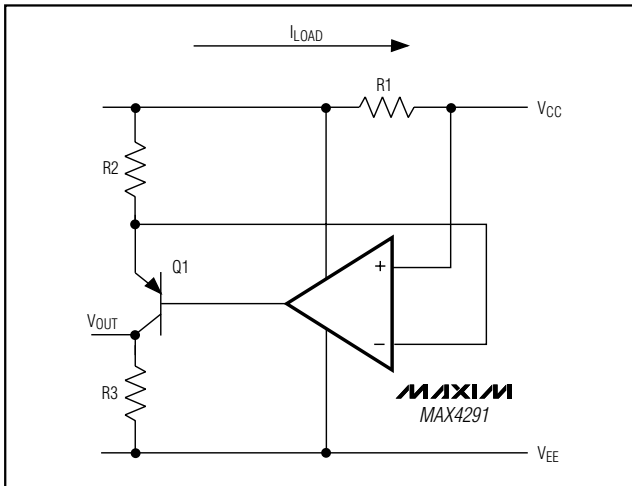
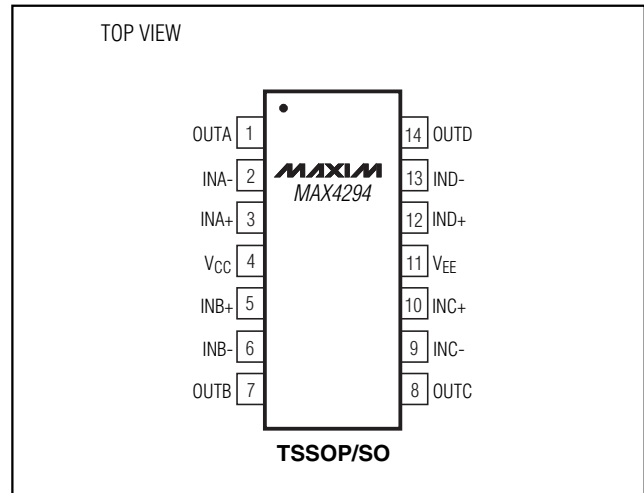


Figure 11. Current Monitor for a 2-Cell Battery Stack

Pin Configurations (continued)



Chip Information

MAX4291 TRANSISTOR COUNT: 149

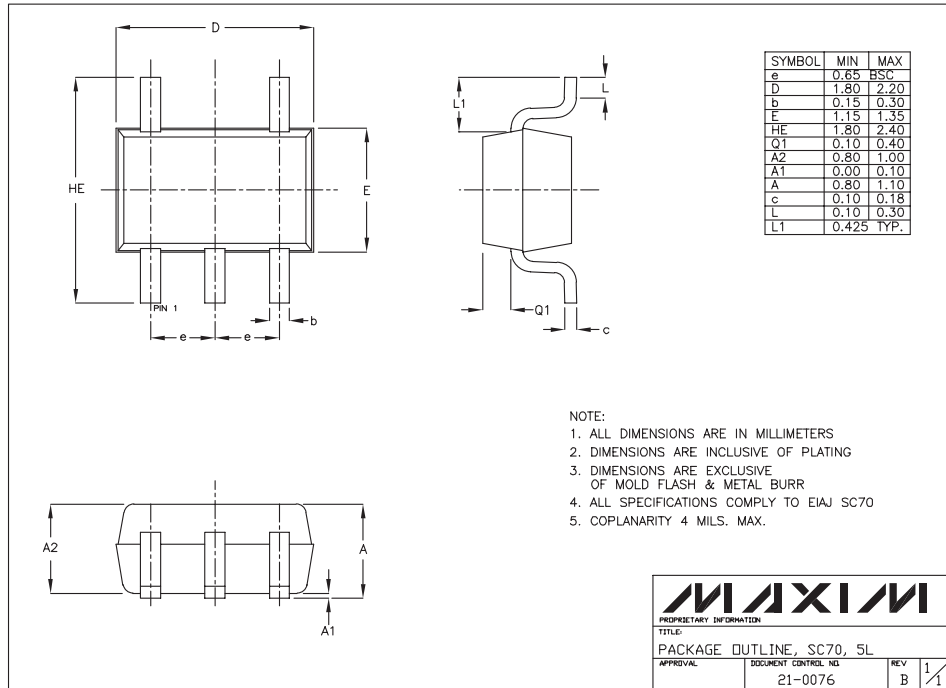
MAX4292 TRANSISTOR COUNT: 356

MAX4294 TRANSISTOR COUNT: 747

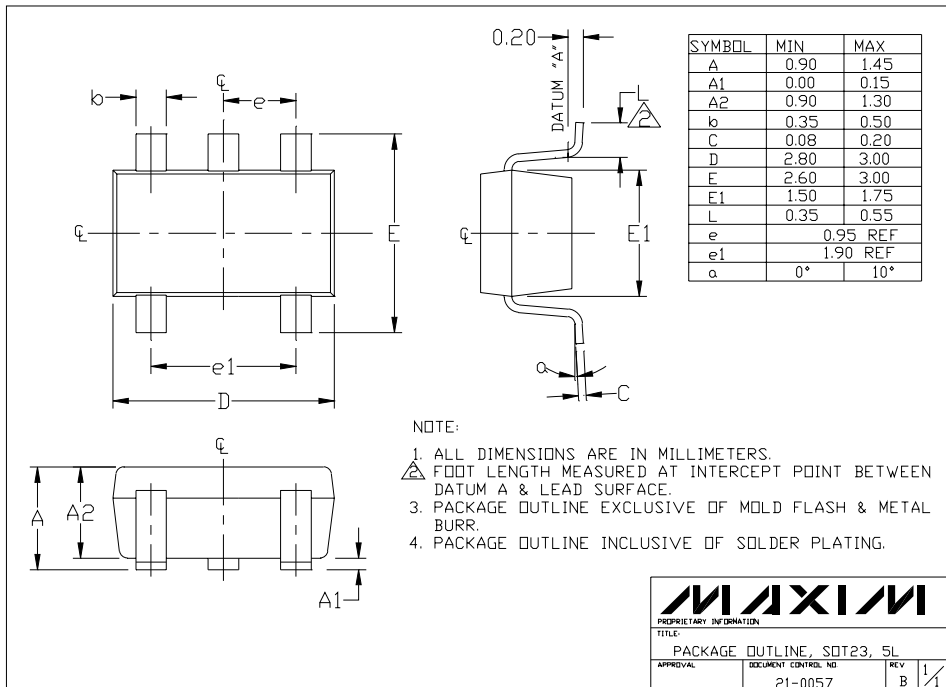
MAX4291/MAX4292/MAX4294

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

Package Information



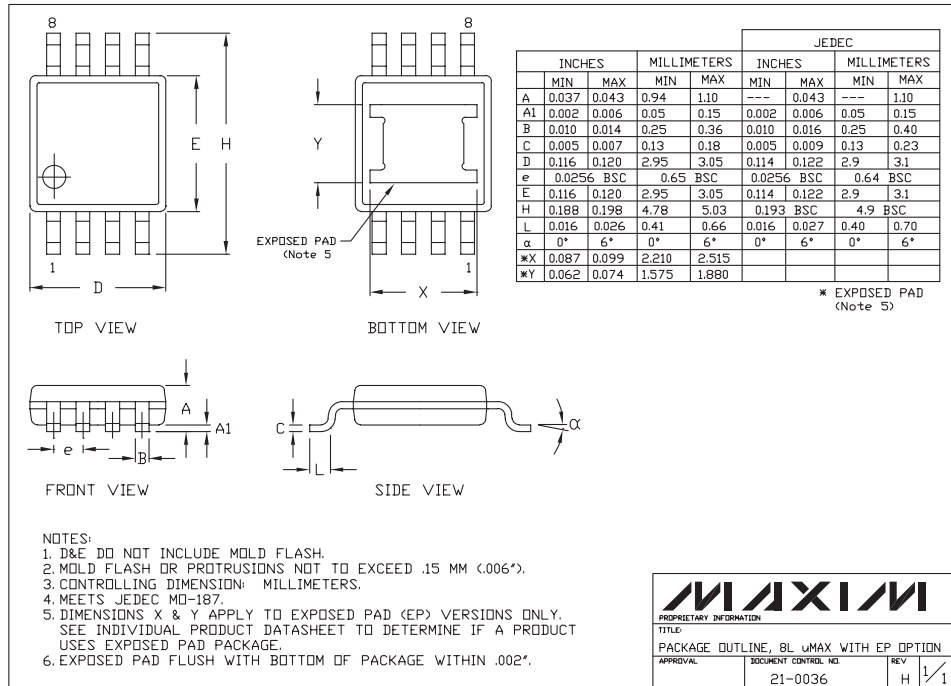
SC70, 5LEPS



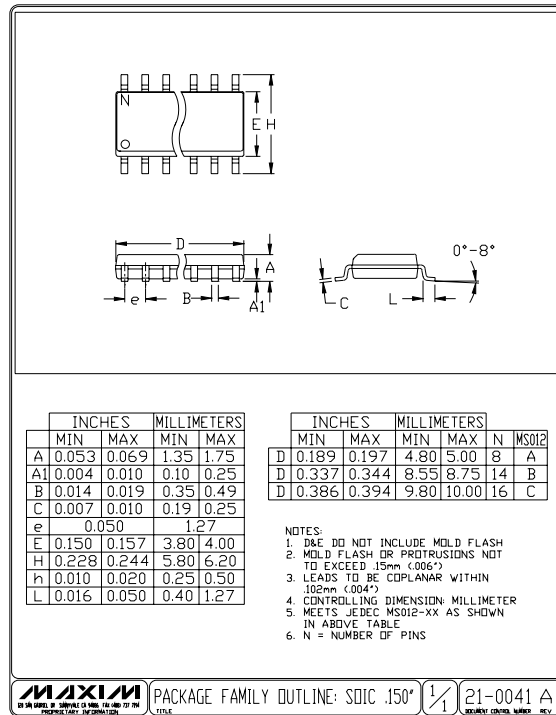
SOT23, 5L

Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

Package Information (continued)



Note: The MAX4292 does not have an exposed pad.



Ultra-Small, +1.8V, μ Power, Rail-to-Rail I/O Op Amps

Package Information (continued)

Symbol	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
A	MIN.	MAX.	MIN.	MAX.
A ₁	0.05	0.15	.002	.006
A ₂	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
⊙	0°	8°	0°	8°

JEDEC	MO-153	N	VARIATIONS			
			MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:

- DIMENSIONS D AND E DO NOT INCLUDE FLASH.
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
- CONTROLLING DIMENSION: MILLIMETER.
- MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
- DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
- EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

LEAD TIP DETAIL

WITH PLATING
BASE METAL

TSSOP-EP

Note: The MAX4294 does not have an exposed pad.

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	1/1
	21-0066	C	

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