



# Low-Voltage, CMOS Analog Multiplexers/Switches

MAX4581/MAX4582/MAX4583

## General Description

The MAX4581/MAX4582/MAX4583 are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (MAX4581), two 4-channel multiplexers (MAX4582), and three single-pole/double-throw (SPDT) switches (MAX4583).

These CMOS devices can operate continuously with  $\pm 2V$  to  $\pm 6V$  dual power supplies or a  $+2V$  to  $+12V$  single supply. Each switch can handle Rail-to-Rail<sup>®</sup> analog signals. The off-leakage current is only 1nA at  $+25^{\circ}C$  or 5nA at  $+85^{\circ}C$ .

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single  $+5V$  or dual  $\pm 5V$  supplies.

## Applications

- Battery-Operated Equipment
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- Automotive

## Features

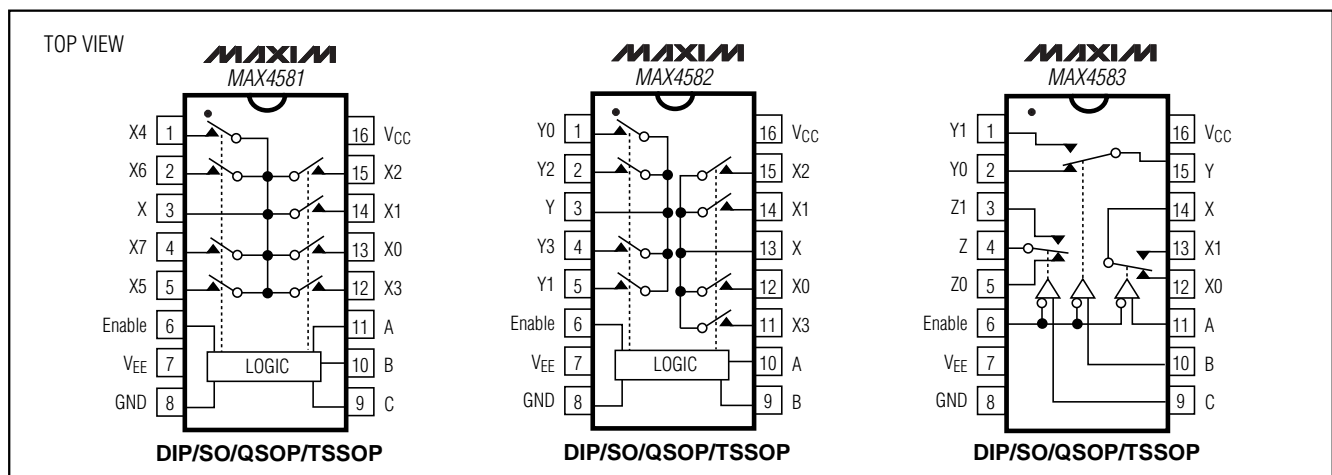
- ◆ Pin Compatible with Industry-Standard 74HC4051/74HC4052/74HC4053 and MAX4051/MAX4052/MAX4053
- ◆ Offered in Automotive Temperature Range ( $-40^{\circ}C$  to  $+125^{\circ}C$ )
- ◆ Guaranteed On-Resistance:
  - 80 $\Omega$  with  $\pm 5V$  Supplies
  - 150 $\Omega$  with Single  $+5V$  Supply
- ◆ Guaranteed On-Resistance Match Between Channels
- ◆ Guaranteed Low Off-Leakage Current: 1nA at  $+25^{\circ}C$
- ◆ Guaranteed Low On-Leakage Current: 1nA at  $+25^{\circ}C$
- ◆  $+2V$  to  $+12V$  Single-Supply Operation
- ◆  $\pm 2V$  to  $\pm 6V$  Dual-Supply Operation
- ◆ TTL/CMOS-Logic Compatible
- ◆ Low Distortion:  $< 0.02\%$  (600 $\Omega$ )
- ◆ Low Crosstalk:  $< -96dB$  (50 $\Omega$ , MAX4582)
- ◆ High Off-Isolation:  $< -74dB$  (50 $\Omega$ )

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4581CPE	0 $^{\circ}C$ to $+70^{\circ}C$	16 Plastic DIP
MAX4581CSE	0 $^{\circ}C$ to $+70^{\circ}C$	16 Narrow SO
MAX4581CUE	0 $^{\circ}C$ to $+70^{\circ}C$	16 TSSOP

Ordering Information continued at end of data sheet.

## Pin Configurations/Functional Diagrams



Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.



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## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V <sub>EE</sub>		Narrow SO (derate 8.70mW/°C above +70°C).....	696mW
V <sub>CC</sub> .....	-0.3V to 13V	QSOP (derate 8.3mW/°C above +70°C) .....	667mW
Voltage into Any Terminal (Note 1) ... (V <sub>EE</sub> - 0.3V) to (V <sub>CC</sub> + 0.3V)		TSSOP (derate 6.7mW/°C above +70°C) .....	457mW
Continuous Current into Any Terminal .....	±20mA	Operating Temperature Ranges	
Peak Current, X <sub>-</sub> , Y <sub>-</sub> , Z <sub>-</sub>		MAX458_C_ .....	0°C to +70°C
(pulsed at 1ms, 10% duty cycle) .....	±40mA	MAX458_E_ .....	-40°C to +85°C
ESD per Method 3015.7 .....	>2000V	MAX458_A_ .....	-40°C to +125°C
Continuous Power Dissipation (T <sub>A</sub> = +70°C)		Storage Temperature Range .....	-65°C to +150°C
Plastic DIP (derate 10.53mW/°C above +70°C).....	842mW	Lead Temperature (soldering, 10sec) .....	+300°C

**Note 1:** Voltages exceeding V<sub>CC</sub> or V<sub>EE</sub> on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Dual Supplies

(V<sub>CC</sub> = 4.5V to 5.5V, V<sub>EE</sub> = -4.5V to -5.5V, V<sub>H</sub> = 2.4V, V<sub>L</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP (Note 2)	MAX	UNITS	
<b>ANALOG SWITCH</b>								
Analog-Signal Range	V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub>		C, E, A	V <sub>EE</sub>		V <sub>CC</sub>	V	
Switch On-Resistance	R <sub>ON</sub>	V <sub>CC</sub> = 4.5V; V <sub>EE</sub> = -4.5V; I <sub>X</sub> , I <sub>Y</sub> , I <sub>Z</sub> = 1mA; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 3.5V	+25°C		50	80	Ω	
			C, E, A			100		
Switch On-Resistance Match Between Channels (Note 3)	ΔR <sub>ON</sub>	V <sub>CC</sub> = 4.5V; V <sub>EE</sub> = -4.5V; I <sub>X</sub> , I <sub>Y</sub> , I <sub>Z</sub> = 1mA; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 3.5V	+25°C		1	4	Ω	
			C, E, A			6		
Switch On-Resistance Flatness (Note 4)	R <sub>FLAT(ON)</sub>	V <sub>CC</sub> = 5V; V <sub>EE</sub> = -5V; I <sub>X</sub> , I <sub>Y</sub> , I <sub>Z</sub> = 1mA; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 3V, 0V, -3V	+25°C		4	10	Ω	
			C, E, A			12		
X <sub>-</sub> , Y <sub>-</sub> , Z <sub>-</sub> Off Leakage (Note 5)	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub> , I <sub>Z(OFF)</sub>	V <sub>CC</sub> = 5.5V; V <sub>EE</sub> = -5.5V; V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = ±4.5V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = ∓4.5V	+25°C	-1		1	nA	
			C, E, A	-10		10		
X, Y, Z Off Leakage (Note 5)	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub> , I <sub>Z(OFF)</sub>	V <sub>CC</sub> = 5.5V; V <sub>EE</sub> = -5.5V; V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = ±4.5V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = ∓4.5V	MAX4581	+25°C	-2		2	nA
			MAX4582 MAX4583	C, E, A	-100		100	
				+25°C	-1		1	
X, Y, Z On Leakage (Note 5)	I <sub>X(ON)</sub> , I <sub>Y(ON)</sub> , I <sub>Z(ON)</sub>	V <sub>CC</sub> = 5.5V; V <sub>EE</sub> = -5.5V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = ±4.5V	MAX4581	+25°C	-2		2	nA
			MAX4582 MAX4583	C, E, A	-100		100	
				+25°C	-1		1	
MAX4582 MAX4583			C, E, A	-50		50		
			+25°C	-1		1		
<b>DIGITAL I/O</b>								
Logic Input Logic Threshold High	V <sub>AH</sub> , V <sub>BH</sub> , V <sub>CH</sub>		C, E, A		1.5	2.4	V	
Logic Input Logic Threshold Low	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>CL</sub>		C, E, A	0.8	1.5		V	

# Low-Voltage, CMOS Analog Multiplexers/Switches

MAX4581/MAX4582/MAX4583

## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

( $V_{CC} = 4.5V$  to  $5.5V$ ,  $V_{EE} = -4.5V$  to  $-5.5V$ ,  $V_H = 2.4V$ ,  $V_L = 0.8V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP (Note 2)	MAX	UNITS
Input Current High	$I_{AH}$ , $I_{BH}$ , $I_{CH}$	$V_A, V_B, V_C = 2.4V$	C, E, A	-1		1	$\mu A$
Input Current Low	$I_{AL}$ , $I_{BL}$ , $I_{CL}$	$V_A, V_B, V_C = 0.8V$	C, E, A	-1		1	$\mu A$
<b>SWITCH DYNAMIC CHARACTERISTICS</b>							
Inhibit Turn-On Time	$t_{(ON)}$	$V_{X-}, V_{Y-}, V_{Z-} = 3V$ ; $R_L = 300\Omega$ ; $C_L = 35pF$ ; Figure 3	$T_A = +25^\circ C$ C, E, A		100	200	ns
Inhibit Turn-Off Time	$t_{(OFF)}$	$V_{X-}, V_{Y-}, V_{Z-} = 3V$ ; $R_L = 300\Omega$ ; $C_L = 35pF$ ; Figure 3	$T_A = +25^\circ C$ C, E, A		40	100	ns
Address Transition Time	$t_{TRANS}$	$V_{X-}, V_{Y-}, V_{Z-} = \pm 3V$ ; $R_L = 300\Omega$ ; $C_L = 35pF$ ; Figure 2	$T_A = +25^\circ C$ C, E, A		90	200	ns
Break-Before-Make Time	$t_{BBM}$	$V_{X-}, V_{Y-}, V_{Z-} = 3V$ ; $R_L = 300\Omega$ ; $C_L = 35pF$ ; Figure 4	$T_A = +25^\circ C$	4	20		ns
Charge Injection (Note 6)	Q	$C = 1nF$ , $R_S = 0\Omega$ , $V_S = 0V$	$T_A = +25^\circ C$		0.5	5	pC
Input Off Capacitance	$C_{X(OFF)}$ , $C_{Y(OFF)}$ , $C_{Z(OFF)}$	$V_{X-}, V_{Y-}, V_{Z-} = 0V$ ; $f = 1MHz$ ; Figure 7	$T_A = +25^\circ C$		4		pF
Output Off Capacitance	$C_{X(OFF)}$ , $C_{Y(OFF)}$ , $C_{Z(OFF)}$	$V_{X-}, V_{Y-}, V_{Z-} = 0V$ ; $f = 1MHz$ ; Figure 7	$T_A = +25^\circ C$	MAX4581	18		pF
				MAX4582	10		
				MAX4583	6		
Output On Capacitance	$C_{X(ON)}$ , $C_{Y(ON)}$ , $C_{Z(ON)}$	$V_{X-}, V_{Y-}, V_{Z-} = 0V$ ; $f = 1MHz$ ; Figure 7	$T_A = +25^\circ C$	MAX4581	25		pF
				MAX4582	17		
				MAX4583	12.5		
Off Isolation	$V_{ISO}$	$R_L = 50\Omega$ , $f = 1MHz$ , Figure 6	$T_A = +25^\circ C$		-73		dB
Channel-to-Channel Crosstalk	$V_{CT}$	$R_L = 50\Omega$ , $f = 1MHz$ , Figure 6	MAX4582	$T_A = +25^\circ C$	-96		pF
			MAX4583	$T_A = +25^\circ C$	-73		
Total Harmonic Distortion	THD	$R_L = 600\Omega$ , $5Vp-p$ , $f = 20Hz$ to $20kHz$	$T_A = +25^\circ C$		0.02		%
<b>POWER SUPPLY</b>							
Power-Supply Range	$V_{CC}$ , $V_{EE}$		C, E, A	$\pm 2$		$\pm 6$	V
Power-Supply Current	$I_{CC}$ , $I_{EE}$	$V_{CC} = 5.5V$ , $V_{EE} = -5.5V$ , $V_A, V_B, V_C, V_{Enable} = V+$ or $0$	$T_A = +25^\circ C$	-1		1	$\mu A$
			C, E, A	-10		10	

**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

**Note 3:**  $\Delta RON = RON(MAX) - RON(MIN)$ .

**Note 4:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e.,  $V_{X-}, V_{Y-}, V_{Z-} = 3V$  to  $0$  and  $0$  to  $-3V$ .

**Note 5:** Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at  $T_A = +25^\circ C$ .

**Note 6:** Guaranteed by design, not production tested.

# Low-Voltage, CMOS Analog Multiplexers/Switches

## ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V<sub>CC</sub> = 4.5V to 5.5V, V<sub>EE</sub> = 0V, V<sub>H</sub> = 2.4V, V<sub>L</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP (Note 2)	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog-Signal Range	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> , V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub>		C, E, A	V <sub>EE</sub>		V <sub>CC</sub>	V
Switch On-Resistance	R <sub>ON</sub>	V <sub>CC</sub> = 4.5V; I <sub>X</sub> , I <sub>Y</sub> , I <sub>Z</sub> = 1mA; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 3.5V	T <sub>A</sub> = +25°C C, E, A		90	150 200	Ω
Switch On-Resistance Match Between Channels (Note 3)	ΔR <sub>ON</sub>	V <sub>CC</sub> = 4.5V; I <sub>X</sub> , I <sub>Y</sub> , I <sub>Z</sub> = 1mA; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 3.5V	T <sub>A</sub> = +25°C C, E, A		2	8 10	Ω
X <sub>-</sub> , Y <sub>-</sub> , Z <sub>-</sub> Off Leakage (Note 5)	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub> , I <sub>Z(OFF)</sub>	V <sub>CC</sub> = 5.5V; V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 1V, 4.5V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 4.5V, 1V	T <sub>A</sub> = +25°C C, E, A	-1		1 10	nA
X, Y, Z Off Leakage (Note 5)	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub> , I <sub>Z(OFF)</sub>	V <sub>CC</sub> = 5.5V; V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 1V, 4.5V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 4.5V, 1V	MAX4581	T <sub>A</sub> = +25°C	-2	2	nA
				C, E, A	-100	100	
			MAX4582 MAX4583	T <sub>A</sub> = +25°C C, E, A	-1 -50	1 50	
X, Y, Z On Leakage (Note 5)	I <sub>X(ON)</sub> , I <sub>Y(ON)</sub> , I <sub>Z(ON)</sub>	V <sub>CC</sub> = 5.5V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 4.5V, 1V	MAX4581	T <sub>A</sub> = +25°C	-2	2	nA
				C, E, A	-100	100	
			MAX4582 MAX4583	T <sub>A</sub> = +25°C C, E, A	-1 -50	1 50	
<b>DIGITAL I/O</b>							
Logic Input Logic Threshold High	V <sub>AH</sub> , V <sub>BH</sub> , V <sub>CH</sub> , V <sub>EnableH</sub>		C, E, A		1.5	2.4	V
Logic Input Logic Threshold Low	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>CL</sub> , V <sub>EnableL</sub>		C, E, A	0.8	1.5		V
Input Current High	I <sub>AH</sub> , I <sub>BH</sub> , I <sub>CH</sub> , I <sub>EnableH</sub>	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>CL</sub> , V <sub>EnableL</sub> = 2.4V	C, E, A	-1		1	μA
Input Current Low	I <sub>AL</sub> , I <sub>BL</sub> , I <sub>CL</sub> , I <sub>EnableL</sub>	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>CL</sub> , V <sub>EnableL</sub> = 0.8V	C, E, A	-1		1	μA
<b>SWITCH DYNAMIC CHARACTERISTICS</b>							
Charge Injection (Note 6)	Q	C = 1nF, R <sub>S</sub> = 0Ω, V <sub>S</sub> = 2.5V	T <sub>A</sub> = +25°C		0.8	5	pC
Enable Turn-On Time	t <sub>(ON)</sub>	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 3	T <sub>A</sub> = +25°C		100	200	ns
				C, E, A		250	
Enable Turn-Off Time	t <sub>(OFF)</sub>	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 3	T <sub>A</sub> = +25°C		40	100	ns
				C, E, A		150	
Address Transition Time	t <sub>TRANS</sub>	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 3V/0V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 2	T <sub>A</sub> = +25°C		80	200	ns
				C, E, A		250	
Break-Before-Make Time	t <sub>BBM</sub>	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 4	T <sub>A</sub> = +25°C	10	30		ns

**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

**Note 3:** ΔR<sub>ON</sub> = R<sub>ON(MAX)</sub> - R<sub>ON(MIN)</sub>.

**Note 4:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges; i.e., V<sub>X-</sub>, V<sub>Y-</sub>, V<sub>Z-</sub> = 3V to 0 and 0 to -3V.

**Note 5:** Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T<sub>A</sub> = +25°C.

**Note 6:** Guaranteed by design, not production tested.

# Low-Voltage, CMOS Analog Multiplexers/Switches

MAX4581/MAX4582/MAX4583

## ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V<sub>CC</sub> = 2.7V to 3.6V, V<sub>EE</sub> = 0V, V<sub>H</sub> = 2.0V, V<sub>L</sub> = 0.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP (Note 2)	MAX	UNITS
<b>POWER SUPPLY</b>							
Power-Supply Range	V <sub>CC</sub> , V <sub>EE</sub>		C, E, A	2		12	V
Power-Supply Current	I <sub>CC</sub> , I <sub>EE</sub>	V <sub>CC</sub> = 3.6V; V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> , V <sub>Enable</sub> = V+ or 0	T <sub>A</sub> = +25°C	-1		1	μA
			C, E, A	-10		10	
<b>ANALOG SWITCH</b>							
Analog-Signal Range	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> , V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub>		C, E, A	V <sub>EE</sub>		V <sub>CC</sub>	V
Switch On-Resistance	R <sub>ON</sub>	V <sub>CC</sub> = 2.7V; I <sub>X</sub> , I <sub>Y</sub> , I <sub>Z</sub> = 0.1mA; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 1.5V	T <sub>A</sub> = +25°C		190	450	Ω
			C, E, A			550	
X <sub>-</sub> , Y <sub>-</sub> , Z <sub>-</sub> Off Leakage (Note 5)	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub> , I <sub>Z(OFF)</sub>	V <sub>CC</sub> = 3.6V; V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 1V, 3V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 3V, 1V	T <sub>A</sub> = +25°C	-1		1	nA
			C, E, A	-10		10	
X, Y, Z Off Leakage (Note 6)	I <sub>X(OFF)</sub> , I <sub>Y(OFF)</sub> , I <sub>Z(OFF)</sub>	V <sub>CC</sub> = 3.6V; V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 1V, 3.0V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 3.0V, 1V	MAX4581	T <sub>A</sub> = +25°C	-2	2	nA
			MAX4582 MAX4583	C, E, A	-100	100	
				C, E, A	-50	50	
X, Y, Z On Leakage (Note 6)	I <sub>X(ON)</sub> , I <sub>Y(ON)</sub> , I <sub>Z(ON)</sub>	V <sub>CC</sub> = 3.6V; V <sub>X</sub> , V <sub>Y</sub> , V <sub>Z</sub> = 3.0V, 1V	MAX4581	T <sub>A</sub> = +25°C	-2	2	nA
			MAX4582 MAX4583	C, E, A	-100	100	
				C, E, A	-50	50	
<b>DIGITAL I/O</b>							
Logic Input Logic Threshold High	V <sub>AH</sub> , V <sub>BH</sub> , V <sub>CH</sub> , V <sub>EnableH</sub>		C, E, A		1.0	2.0	V
Logic Input Logic Threshold Low	V <sub>AL</sub> , V <sub>BL</sub> , V <sub>CL</sub> , V <sub>EnableL</sub>		C, E, A	0.5	1.0		V
Input Current High	I <sub>AH</sub> , I <sub>BH</sub> , I <sub>CH</sub> , I <sub>EnableH</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> = V <sub>Enable</sub> = 2.0V	C, E, A	-1		1	μA
Input Current Low	I <sub>AL</sub> , I <sub>BL</sub> , I <sub>CL</sub> , I <sub>EnableL</sub>	V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> = V <sub>Enable</sub> = 0.5V	C, E, A	-1		1	μA
<b>SWITCH DYNAMIC CHARACTERISTICS</b> (Note 6)							
Enable Turn-On Time	t <sub>(ON)</sub>	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 1.5V; R <sub>L</sub> = 300Ω; C <sub>L</sub> = 35pF; Figure 3	T <sub>A</sub> = +25°C		170	300	ns
			C, E, A			400	
Enable Turn-Off Time	t <sub>(OFF)</sub>	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 1.5V; R <sub>L</sub> = 300Ω; C <sub>L</sub> = 35pF; Figure 3	T <sub>A</sub> = +25°C		50	200	ns
			C, E, A			300	
Address Transition Time	t <sub>TRANS</sub>	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 1.5V/0V; R <sub>L</sub> = 300Ω; C <sub>L</sub> = 35pF; Figure 2	T <sub>A</sub> = +25°C		130	300	ns
			C, E, A			400	
Break-Before-Make Time	t <sub>BBM</sub>	V <sub>X-</sub> , V <sub>Y-</sub> , V <sub>Z-</sub> = 1.5V; R <sub>L</sub> = 300Ω; C <sub>L</sub> = 35pF	T <sub>A</sub> = +25°C	15	40		ns
<b>POWER SUPPLY</b>							
Power-Supply Current	I <sub>CC</sub> , I <sub>EE</sub>	V <sub>CC</sub> = 3.6V, V <sub>A</sub> , V <sub>B</sub> , V <sub>C</sub> , V <sub>Enable</sub> = V+ or 0	T <sub>A</sub> = +25°C	-1		1	μA
			C, E, A	-10		10	

**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

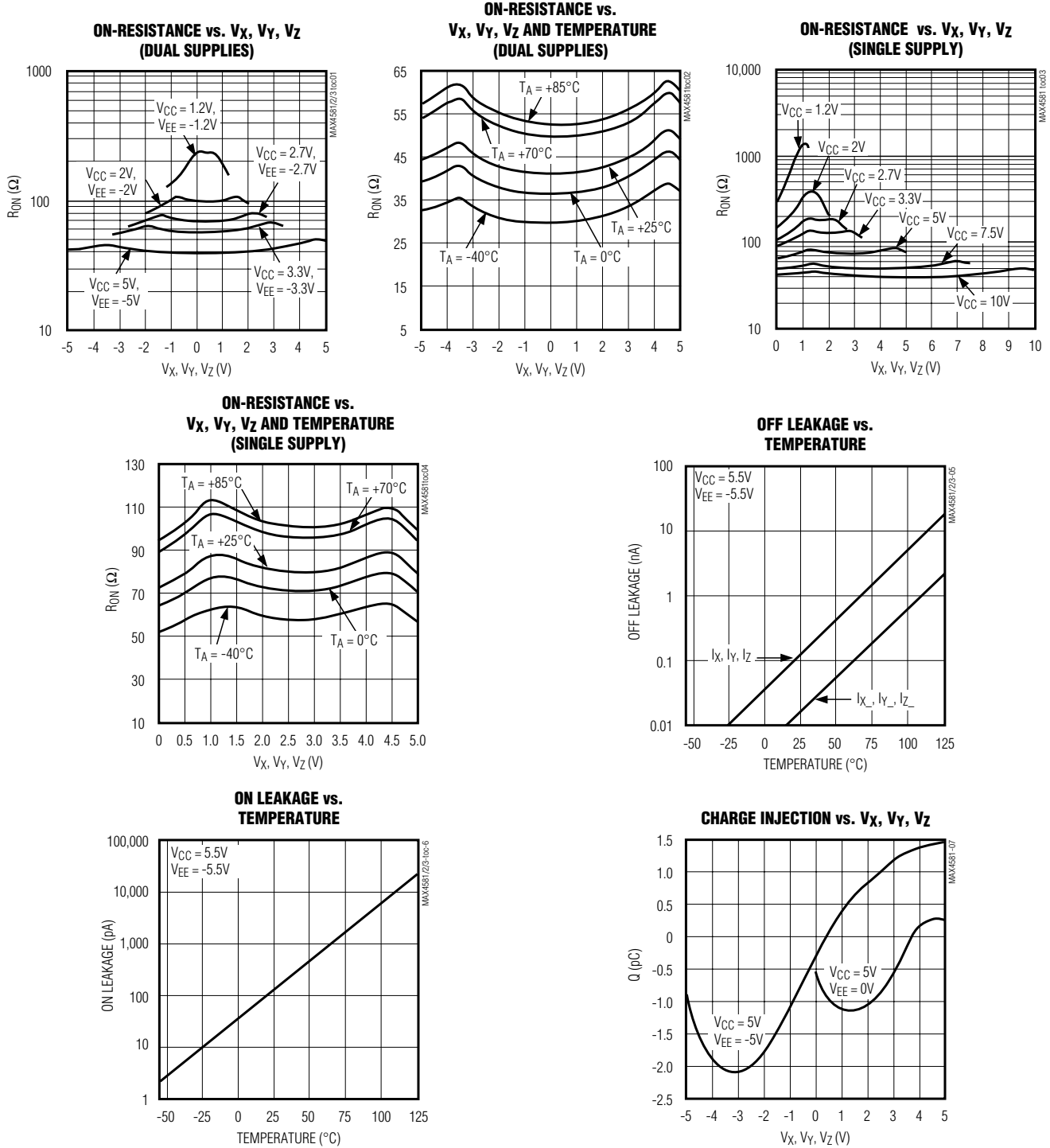
**Note 5:** Leakage parameters are 100% tested at maximum-rated hot operating temperature, and guaranteed by correlation at T<sub>A</sub> = +25°C.

**Note 6:** Guaranteed by design, not production tested.

# Low-Voltage, CMOS Analog Multiplexers/Switches

## Typical Operating Characteristics

( $V_{CC} = 5V$ ,  $V_{EE} = -5V$ ,  $GND = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

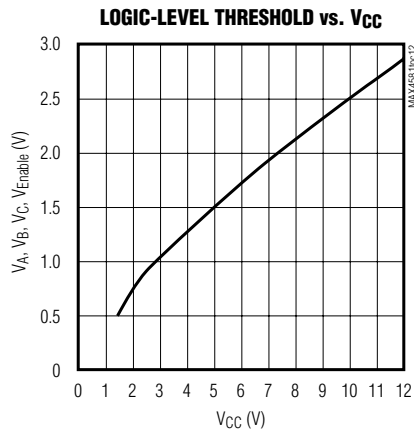
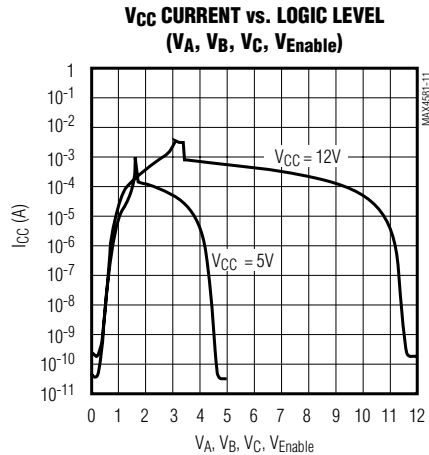
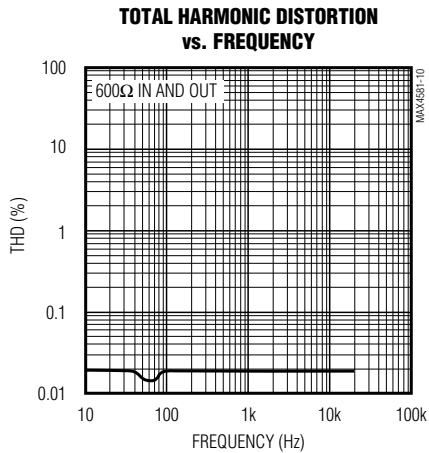
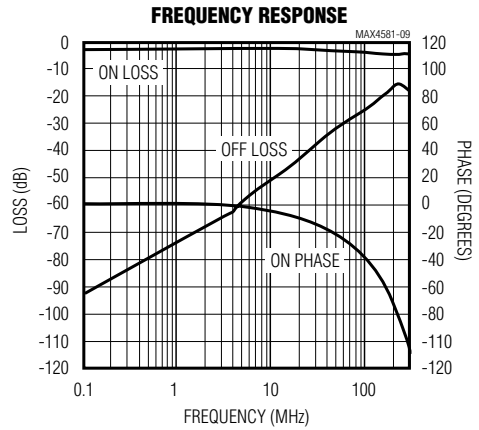
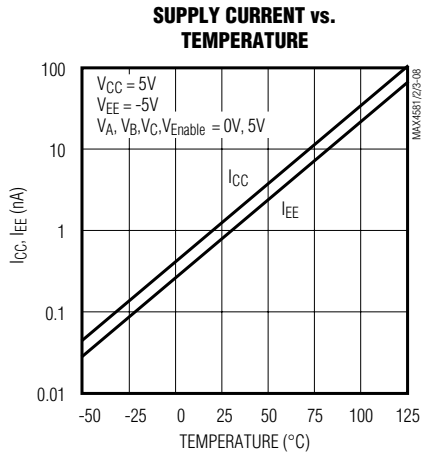


# Low-Voltage, CMOS Analog Multiplexers/Switches

## Typical Operating Characteristics (continued)

( $V_{CC} = 5V$ ,  $V_{EE} = -5V$ ,  $GND = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX4581/MAX4582/MAX4583



# Low-Voltage, CMOS Analog Multiplexers/Switches

## Pin Description

PIN			NAME	FUNCTION
MAX4581	MAX4582	MAX4583		
13, 14, 15, 12, 1, 5, 2, 4	—	—	X0–X7	Analog Switch Inputs 0–7
3	—	—	X	Analog Switch Output
—	12, 14, 15, 11	—	X0, X1, X2, X3	Analog Switch “X” Inputs 0–3
—	13	14	X	Analog Switch “X” Output
—	—	13	X1	Analog Switch “X” Normally Open Input
—	—	12	X0	Analog Switch “X” Normally Closed Input
—	—	1	Y1	Analog Switch “Y” Normally Open Input
—	—	2	Y0	Analog Switch “Y” Normally Closed Input
6	6	6	Enable	Digital Enable Input. Normally connect to GND. Can be driven to logic high to set all switches off.
7	7	7	VEE	Negative Analog Supply-Voltage Input. Connect to GND for single-supply operation.
8	8	8	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V <sub>CC</sub> and V <sub>EE</sub> .)
11	10	11	A	Digital Address “A” Input
10	9	10	B	Digital Address “B” Input
9	—	9	C	Digital Address “C” Input
—	1, 5, 2, 4	—	Y0, Y1, Y2, Y3	Analog Switch “Y” Inputs 0–3
—	3	15	Y	Analog Switch “Y” Output
—	—	5	Z0	Analog Switch “Z” Normally Closed Input
—	—	3	Z1	Analog Switch “Z” Normally Open Input
—	—	4	Z	Analog Switch “Z” Output
16	16	16	V <sub>CC</sub>	Positive Analog and Digital Supply Voltage Input

**Note:** Input and output pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

## Applications Information

### Power-Supply Considerations

#### Overview

The MAX4581/MAX4582/MAX4583 construction is typical of most CMOS analog switches. They have three supply pins: V<sub>CC</sub>, V<sub>EE</sub>, and GND. V<sub>CC</sub> and V<sub>EE</sub> are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V<sub>CC</sub> and V<sub>EE</sub>. If any analog signal exceeds V<sub>CC</sub> or V<sub>EE</sub>, one of these diodes will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V<sub>CC</sub> or V<sub>EE</sub>.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V<sub>CC</sub> or V<sub>EE</sub> and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V<sub>CC</sub> and V<sub>EE</sub> pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND.



# Low-Voltage, CMOS Analog Multiplexers/Switches

MAX4581/MAX4582/MAX4583

**Table 1. Truth Table/Switch Programming**

ENABLE INPUT	SELECT INPUTS			ON SWITCHES		
	C*	B	A	MAX4581	MAX4582	MAX4583
H	X	X	X	All switches open	All switches open	All switches open
L	L	L	L	X-X0	X-X0, Y-Y0	X-X0, Y-Y0, Z-Z0
L	L	L	H	X-X1	X-X1, Y-Y1	X-X1, Y-Y0, Z-Z0
L	L	H	L	X-X2	X-X2, Y-Y2	X-X0, Y-Y1, Z-Z0
L	L	H	H	X-X3	X-X3, Y-Y3	X-X1, Y-Y1, Z-Z0
L	H	L	L	X-X4	X-X0, Y-Y0	X-X0, Y-Y0, Z-Z1
L	H	L	H	X-X5	X-X1, Y-Y1	X-X1, Y-Y0, Z-Z1
L	H	H	L	X-X6	X-X2, Y-Y2	X-X0, Y-Y1, Z-Z1
L	H	H	H	X-X7	X-X3, Y-Y3	X-X1, Y-Y1, Z-Z1

X = Don't care

\*C not present on MAX4582.

**Note:** Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

V<sub>CC</sub> and GND power the internal logic and logic-level translators, and set the input logic limits. The logic-level translators convert the logic levels into switched V<sub>CC</sub> and V<sub>EE</sub> signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies and signals and the analog supplies. V<sub>CC</sub> and V<sub>EE</sub> have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when V<sub>CC</sub> is +5V. As V<sub>CC</sub> rises, the threshold increases slightly, so when V<sub>CC</sub> reaches +12V the threshold is about 3.1V (above the TTL-guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs).

### Bipolar Supplies

These devices operate with bipolar supplies between ±2V and ±5V. The V<sub>CC</sub> and V<sub>EE</sub> supplies need not be symmetrical, but their sum cannot exceed the +13V absolute maximum rating

### Single Supply

These devices operate from a single supply between +2V and +12V when V<sub>EE</sub> is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually “work” with a single supply near or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

## Low-Voltage, CMOS Analog Multiplexers/Switches

### Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence  $V_{CC}$  on first, then  $V_{EE}$ , followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog-signal range to one diode drop below  $V_{CC}$  and one diode drop above  $V_{EE}$ , but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between  $V_{CC}$  and  $V_{EE}$  should not exceed 13V. These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

### High-Frequency Performance

In  $50\Omega$  systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks which are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -50dB in  $50\Omega$  systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also degrade off isolation. Adjacent channel attenuation is about 3dB above that of a bare IC socket and is entirely due to capacitive coupling.

### Pin Nomenclature

The MAX4581/MAX4582/MAX4583 are pin-compatible with the industry-standard 74HC4051/74HC4052/74HC4053 and the MAX4051/MAX4052/MAX4053. They function identically and have identical logic diagrams, although these parts differ electrically.

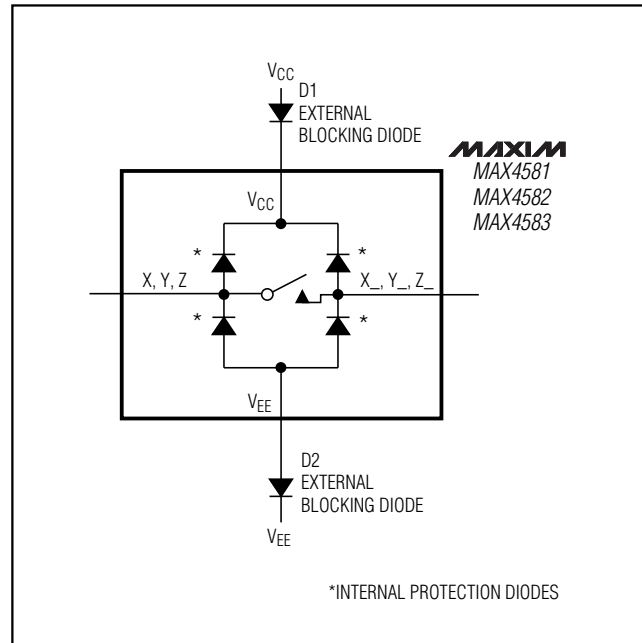


Figure 1. Overvoltage Protection Using External Blocking Diodes

The pin designations and logic diagrams in this data sheet conform to the original 1972 specifications published by RCA for the CD4051/CD4052/CD4053. These designations differ from the standard Maxim switch and mux designations as found all other Maxim data sheets (including the MAX4051/MAX4052/MAX4053) and may cause confusion. Designers who feel more comfortable with Maxim's standard designations are advised that the pin designations and logic diagrams on the MAX4051/MAX4052/MAX4053 data sheet may be freely applied to the MAX4581/MAX4582/MAX4583.

# Low-Voltage, CMOS Analog Multiplexers/Switches

## Test Circuits/Timing Diagrams

MAX4581/MAX4582/MAX4583

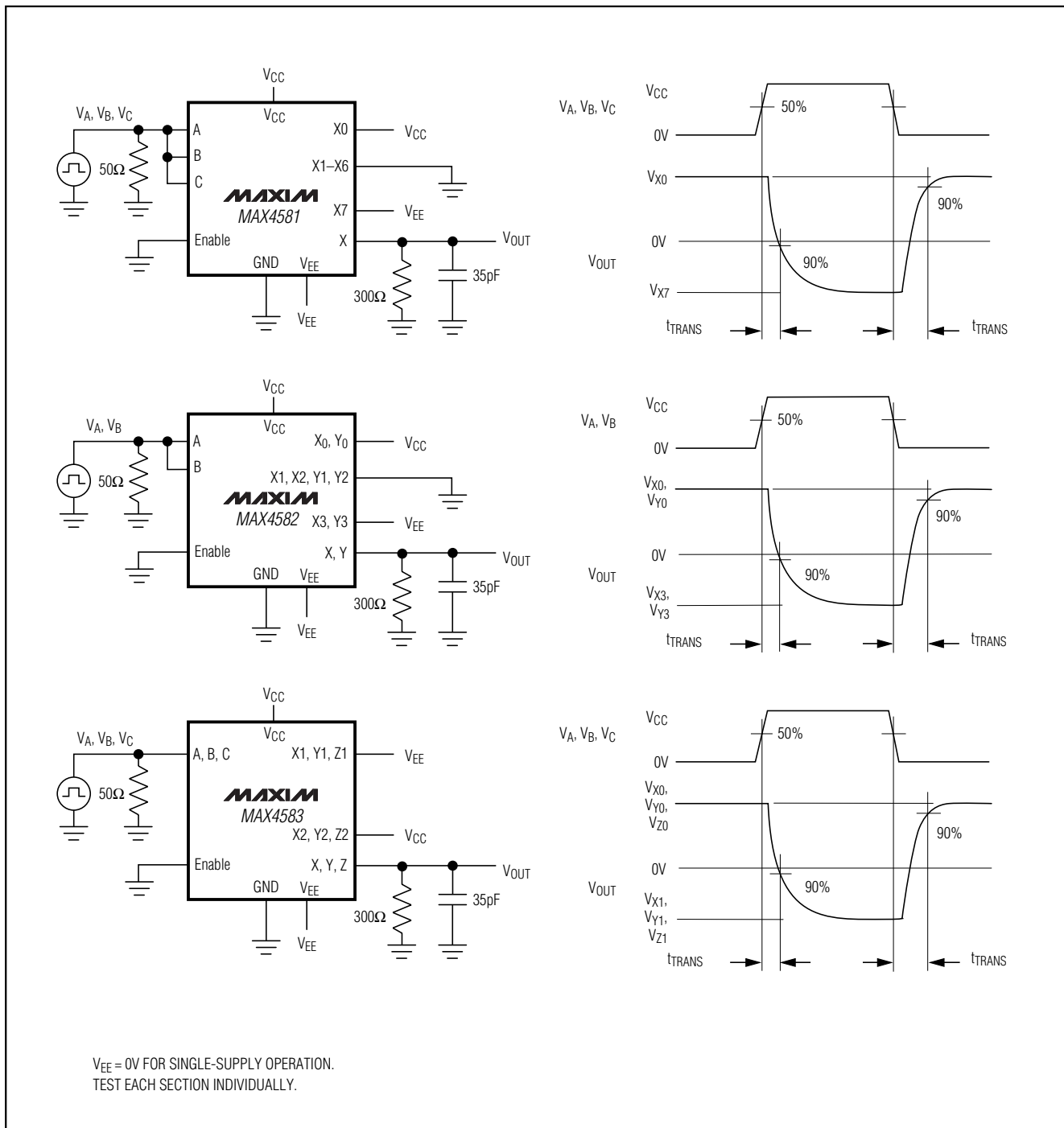
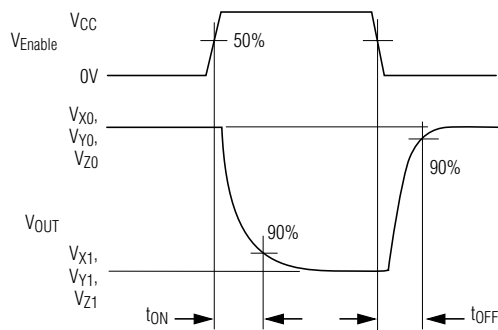
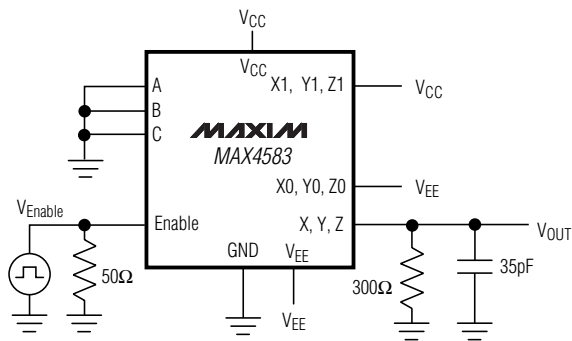
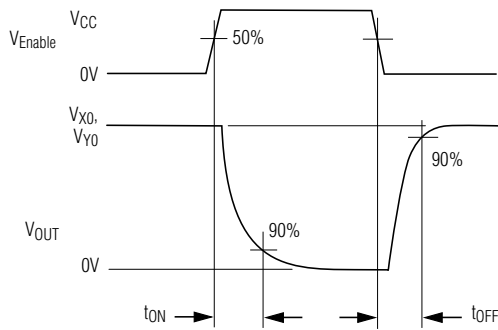
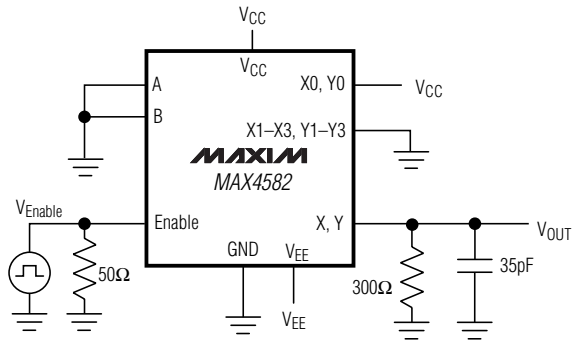
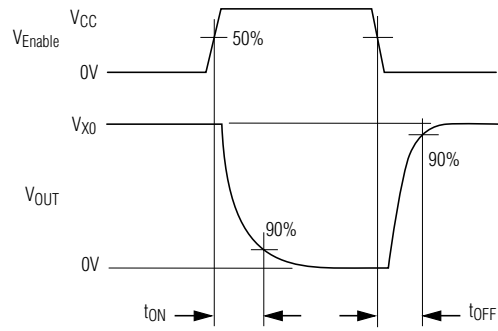
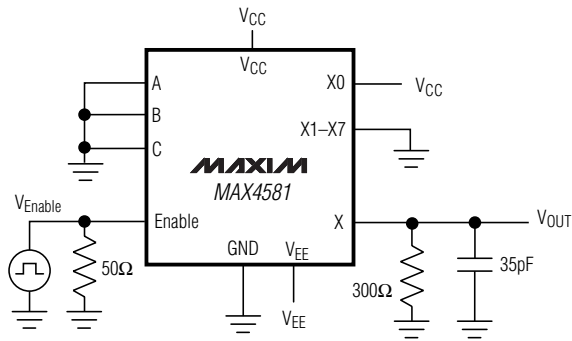


Figure 2. Address Transition Times

# Low-Voltage, CMOS Analog Multiplexers/Switches

## Test Circuits/Timing Diagrams (continued)



V<sub>EE</sub> = 0V FOR SINGLE-SUPPLY OPERATION.  
TEST EACH SECTION INDIVIDUALLY.

Figure 3. Inhibit Switching Times

# Low-Voltage, CMOS Analog Multiplexers/Switches

## Test Circuits/Timing Diagrams (continued)

MAX4581/MAX4582/MAX4583

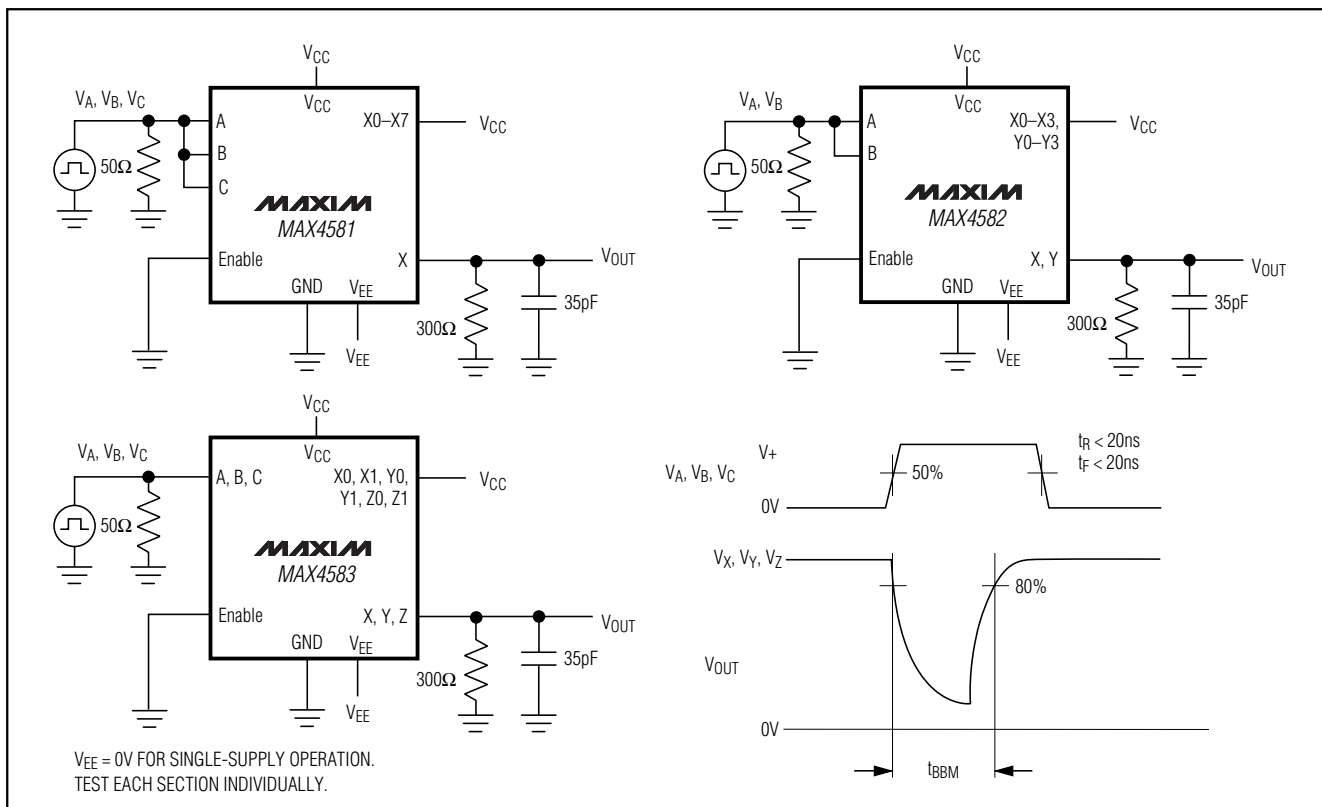


Figure 4. Break-Before-Make Interval

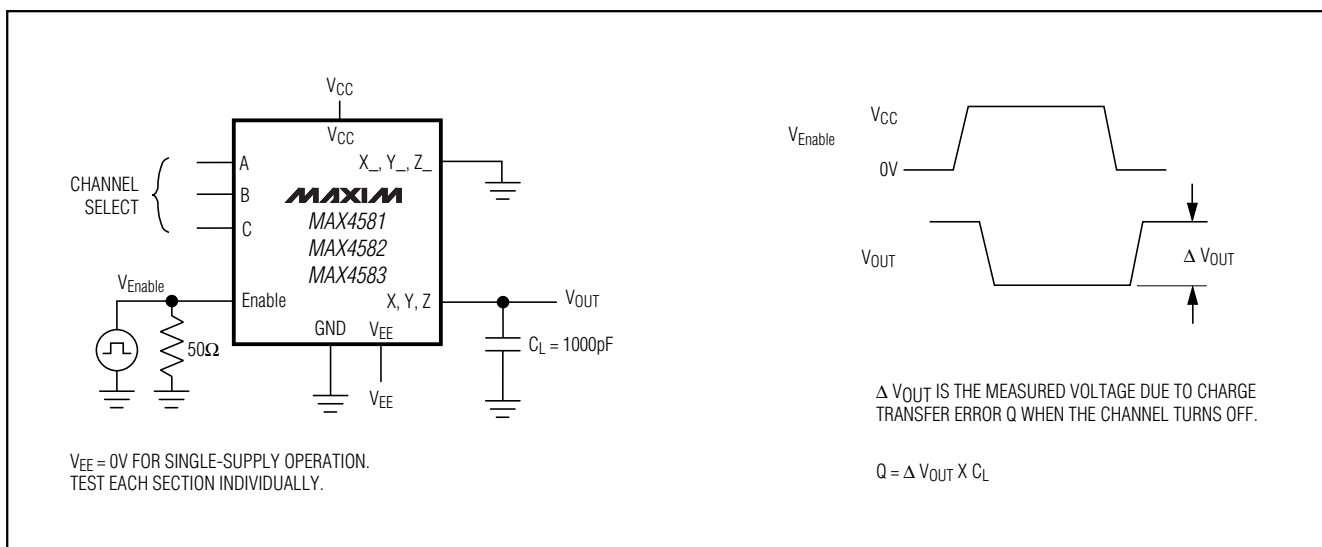


Figure 5. Charge Injection

# Low-Voltage, CMOS Analog Multiplexers/Switches

## Test Circuits/Timing Diagrams (continued)

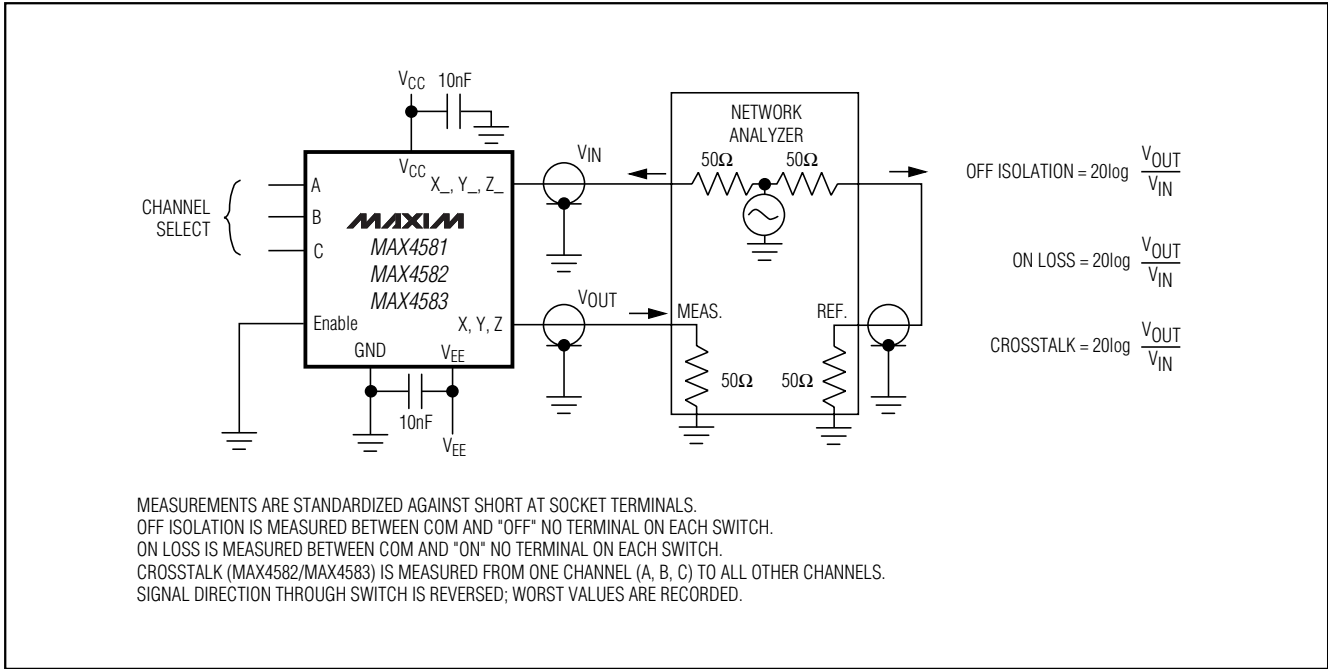


Figure 6. Off Isolation, On Loss, and Crosstalk

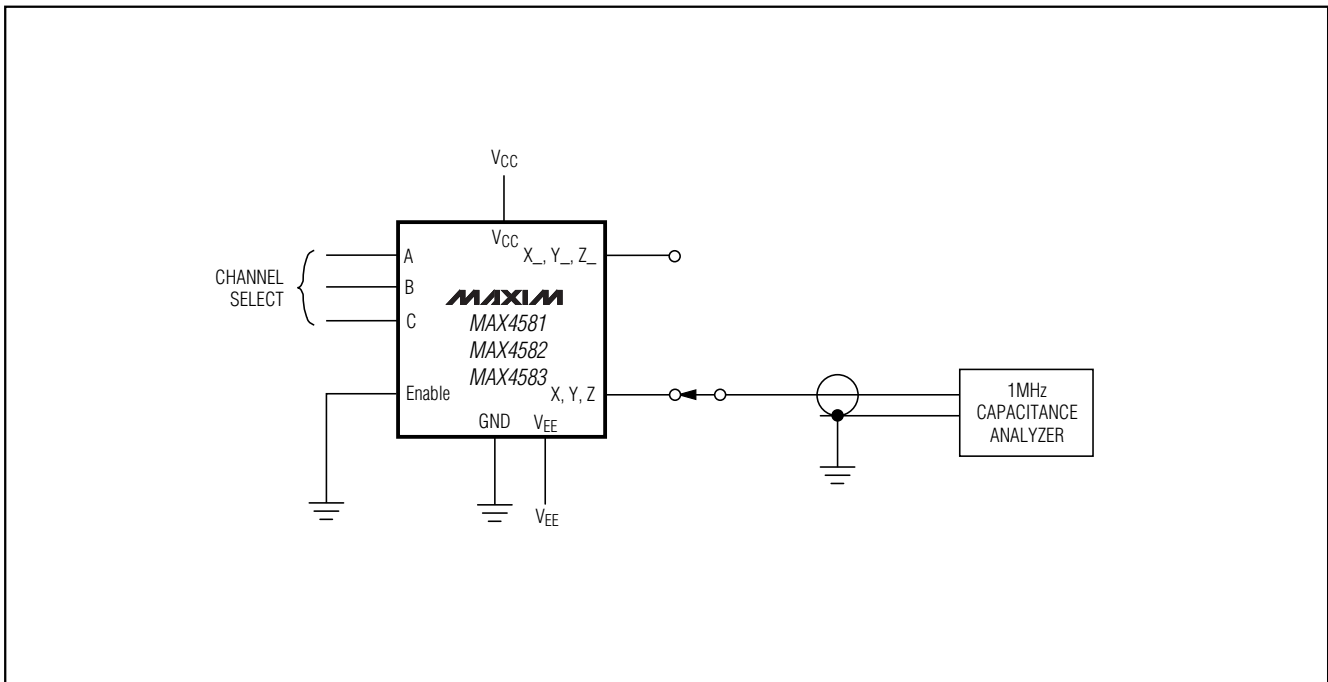


Figure 7. Capacitance

# Low-Voltage, CMOS Analog Multiplexers/Switches

MAX4581/MAX4582/MAX4583

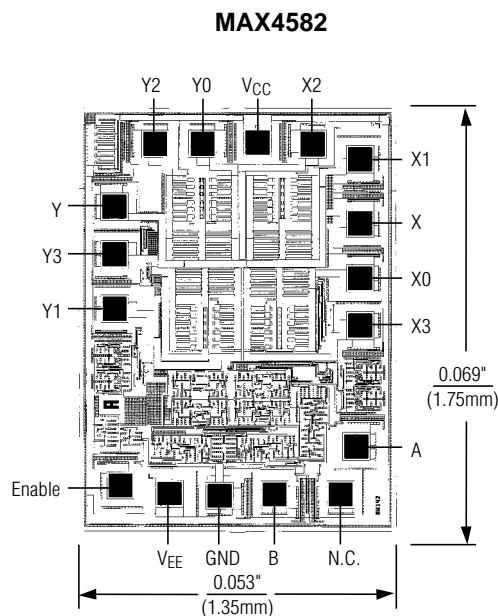
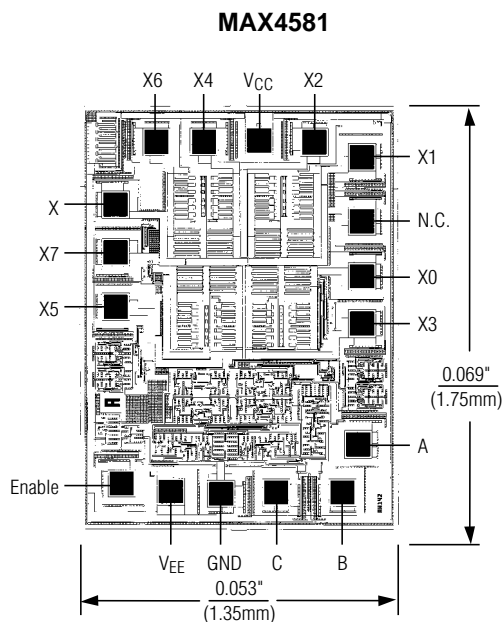
## Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4581CEE	0°C to +70°C	16 QSOP
MAX4581C/D	0°C to +70°C	Dice*
MAX4581EPE	-40°C to +85°C	16 Plastic DIP
MAX4581ESE	-40°C to +85°C	16 Narrow SO
MAX4581EUE	-40°C to +85°C	16 TSSOP
MAX4581EEE	-40°C to +85°C	16 QSOP
MAX4581ASE	-40°C to +125°C	16 Narrow SO
MAX4581AUE	-40°C to +125°C	16 TSSOP
<b>MAX4582</b> CPE	0°C to +70°C	16 Plastic DIP
MAX4582CSE	0°C to +70°C	16 Narrow SO
MAX4582CUE	0°C to +70°C	16 TSSOP
MAX4582CEE	0°C to +70°C	16 QSOP
MAX4582C/D	0°C to +70°C	Dice*
MAX4582EPE	-40°C to +85°C	16 Plastic DIP
MAX4582ESE	-40°C to +85°C	16 Narrow SO

PART	TEMP. RANGE	PIN-PACKAGE
MAX4582EUE	-40°C to +85°C	16 TSSOP
MAX4582EEE	-40°C to +85°C	16 QSOP
MAX4582ASE	-40°C to +125°C	16 Narrow SO
MAX4582AUE	-40°C to +125°C	16 TSSOP
<b>MAX4583</b> CPE	0°C to +70°C	16 Plastic DIP
MAX4583CSE	0°C to +70°C	16 Narrow SO
MAX4583CUE	0°C to +70°C	16 TSSOP
MAX4583CEE	0°C to +70°C	16 QSOP
MAX4583C/D	0°C to +70°C	Dice*
MAX4583EPE	-40°C to +85°C	16 Plastic DIP
MAX4583ESE	-40°C to +85°C	16 Narrow SO
MAX4583EUE	-40°C to +85°C	16 TSSOP
MAX4583EEE	-40°C to +85°C	16 QSOP
MAX4583ASE	-40°C to +125°C	16 Narrow SO
MAX4583AUE	-40°C to +125°C	16 TSSOP

\*Contact factory for availability.

## Chip Topographies



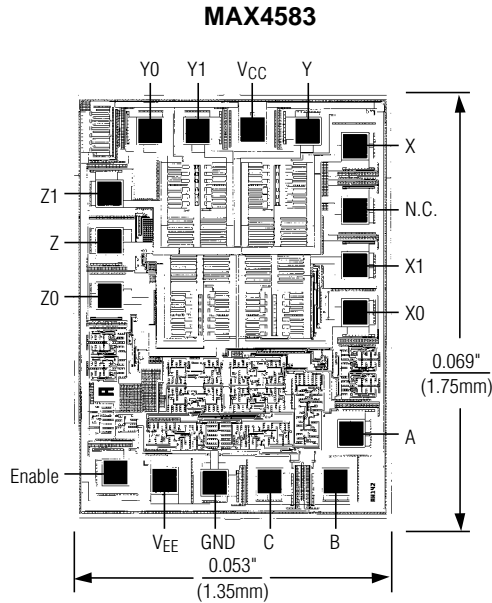
N.C. = NO CONNECTION

TRANSISTOR COUNT: 219  
SUBSTRATE CONNECTED TO V+.

TRANSISTOR COUNT: 219  
SUBSTRATE CONNECTED TO V+.

# Low-Voltage, CMOS Analog Multiplexers/Switches

## Chip Topographies (continued)



N.C. = NO CONNECTION

TRANSISTOR COUNT: 219

SUBSTRATE CONNECTED TO V+.

## Package Information

COMMON DIMENSIONS		MILLIMETERS		INCHES	
		MIN.	MAX.	MIN.	MAX.
A		1.10		0.43	
A1		0.05	0.15	0.02	0.06
A2		0.85	0.95	0.33	0.37
D		0.19	0.30	0.07	0.12
D1		0.19	0.25	0.07	0.10
C		0.090	0.20	0.035	0.08
C1		0.090	0.135	0.035	0.053
D SEE VARIATIONS SEE VARIATIONS					
E		4.30	4.50	1.69	1.77
F		0.65	0.85	0.26	0.33
H		6.25	6.50	2.46	2.56
L		0.50	0.70	0.20	0.28
N SEE VARIATIONS SEE VARIATIONS					
Y		2.85	3.15	1.12	1.24
Ø		0*	8*	0*	8*

JEDEC		VARIATIONS			
MD-153	N	MILLIMETERS		INCHES	
		MIN.	MAX.	MIN.	MAX.
AB	14 D	4.90	5.10	1.93	2.01
AC	16 D	4.90	5.10	1.93	2.01
AC-EP	16 D	4.90	5.10	1.93	2.01
AD	20 D	6.40	6.60	2.52	2.60
AD-EP	20 D	6.40	6.60	2.52	2.60
	X	4.00	4.34	1.57	1.71
AE	24 D	7.70	7.90	3.03	3.11
AF	28 D	9.60	9.80	3.78	3.86
AF-EP	D	9.60	9.80	3.78	3.86
	X	5.35	5.65	2.11	2.22

NOTES:  
 1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.  
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.  
 3. CONTROLLING DIMENSION: MILLIMETER.  
 4. MEETS JEDEC OUTLINE MD-153 VARIATIONS AB, AC, AD, AE, AF.  
 5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.  
 6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM  
 PROPRIETARY INFORMATION  
 TITLE: PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH  
 APPROVAL: [Signature] RECORD NUMBER: 21-0066 REV: C 1/1

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