

AM26LS32AC, AM26LS32AI, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS115D – OCTOBER 1980 – REVISED MARCH 2002

- **AM26LS32A Devices Meet or Exceed the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendations V.10 and V.11**
- **AM26LS32A Devices Have ± 7 -V Common-Mode Range With ± 200 -mV Sensitivity**
- **AM26LS33A Devices Have ± 15 -V Common-Mode Range With ± 500 -mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operate From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output-Enable Inputs**
- **Input Impedance . . . 12 k Ω Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32™ and AM26LS33™**

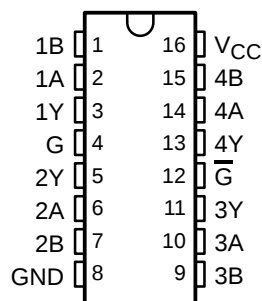
description

The AM26LS32A and AM26LS33A devices are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that, if the inputs are open, the outputs always are high.

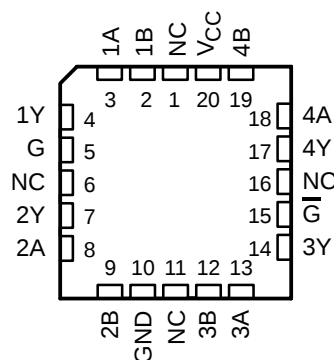
Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this does not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AI is characterized for operation from –40°C to 85°C. The AM26LS32AM and AM26LS33AM are characterized for operation over the full military temperature range of –55°C to 125°C.

AM26LS32AC . . . D, N, OR NS PACKAGE
AM26LS32AI, AM26LS33AC . . . D OR N PACKAGE
AM26LS32AM, AM26LS33AM . . . J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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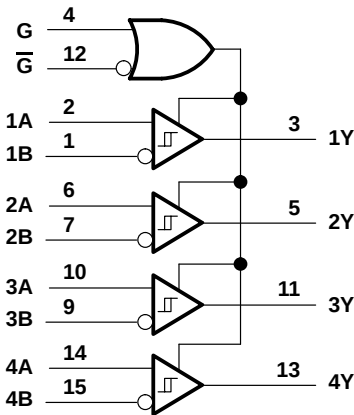
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FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

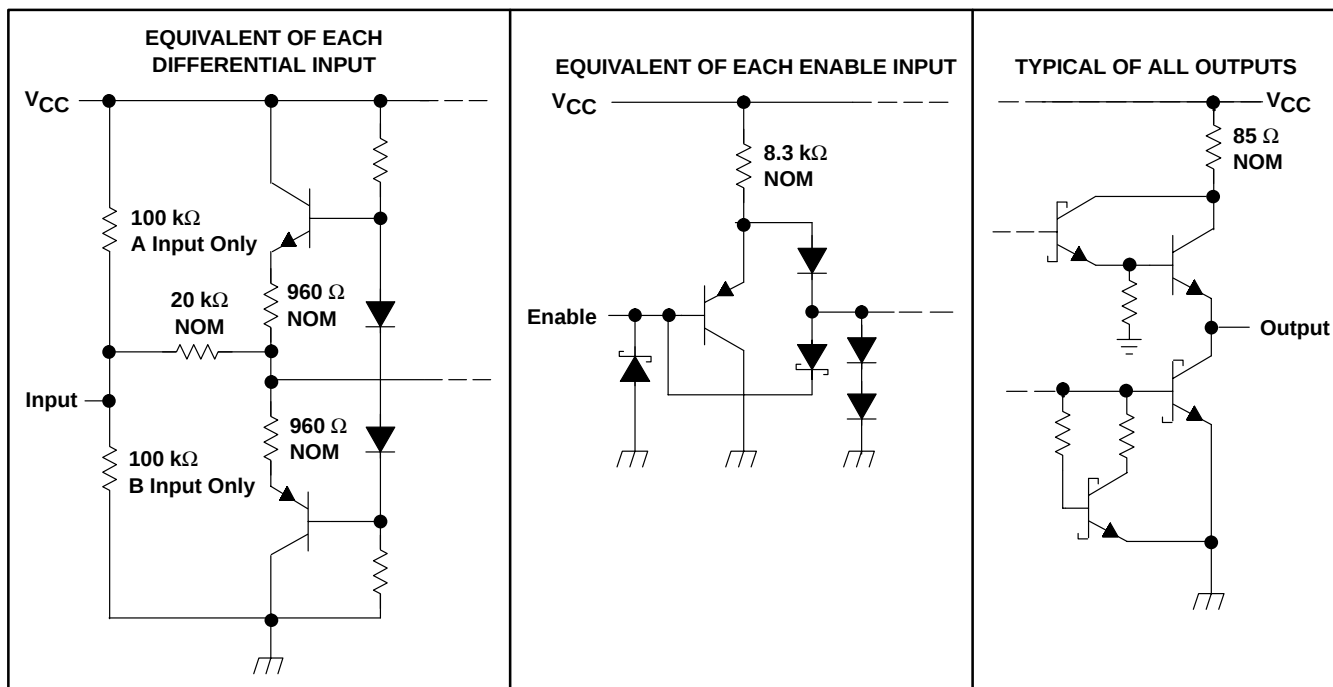
logic diagram (positive logic)



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I : Any differential input	± 25 V
Other inputs	7 V
Differential input voltage, V_{ID} (see Note 2)	± 25 V
Continuous total power dissipation	See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Storage temperature range, T_{Stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW

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recommended operating conditions

			MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage	AM26LS32AC, AM26LS32AI, AM26LS33AC	4.75	5	5.25	V	
		AM26LS32AM, AM26LS33AM	4.5	5	5.5		
V _{IH}	High-level input voltage		2			V	
V _{IL}	Low-level input voltage		0.8			V	
V _{IC}	Common-mode input voltage	AM26LS32A	±7			V	
		AM26LS33A	±15				
I _{OH}	High-level output current		−440			μA	
I _{OL}	Low-level output current		8			mA	
T _A	Operating free-air temperature	AM26LS32AC, AM26LS33AC	0			70	°C
		AM26LS32AI	−40			85	
		AM26LS32AM, AM26LS33AM	−55			125	

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = V _{OHmin} , I _{OH} = –440 μA	AM26LS32A		0.2	V
			AM26LS33A		0.5	
V _{IT–}	Negative-going input threshold voltage	V _O = 0.45 V, I _{OL} = 8 mA	AM26LS32A		–0.2 [‡]	V
			AM26LS33A		–0.5 [‡]	
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT–})			50		mV
V _{IK}	Enable-input clamp voltage	V _{CC} = MIN, I _I = –18 mA			–1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{ID} = 1 V, V _{I(G)} = 0.8 V, I _{OH} = –440 μA	AM26LS32AC AM26LS33AC		2.7	V
			AM26LS32AM, AM26LS32AI, AM26LS33AM		2.5	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{ID} = –1 V, V _{I(G)} = 0.8 V	I _{OL} = 4 mA		0.4	V
			I _{OL} = 8 mA		0.45	
I _{OZ}	Off-state (high-impedance state) output current	V _{CC} = MAX	V _O = 2.4 V		20	μA
			V _O = 0.4 V		–20	
I _I	Line input current	V _I = 15 V, Other input at –10 V to 15 V			1.2	mA
		V _I = –15 V, Other input at –15 V to 10 V			–1.7	
I _{I(EN)}	Enable input current	V _I = 5.5 V			100	μA
I _{IH}	High-level enable current	V _I = 2.7 V			20	μA
I _{IL}	Low-level enable current	V _I = 0.4 V			–0.36	mA
r _I	Input resistance	V _{IC} = –15 V to 15 V, One input to ac ground	12	15		kΩ
I _{OS}	Short-circuit output current [§]	V _{CC} = MAX	–15		–85	mA
I _{CC}	Supply current	V _{CC} = MAX, All outputs disabled		52	70	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

[‡] The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

[§] Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.



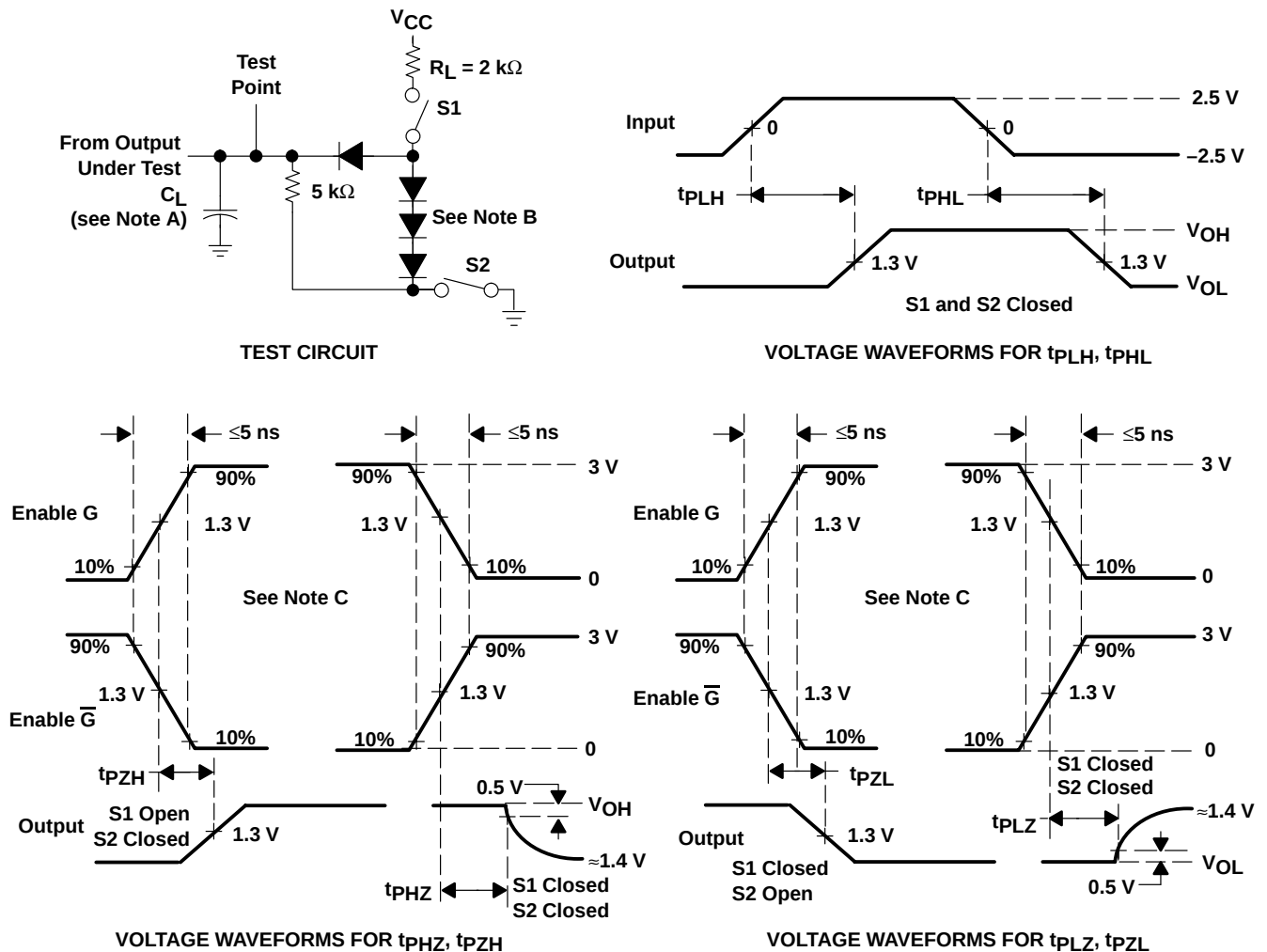
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}$, See Figure 1		20	35	ns
t_{PHL} Propagation delay time, high-to-low-level output			22	35	
t_{PZH} Output enable time to high level	$C_L = 15\text{ pF}$, See Figure 1		17	22	ns
t_{PZL} Output enable time to low level			20	25	
t_{PHZ} Output disable time from high level	$C_L = 5\text{ pF}$, See Figure 1		21	30	ns
t_{PLZ} Output disable time from low level			30	40	

PARAMETER MEASUREMENT INFORMATION



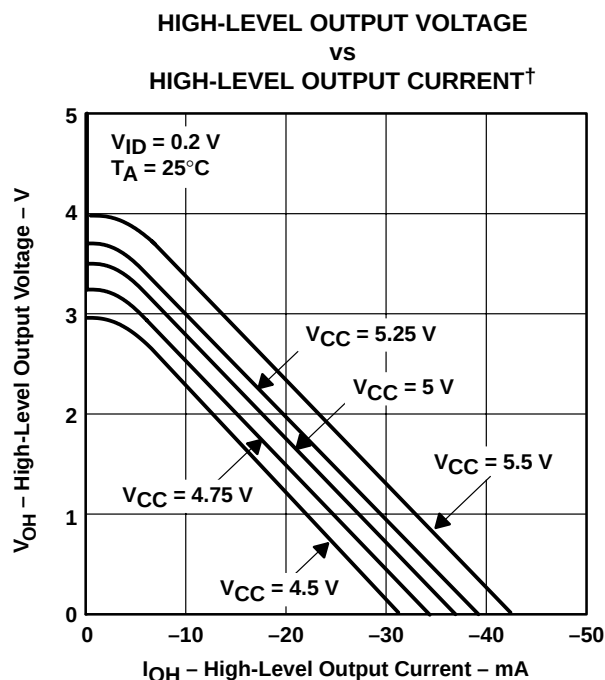
- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\bar{G}$ high; $\bar{G}$ is tested with G low.

Figure 1

AM26LS32AC, AM26LS32AI, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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TYPICAL CHARACTERISTICS



† $V_{CC} = 5.5 \text{ V}$ and $V_{CC} = 4.5 \text{ V}$ applies to M-suffix devices only.

Figure 2

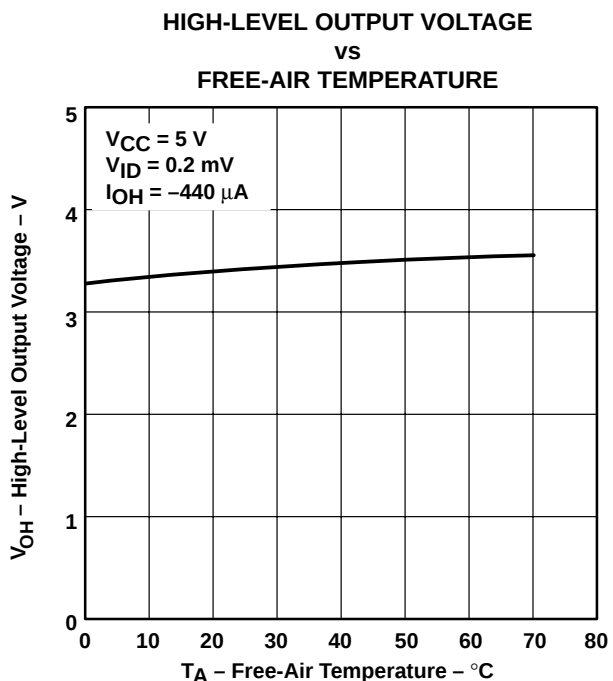


Figure 3

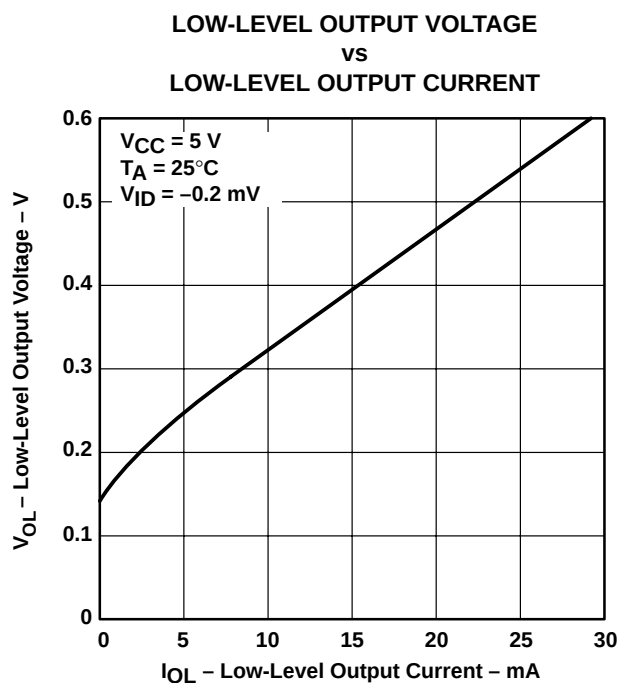


Figure 4

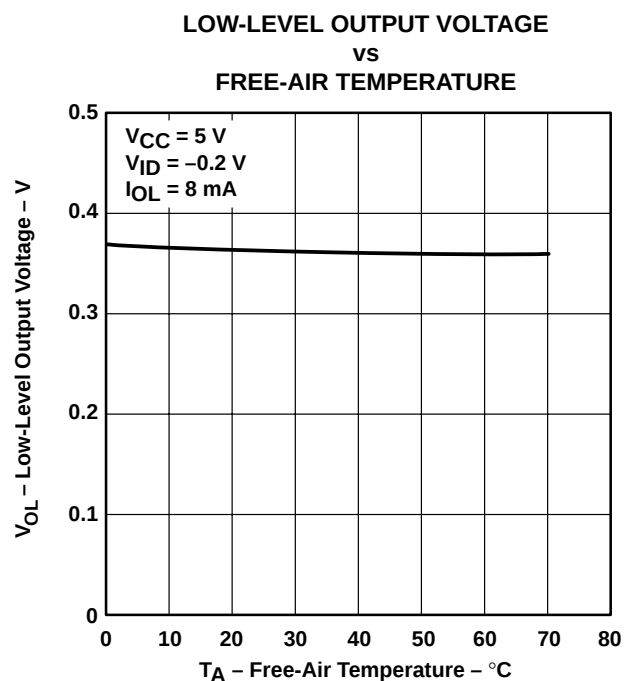


Figure 5

AM26LS32AC, AM26LS32AI, AM26LS33AC,
AM26LS32AM, AM26LS33AM
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TYPICAL CHARACTERISTICS

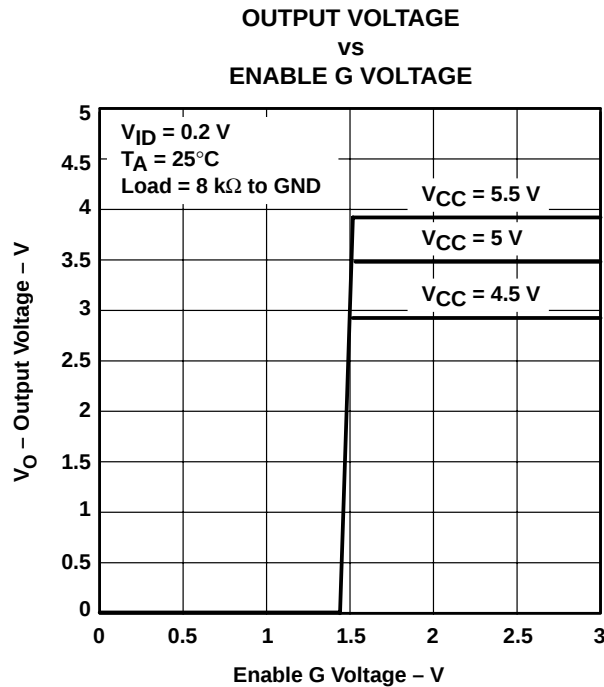


Figure 6

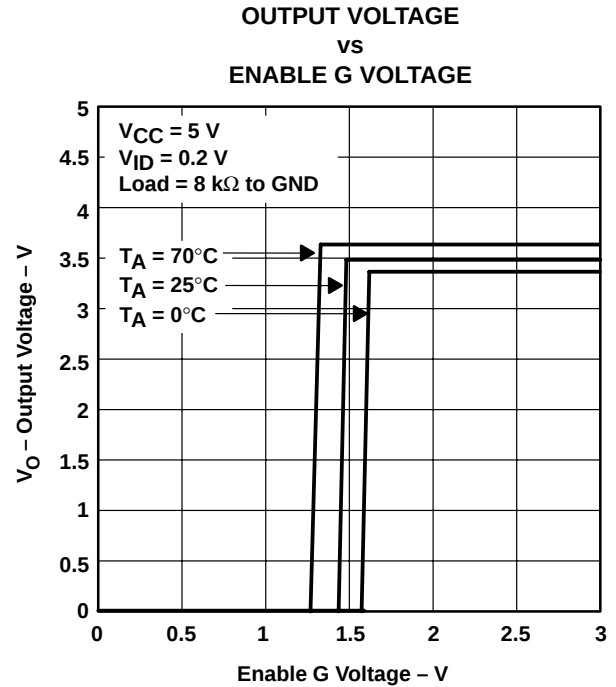


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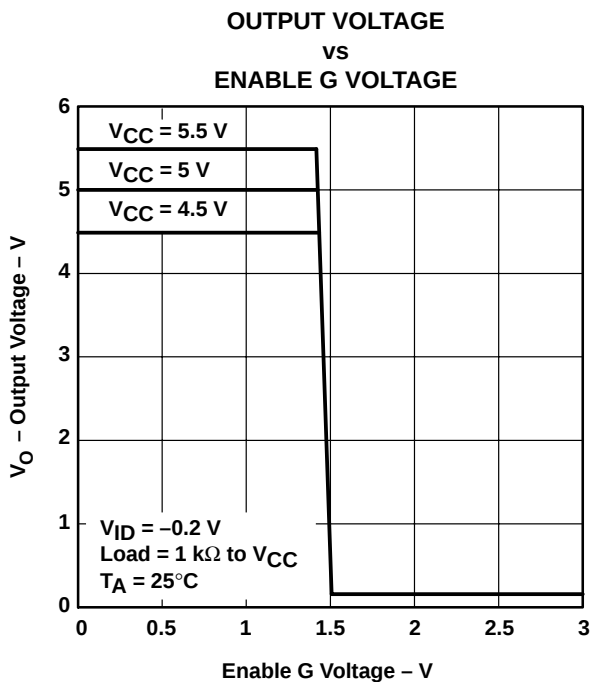


Figure 8

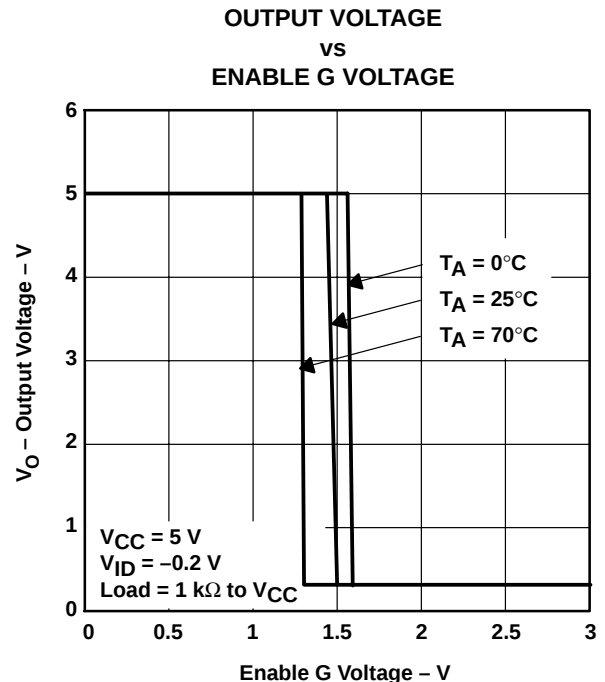


Figure 9

AM26LS32AC, AM26LS32AI, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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TYPICAL CHARACTERISTICS

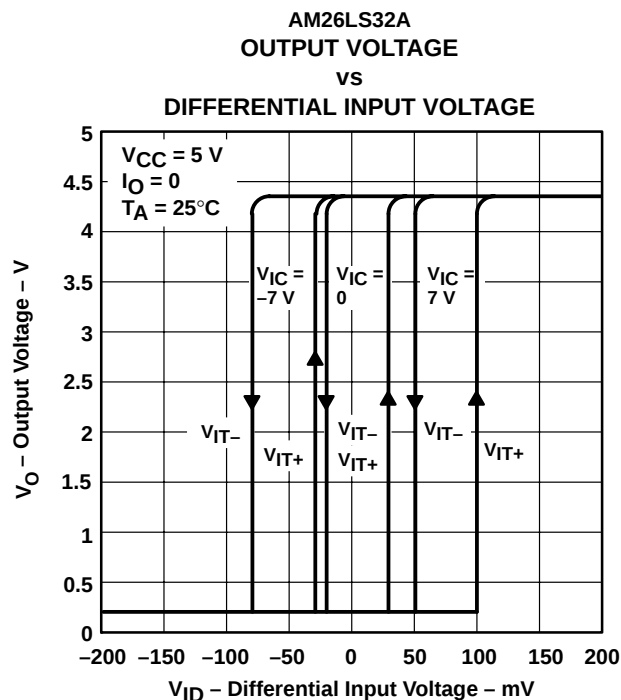


Figure 10

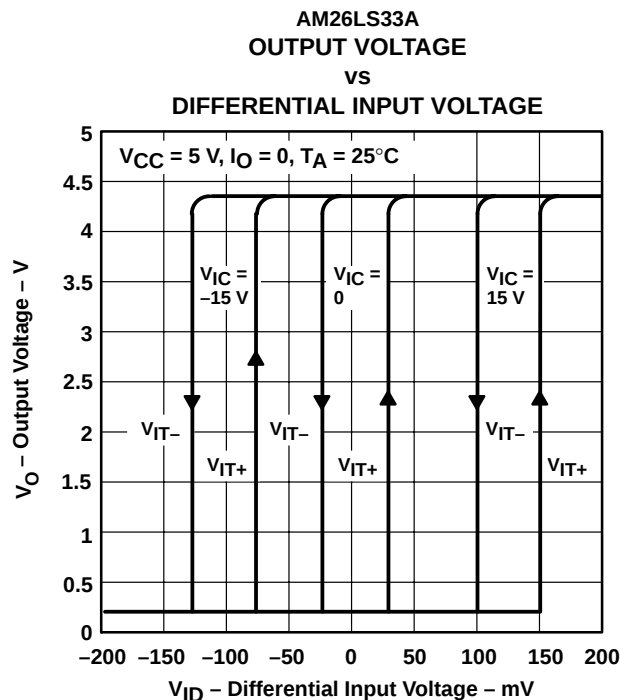


Figure 11

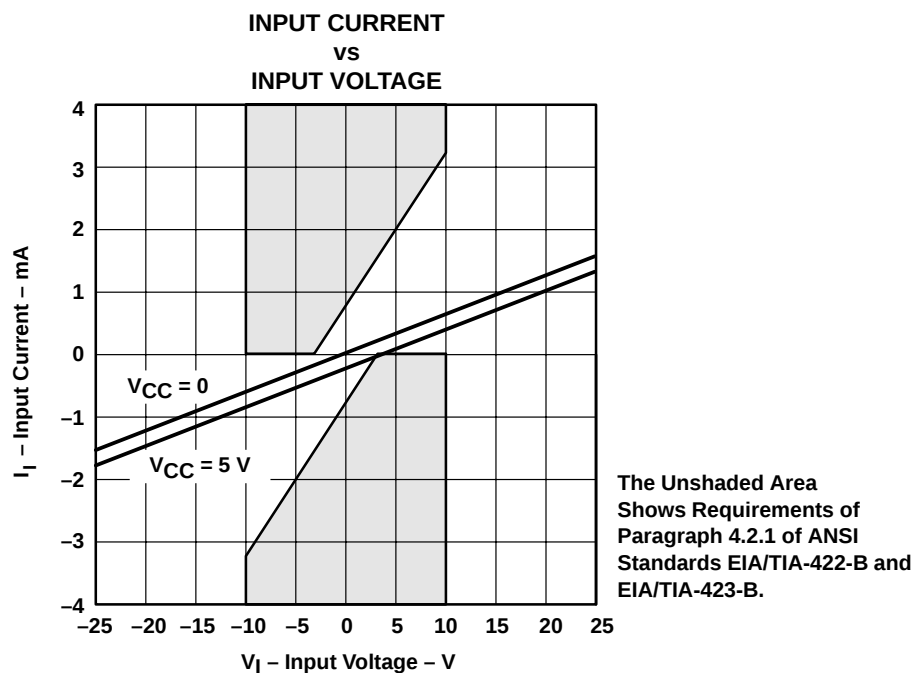
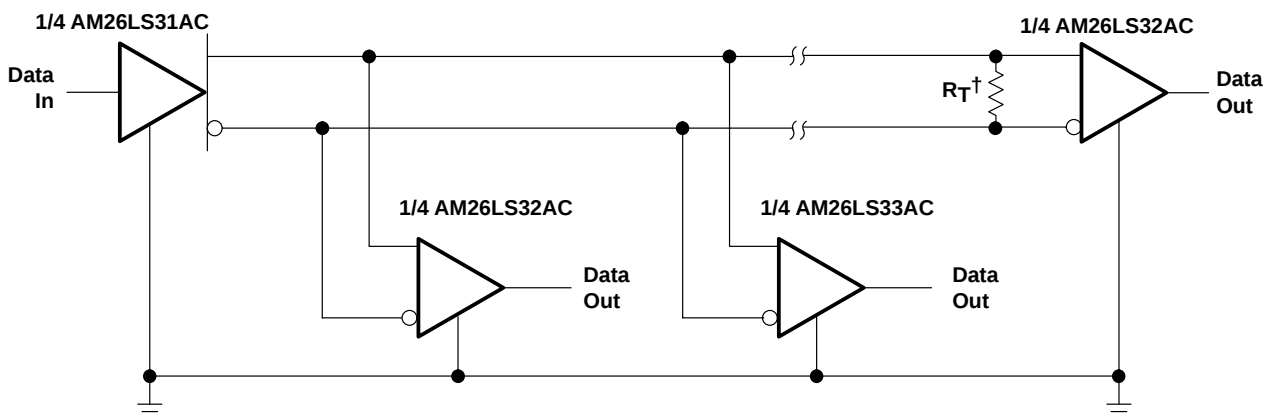


Figure 12

AM26LS32AC, AM26LS32AI, AM26LS33AC,
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APPLICATION INFORMATION



$^\dagger R_T$ equals the characteristic impedance of the line.

Figure 13. Circuit With Multiple Receivers

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