- **4.5-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 5.5 ns at 5 V**

SN54ALS11A, . . . J OR W PACKAGE
SN54AS11 . . . J PACKAGE
SN74ALS11A, SN74AS11 . . . D, N, OR NS PACKAGE
(TOP VIEW)

```
        ┌───┐
1A  [ 1   14 ]  V_CC
1B  [ 2   13 ]  1C
2A  [ 3   12 ]  1Y
2B  [ 4   11 ]  3C
2C  [ 5   10 ]  3B
2Y  [ 6    9 ]  3A
GND [ 7    8 ]  3Y
```
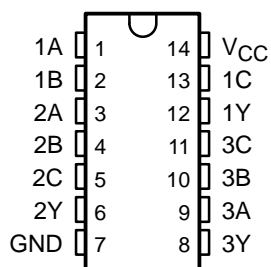
SN54ALS11A, SN54AS11 . . . FK PACKAGE
(TOP VIEW)

```
           1B  1A  NC  V_CC 1C
            3   2   1  20  19
        ┌─────────────────────┐
2A  [ 4                    18 ]  1Y
NC  [ 5                    17 ]  NC
2B  [ 6                    16 ]  3C
NC  [ 7                    15 ]  NC
2C  [ 8                    14 ]  3B
        └─────────────────────┘
            9  10  11  12  13
           2Y GND NC  3Y  3A
```
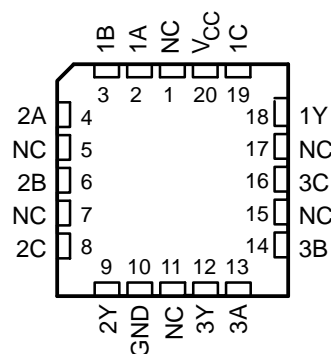
NC – No internal connection

description/ordering information

These devices contain three independent 3-input positive-AND gates. They perform the Boolean functions $Y = A \bullet B \bullet C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS11AN	SN74ALS11AN
			SN74AS11N	SN74AS11N
	SOIC – D	Tube	SN74ALS11AD	ALS11A
		Tape and reel	SN74ALS11ADR	
		Tube	SN74AS11D	AS11
		Tape and reel	SN74AS11DR	
	SOP – NS	Tape and reel	SN74ALS11ANSR	ALS11A
			SN74AS11NSR	74AS11
−55°C to 125°C	CDIP – J	Tube	SNJ54ALS11AJ	SNJ54ALS11AJ
			SNJ54AS11J	SNJ54AS11J
	CFP – W	Tube	SNJ54ALS11AW	SNJ54ALS11AW
	LCCC – FK	Tube	SNJ54ALS11AFK	SNJ54ALS11AFK
			SNJ54AS11FK	SNJ54AS11FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic diagram, each gate (positive logic)
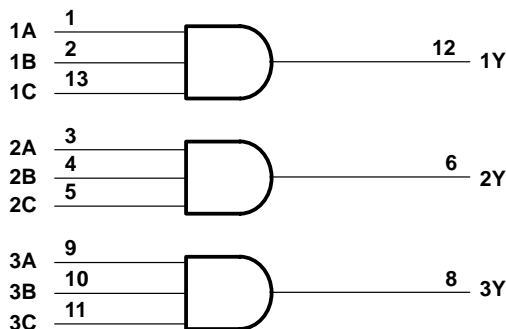
Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range (SN54ALS11A, SN74ALS11A) (unless otherwise noted)†

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Package thermal impedance, θ_{JA} (see Note 1): D package .... 86°C/W
 N package .... 80°C/W
 NS package .... 76°C/W
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		SN54ALS11A			SN74ALS11A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡			0.8	V
				0.7§				
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

‡ Applies over temperature range –55°C to 70°C
§ Applies over temperature range 70°C to 125°C
NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS11A			SN74ALS11A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0		1.6	3		1.6	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V TO 5.5 V, C_L = 50 PF, R_L = 500 Ω, T_A = MIN TO MAX§				UNIT
			SN54ALS11A		SN74ALS11A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	2	14	2	13	ns
t_{PHL}			2	12.5	2	10	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (SN54AS11, SN74AS11) (unless otherwise noted)¶

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Package thermal impedance, θ_{JA} (see Note 1): D package .... 86°C/W
　　　　　　　　　　　　　　　　　　　　　N package .... 80°C/W
　　　　　　　　　　　　　　　　　　　　　NS package .... 76°C/W
Storage temperature range .... −65°C to 150°C

¶ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		SN54AS11 MIN	NOM	MAX	SN74AS11 MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS11 MIN	TYP[†]	MAX	SN74AS11 MIN	TYP[†]	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O[‡]	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.3	7		4.3	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0		11.2	18		11.2	18	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V TO 5.5 V, C_L = 50 PF, R_L = 500 Ω, T_A = MIN TO MAX[§] SN54AS11 MIN	MAX	SN74AS11 MIN	MAX	UNIT
t_{PLH}	A, B, or C	Y	1	6.5	1	6	ns
t_{PHL}			1	6.5	1	5.5	

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

**LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**

**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PULSE DURATIONS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**
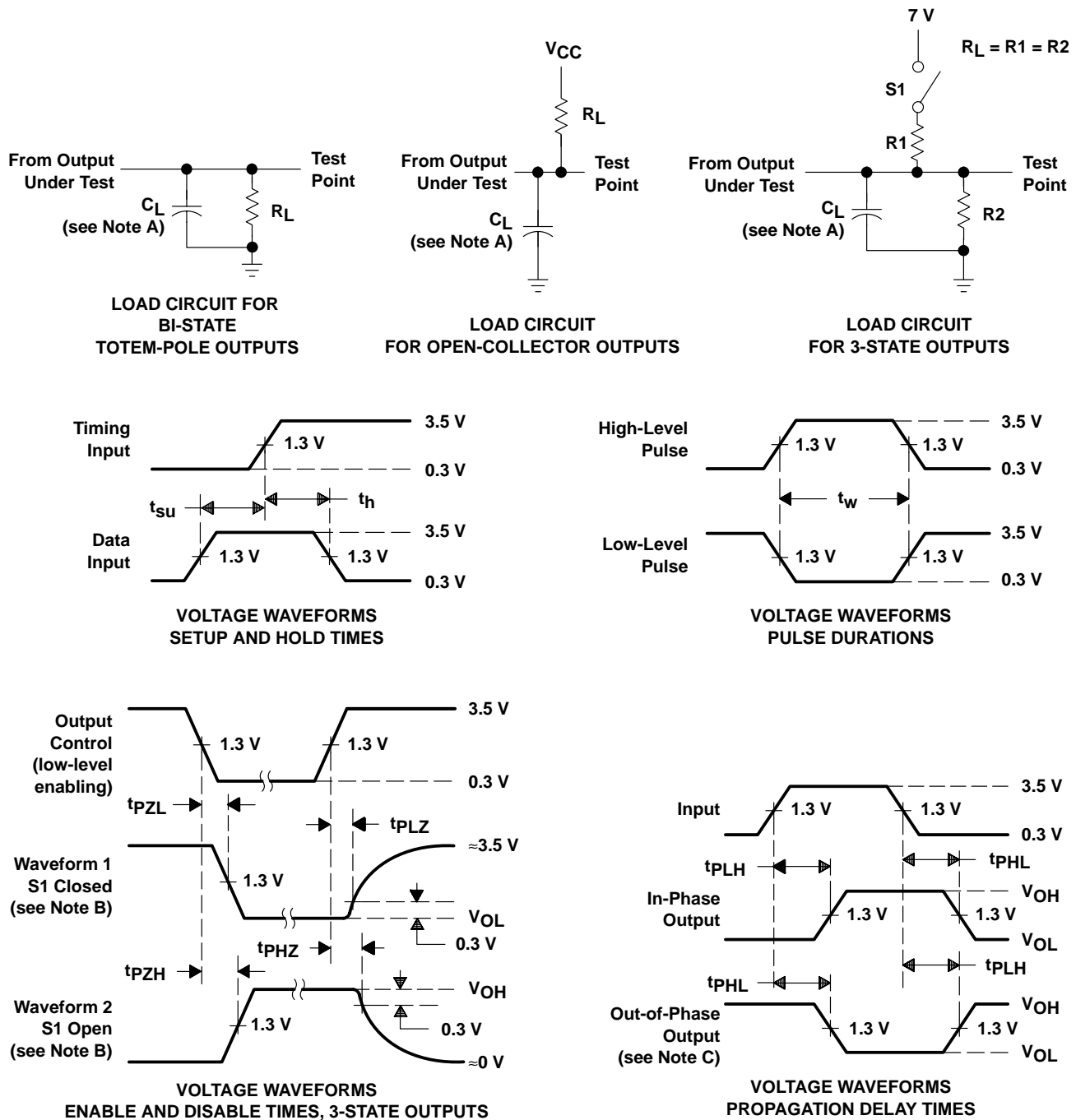
NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
   D. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
   E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-86841012A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8684101CA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
5962-8684101DA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
5962-9756101Q2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9756101QCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/37402B2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
JM38510/37402BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54ALS11AJ	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54AS11J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN74ALS11AD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS11ADR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS11AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS11ANSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AS11D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AS11DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AS11N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AS11NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54ALS11AFK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54ALS11AJ	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54ALS11AW	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SNJ54AS11FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54AS11J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

0.065 (1,65)
0.045 (1,14)

C

1   7

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R−GDFP−F14)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14) / 0.026 (0,66)

0.260 (6,60) / 0.235 (5,97)

0.080 (2,03) / 0.045 (1,14)

0.006 (0,15) / 0.004 (0,10)

0.280 (7,11) MAX

0.019 (0,48) / 0.015 (0,38)

1   14

0.050 (1,27)

0.390 (9,91) / 0.335 (8,51)

0.005 (0,13) MIN
4 Places

7   8

0.360 (9,14) / 0.250 (6,35)

0.360 (9,14) / 0.250 (6,35)

4040180−2/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within MIL STD 1835 GDFP1−F14 and JEDEC MO−092AB

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
           B. This drawing is subject to change without notice.
           C. This package can be hermetically sealed with a metal lid.
           D. The terminals are gold plated.
           E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

Gauge Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

0.430 (10,92) MAX

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
www.ti.com

D (R−PDSO−G14) PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14

8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F 07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
   D. Falls within JEDEC MS−012 variation AB.

NS (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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