

# SN54ACT373, SN74ACT373 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SCAS544E – OCTOBER 1995 – REVISED OCTOBER 2002

- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 10 ns at 5 V
- Inputs Are TTL-Voltage Compatible

## description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

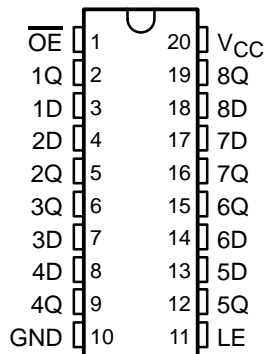
The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

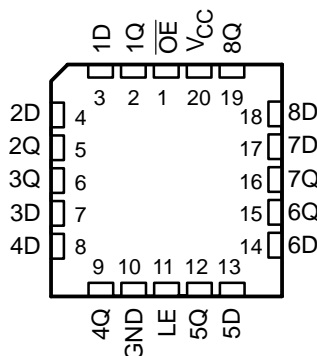
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ACT373 . . . J OR W PACKAGE  
SN74ACT373 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54ACT373 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ACT373N	SN74ACT373N
	SOIC – DW	Tube	SN74ACT373DW	ACT373
		Tape and reel	SN74ACT373DWR	
	SOP – NS	Tape and reel	SN74ACT373NSR	ACT373
	SSOP – DB	Tape and reel	SN74ACT373DBR	AD373
	TSSOP – PW	Tape and reel	SN74ACT373PWR	AD373
-55°C to 125°C	CDIP – J	Tube	SNJ54ACT373J	SNJ54ACT373J
	CFP – W	Tube	SNJ54ACT373W	SNJ54ACT373W
	LCCC – FK	Tube	SNJ54ACT373FK	SNJ54ACT373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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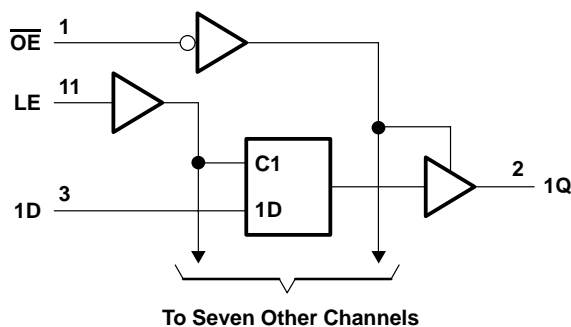
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**FUNCTION TABLE**  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
PW package .....	83°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions (see Note 3)

		SN54ACT373		SN74ACT373		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-24	mA
I <sub>OL</sub>	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate		8		8	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54ACT373		SN74ACT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.49	4.4		4.4		V	
		5.5 V	5.4	5.49	5.4		5.4			
	I <sub>OH</sub> = -24 mA	4.5 V	3.86		3.7		3.76			
		5.5 V	4.86		4.7		4.76			
	I <sub>OH</sub> = -50 mA†	5.5 V			3.85					
I <sub>OH</sub> = -75 mA†	5.5 V					3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		V	
		5.5 V			0.1		0.1			
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.44			
		5.5 V			0.36		0.44			
	I <sub>OL</sub> = 50 mA†	5.5 V				1.65				
I <sub>OL</sub> = 75 mA†	5.5 V					1.65				
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±5		μA	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80		μA	
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.6			1.5		mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5					pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		SN54ACT373		SN74ACT373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	7		8.5		8		ns
t <sub>su</sub>	Setup time, data before LE↓	7		8.5		8		ns
t <sub>h</sub>	Hold time, data after LE↓	0		1		1		ns



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**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

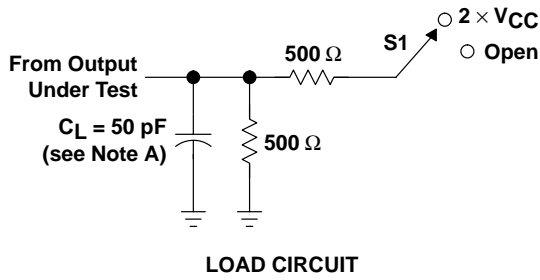
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54ACT373		SN74ACT373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Q	2.5	8.5	10	1.5	12.5	1.5	11.5	ns
t <sub>PHL</sub>			2	8	10	1.5	12.5	1.5	11.5	
t <sub>PLH</sub>	LE	Q	2.5	8.5	11	1.5	12.5	2	11.5	ns
t <sub>PHL</sub>			2	8	10	1.5	11.5	1.5	11.5	
t <sub>PZH</sub>	$\overline{OE}$	Q	2	8	9.5	1.5	11.5	1.5	10.5	ns
t <sub>PZL</sub>			2	7.5	9	1.5	11	1.5	10.5	
t <sub>PHZ</sub>	$\overline{OE}$	Q	2.5	9	11	1.5	14	2.5	12.5	ns
t <sub>PLZ</sub>			1.5	7.5	8.5	1.5	11	1	10	

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

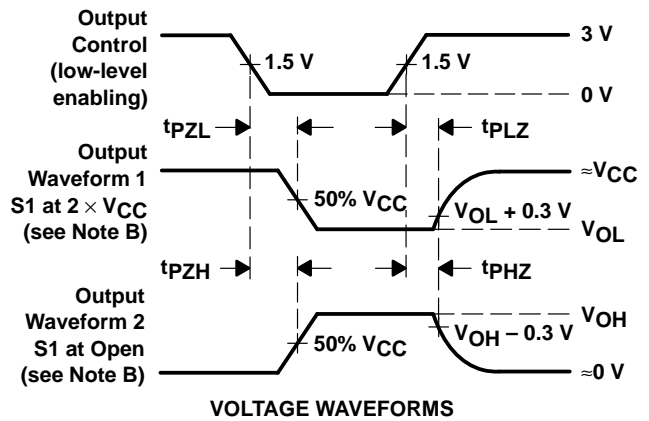
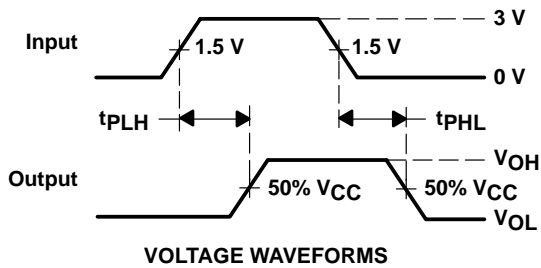
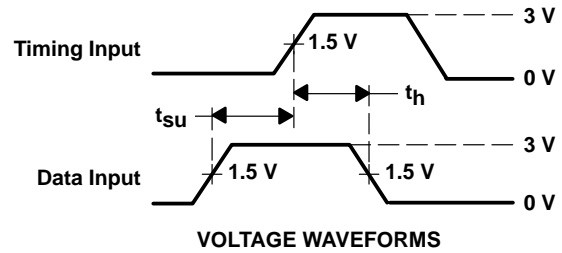
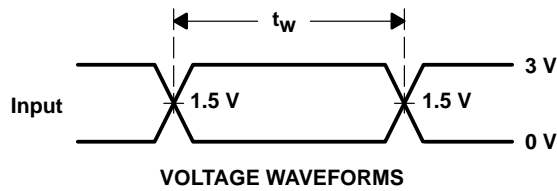
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 1 MHz	40	pF



PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-87556012A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-8755601RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8755601SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-8755601VRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8755601VSA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
SN74ACT373DBLE	OBSOLETE	SSOP	DB	20		None	Call TI	Call TI
SN74ACT373DBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT373DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT373DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ACT373NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74ACT373PW	ACTIVE	TSSOP	PW	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74ACT373PWLE	OBSOLETE	TSSOP	PW	20		None	Call TI	Call TI
SN74ACT373PWR	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SNJ54ACT373FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54ACT373J	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
SNJ54ACT373W	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

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<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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