

HIGH-SPEED PWM CONTROLLER

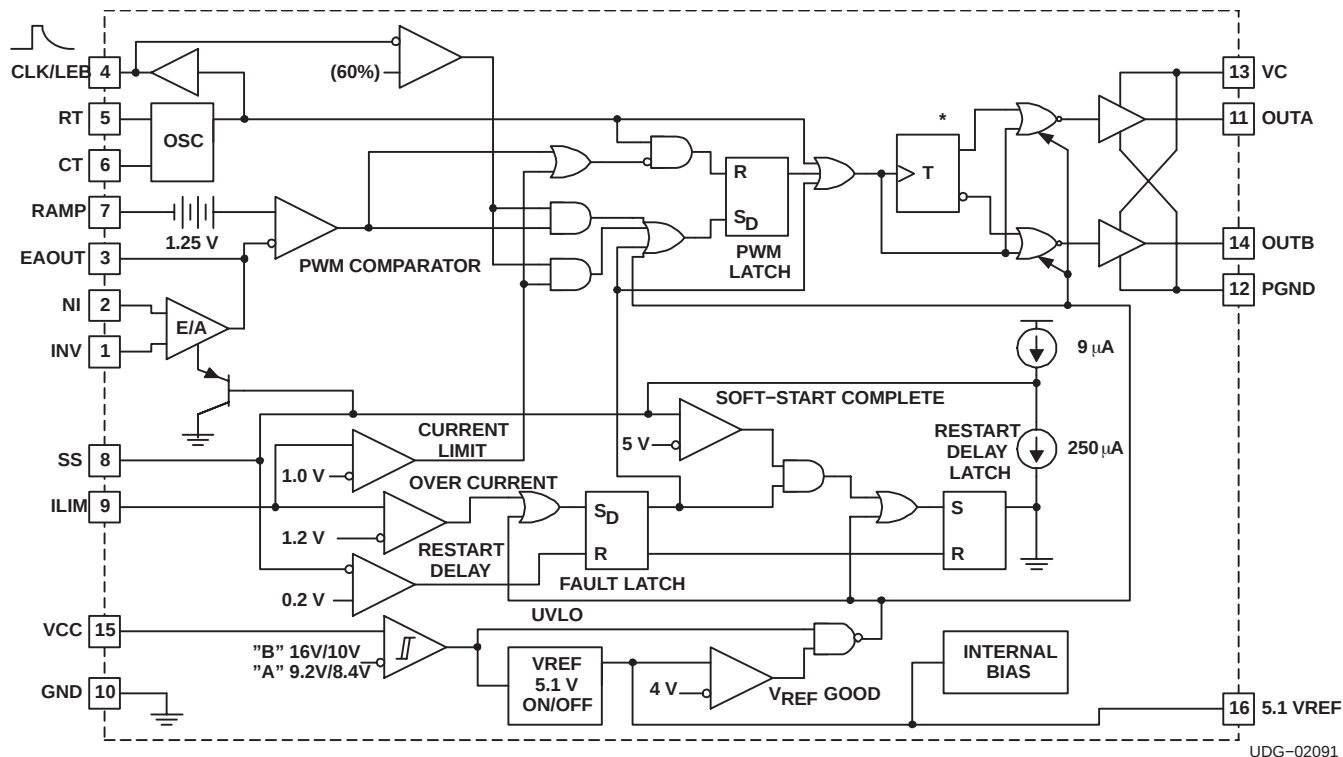
FEATURES

- Improved Versions of the UC3823/UC3825 PWMs
- Compatible with Voltage-Mode or Current-Mode Control Methods
- Practical Operation at Switching Frequencies to 1 MHz
- 50-ns Propagation Delay to Output
- High-Current Dual Totem Pole Outputs (2-A Peak)
- Trimmed Oscillator Discharge Current
- Low 100- μ A Startup Current
- Pulse-by-Pulse Current Limiting Comparator
- Latched Overcurrent Comparator With Full Cycle Restart

DESCRIPTION

The UC3823A and UC3823B and the UC3825A and UC3825B family of PWM controllers are improved versions of the standard UC3823 and UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset voltage is 2 mV. Current limit threshold is assured to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100 μ A, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2-A peak currents during transitions.

BLOCK DIAGRAM



* On the UC1823A version, toggles Q and $\bar{Q}$ are always low.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2 V. The overcurrent comparator sets a latch that ensures full discharge of the soft-start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft-start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 CLOCK pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC3825A and UC3825B have dual alternating outputs and the same pin configuration of the UC3825. The UC3823A and UC3823B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the UC3823A and UC3823B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. "A" version parts have UVLO thresholds identical to the original UC3823 and UC3825. The "B" versions have UVLO thresholds of 16 V and 10 V, intended for ease of use in off-line applications.

Consult the application note, *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers*, (SLUA125) for detailed technical and applications information.

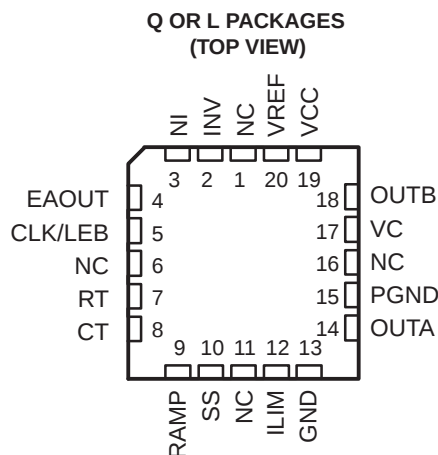
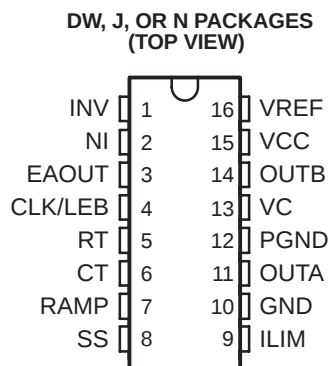
ORDERING INFORMATION

T _A	MAXIMUM DUTY CYCLE	UVLO					
		9.2 V / 8.4 V			16 V / 10 V		
		SOIC-16 ⁽¹⁾ (DW)	PDIP-16 (N)	PLCC-20 ⁽¹⁾ (Q)	SOIC-16 (DW)	PDIP-16 (N)	PLCC-20 ⁽¹⁾ (Q)
-40°C to 85°C	< 100%	UC2823ADW	UC2823AN	UC2823AQ	UC2823BDW	UC2823BN	–
	< 50%	UC2825ADW	UC2825AN	UC2825AQ	UC2825BDW	UC2825BN	–
-0°C to 70°C	< 100%	UC3823ADW	UC3823AN	UC3823AQ	UC3823BDW	UC3823BN	–
	< 50%	UC3825ADW	UC3825AN	UC3825AQ	UC3825BDW	UC3825BN	UC3825BQ

(1) The DW and Q packages are also available taped and reeled. Add TR suffix to the device type (i.e., UC2823ADWR). To order quantities of 1000 devices per reel for the Q package and 2000 devices per reel for the DW package.

T _A	MAXIMUM DUTY CYCLE	UVLO	
		9.2 V / 8.4 V	
		CDIP-16 (J)	LCCC-20 (L)
-55°C to 125°C	< 100%	UC1823AJ, UC1823AJ883B, UC1823AJQMLV	UC1823AL, UC1823AL883B
	< 50%	UC1825AJ, UC1825AJ883B, UC1825AJQMLV	UC1825AL, UC1825AL883B, UC1825ALQMLV

PIN ASSIGNMENTS



NC = no connection

TERMINAL FUNCTIONS

NAME	TERMINAL NO.		I/O	DESCRIPTION
	J or DW	Q or L		
CLK/LEB	4	5	O	Output of the internal oscillator
CT	6	8	I	Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.
EAOUT	3	4	O	Output of the error amplifier for compensation
GND	10	13	–	Analog ground return pin
ILIM	9	12	I	Input to the current limit comparator
INV	1	2	I	Inverting input to the error amplifier
NI	2	3	I	Non-inverting input to the error amplifier
OUTA	11	14	O	High current totem pole output A of the on-chip drive stage.
OUTB	14	18	O	High current totem pole output B of the on-chip drive stage.
PGND	12	15	–	Ground return pin for the output driver stage
RAMP	7	9	I	Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input.
RT	5	7	I	Timing resistor connection pin for oscillator frequency programming
SS	8	10	I	Soft-start input pin which also doubles as the maximum duty cycle clamp.
VC	13	17	–	Power supply pin for the output stage. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths.
VCC	15	19	–	Power supply pin for the device. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths
VREF	16	20	O	5.1-V reference. For stability, the reference should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

			UNIT
V _{IN}	Supply voltage,	VC, VCC	22 V
I _O	Source or sink current, DC	OUTA, OUTB	0.5 A
I _O	Source or sink current, pulse (0.5 μs)	OUTA, OUTB	2.2 A
Analog inputs		INV, NI, RAMP	–0.3 V to 7 V
		ILIM, SS	–0.3 V to 6 V
Power ground		PGND	±0.2 V
I _{CLK}	Clock output current	CLK/LEB	–5 mA
I _{O(EA)}	Error amplifier output current	EAOUT	5 mA
I _{SS}	Soft-start sink current	SS	20 mA
I _{OSC}	Oscillator charging current	RT	–5 mA
T _J	Operating virtual junction temperature range		–55°C to 150°C
T _{Stg}	Storage temperature		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		–55°C to 150°C
t _{STG}	Storage temperature		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds		300°C

⁽¹⁾ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_A = -55^{\circ}\text{C}$ to 125°C for the UC1823A/UC1825A, $T_A = -40^{\circ}\text{C}$ to 85°C for the UC2823x/UC2825x, $T_A = 0^{\circ}\text{C}$ to 70°C for the UC3823x/UC3825x, $R_T = 3.65\text{ k}\Omega$, $C_T = 1\text{ nF}$, $V_{CC} = 12\text{ V}$, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE, V_{REF}						
V_O	Output voltage range	$T_J = 25^{\circ}\text{C}$, $I_O = 1\text{ mA}$	5.05	5.1	5.15	V
	Line regulation	$12\text{ V} \leq V_{CC} \leq 20\text{ V}$		2	15	mV
	Load regulation	$1\text{ mA} \leq I_O \leq 10\text{ mA}$		5	20	
	Total output variation	Line, load, temperature	5.03		5.17	V
	Temperature stability ⁽¹⁾	$T_{(\min)} < T_A < T_{(\max)}$		0.2	0.4	mV/ $^{\circ}\text{C}$
	Output noise voltage ⁽¹⁾	$10\text{ Hz} < f < 10\text{ kHz}$		50		μVRMS
	Long term stability ⁽¹⁾	$T_J = 125^{\circ}\text{C}$, 1000 hours		5	25	mV
	Short circuit current	$V_{REF} = 0\text{ V}$	30	60	90	mA
OSCILLATOR						
f_{OSC}	Initial accuracy ⁽¹⁾	$T_J = 25^{\circ}\text{C}$	375	400	425	kHz
		$R_T = 6.6\text{ k}\Omega$, $C_T = 220\text{ pF}$, $T_A = 25^{\circ}\text{C}$	0.9	1	1.1	MHz
	Total variation ⁽¹⁾	Line, temperature	350		450	kHz
		$R_T = 6.6\text{ k}\Omega$, $C_T = 220\text{ pF}$	0.85		1.15	MHz
	Voltage stability	$12\text{ V} < V_{CC} < 20\text{ V}$			1%	
	Temperature stability ⁽¹⁾	$T_{(\min)} < T_A < T_{(\max)}$		5%		
	High-level output voltage, clock		3.7	4		V
	Low-level output voltage, clock			0	0.2	
	Ramp peak		2.6	2.8	3	
	Ramp valley		0.7	1	1.25	
	Ramp valley-to-peak		1.6	1.8	2	
I_{OSC}	Oscillator discharge current	$R_T = \text{OPEN}$, $V_{CT} = 2\text{ V}$	9	10	11	mA
ERROR AMPLIFIER						
	Input offset voltage			2	10	mV
	Input bias current			0.6	3	μA
	Input offset current			0.1	1	
	Open loop gain	$1\text{ V} < V_O < 4\text{ V}$	60	95		dB
CMRR	Common mode rejection ratio	$1.5\text{ V} < V_{CM} < 5.5\text{ V}$	75	95		
PSRR	Power supply rejection ratio	$12\text{ V} < V_{CC} < 20\text{ V}$	85	110		
$I_{O(\text{sink})}$	Output sink current	$V_{EAOUT} = 1\text{ V}$	1	2.5		mA
$I_{O(\text{src})}$	Output source current	$V_{EAOUT} = 4\text{ V}$	-0.5	-1.3		
	High-level output voltage	$I_{EAOUT} = -0.5\text{ mA}$	4.5	4.7	5	V
	Low-level output voltage	$I_{EAOUT} = -1\text{ mA}$	0	0.5	1	
	Gain bandwidth product	$f = 200\text{ kHz}$	6	12		Mhz
	Slew rate ⁽¹⁾		6	9		V/ μs

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS

$T_A = -55^{\circ}\text{C}$ to 125°C for the UC1823A/UC1825A, $T_A = -40^{\circ}\text{C}$ to 85°C for the UC2823x/UC2825x, $T_A = 0^{\circ}\text{C}$ to 70°C for the UC3823x/UC3825x, $R_T = 3.65\text{ k}\Omega$, $C_T = 1\text{ nF}$, $V_{CC} = 12\text{ V}$, $T_A = T_J$ (unless otherwise noted)

PWM COMPARATOR						
I _{BIAS}	Bias current, RAMP	V _{RAMP} = 0 V	-1	-8		μA
	Minimum duty cycle			0%		
	Maximum duty cycle		85%			
t _{LEB}	Leading edge blanking time	R _{LEB} = 2 kΩ, C _{LEB} = 470 pF	300	375	450	ns
R _{LEB}	Leading edge blanking resistance	V _{CLK/LEB} = 3 V	8.5	10.0	11.5	kΩ
V _{ZDC}	Zero dc threshold voltage, EAOUT	V _{RAMP} = 0 V	1.10	1.25	1.4	V
t _{DELAY}	Delay-to-output time	V _{EAOUT} = 2.1 V, V _{ILIM} = 0 V to 2 V step	50	80		ns
CURRENT LIMIT / START SEQUENCE / FAULT						
I _{SS}	Soft-start charge current	V _{SS} = 2.5 V	8	14	20	μA
V _{SS}	Full soft-start threshold voltage		4.3	5		V
I _{DSCH}	Restart discharge current	V _{SS} = 2.5 V	100	250	350	μA
I _{SS}	Restart threshold voltage		0.3	0.5		V
I _{BIAS}	ILIM bias current	V _{ILIM} = 0 V to 2 V step			15	μA
I _{CL}	Current limit threshold voltage		0.95	1	1.05	V
	Overcurrent threshold voltage		1.14	1.2	1.26	
t _d	Delay-to-output time, ILIM ⁽¹⁾	V _{ILIM} = 0 V to 2 V step	50	80		ns
OUTPUT						
	Low-level output saturation voltage	I _{OUT} = 20 mA	0.25	0.4		V
		I _{OUT} = 200 mA	1.2	2.2		
	High-level output saturation voltage	I _{OUT} = 20 mA	1.9	2.9		
		I _{OUT} = 200 mA	2	3		
t _r , t _f	Rise/fall time ⁽¹⁾	C _L = 1 nF	20	45		ns
UNDERVOLTAGE LOCKOUT (UVLO)						
Start threshold voltage		UC2823B, UC2825B, UC3825B, UC3825B	16	17		V
		UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A	8.4	9.2	9.6	
Stop threshold voltage		UC2823B, UC2825B, UC3825B, UC3825B	9	10		
OVLO hysteresis		UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A	0.4	0.8	1.2	
		UC2823B, UC2825B, UC3825B, UC3825B	5	6	7	
SUPPLY CURRENT						
I _{su}	Startup current	V _C = V _{CC} = V _{TH} = -0.5 V	100	300		μA
I _{CC}	Input current		28	36		mA

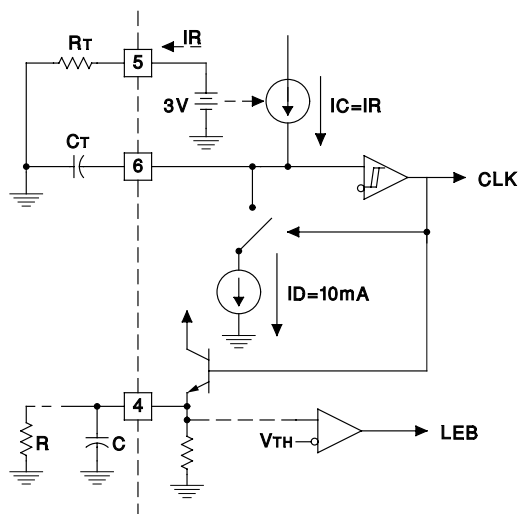
(1) Ensured by design. Not production tested.

APPLICATION INFORMATION

The oscillator of the UC3823A, UC3823B, UC3825A, and UC3825B is a saw tooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin (C_{CT}). The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency (RT) and D_{MAX} . The design equations are:

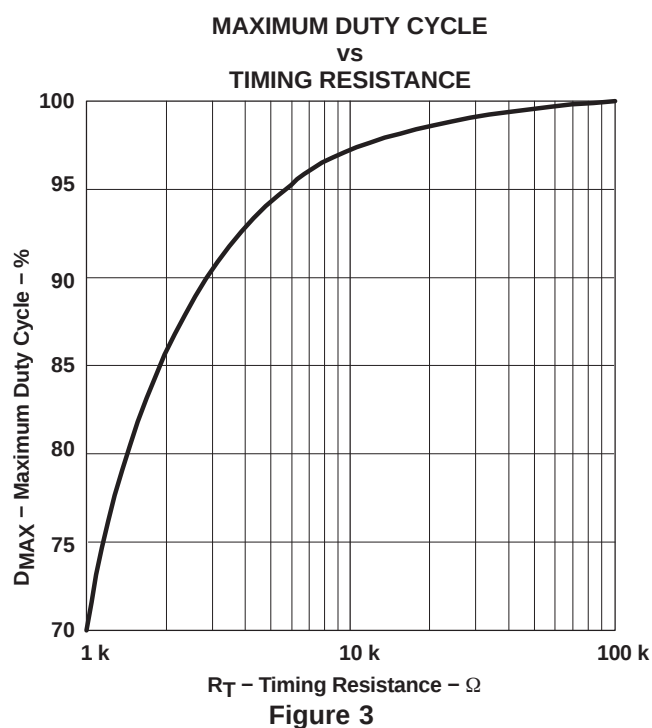
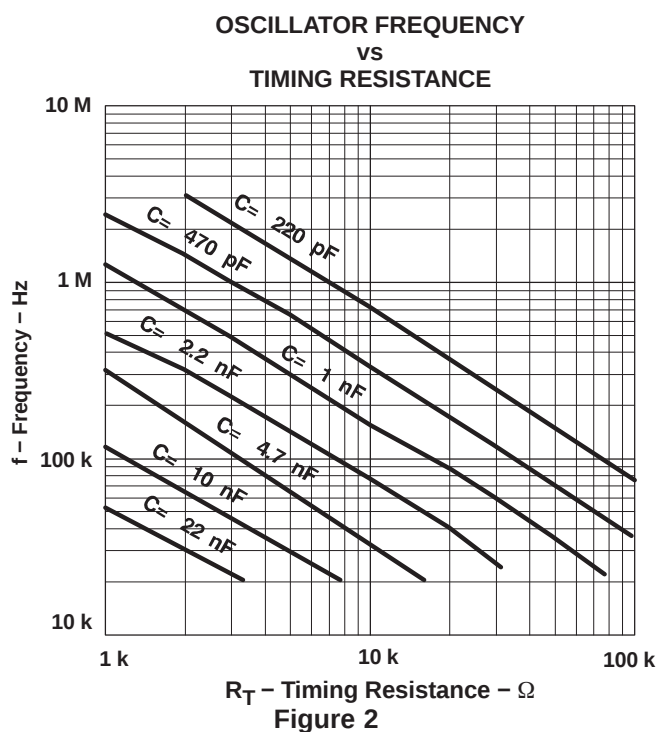
$$R_T = \frac{3 \text{ V}}{(10 \text{ mA}) \times (1 - D_{MAX})} \quad C_T = \frac{(1.6 \times D_{MAX})}{(R_T \times f)} \quad (1)$$

Recommended values for R_T range from 1 k Ω to 100 k Ω . Control of D_{MAX} less than 70% is not recommended.



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Figure 1. Oscillator



LEADING EDGE BLANKING

The UC3823A, UC2823B, UC3825A, and UC3825B perform fixed frequency pulse width modulation control. The UC3823A, and UC3823B outputs operate together at the switching frequency and can vary from zero to some value less than 100%. The UC3825A and UC3825B outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

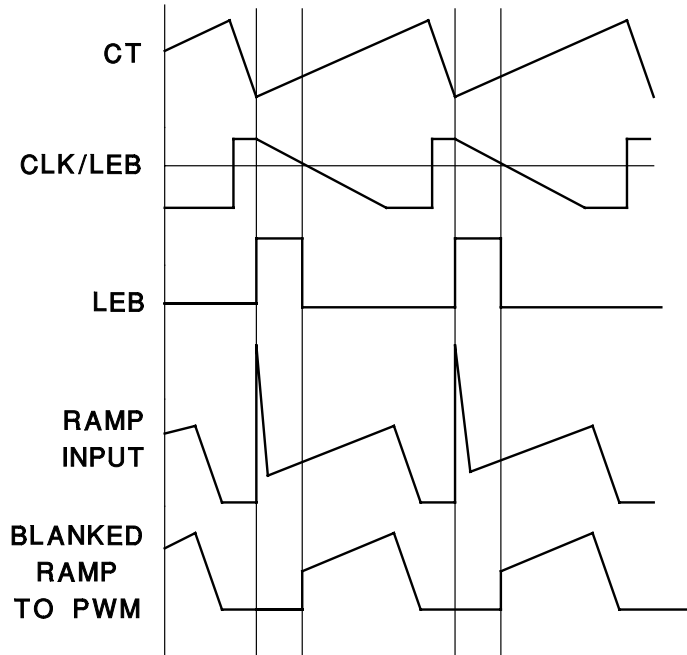
Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a leading edge blanking (LEB) period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-kΩ resistor determines the blanked interval. The 10-kΩ resistor has a 10% tolerance. For more accuracy, an external 2-kΩ 1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 kΩ with a tolerance of 2.4%. The design equation is:

$$t_{LEB} = 0.5 \times (R \parallel 10 \text{ k}\Omega) \times C \quad (2)$$

Values of R less than 2 kΩ should not be used.

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.



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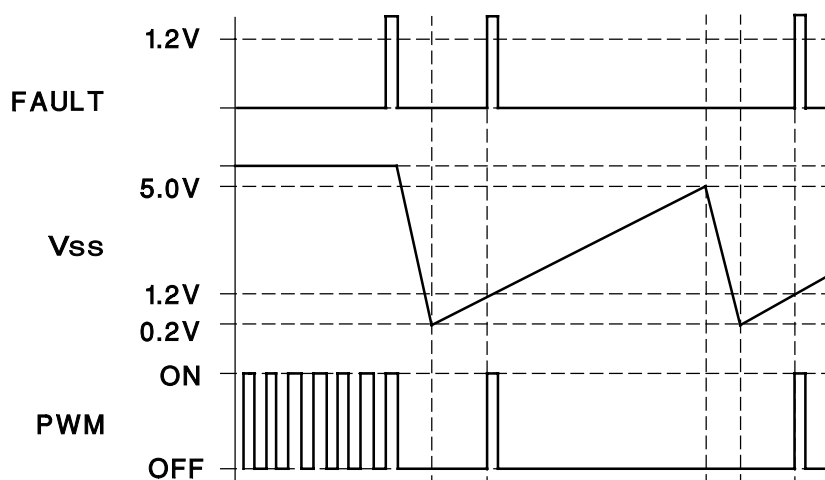
Figure 4. Leading Edge Blanking Operational Waveforms

UVLO, SOFT-START AND FAULT MANAGEMENT

Soft-start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amplifier output is also forced low. While the internal 9- μ A source charges the SS pin, the error amplifier output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2 V, the fault latch is set and the output pins are driven low. The soft-start cap is then discharged by a 250- μ A current sink. No more output pulses are allowed until soft-start is fully discharged and ILIM is below 1.2 V. At this point the fault latch resets and the chip executes a soft-start.

Should the fault latch get set during soft-start, the outputs are immediately terminated, but the soft-start capacitor does not discharge until it has been fully charged first. This results in a controlled hiccup interval for continuous fault conditions.

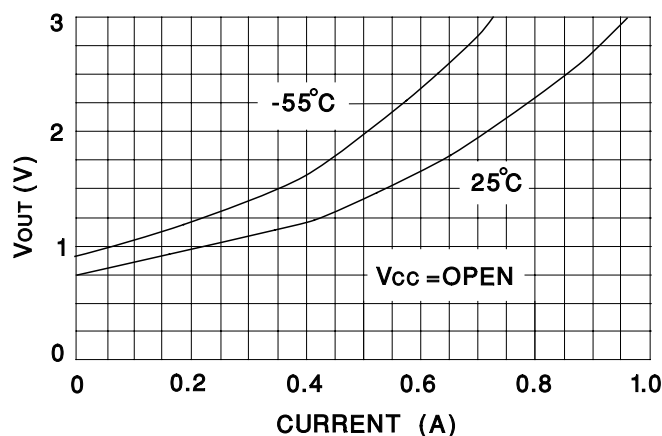


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Figure 5. Soft-Start and Fault Waveforms

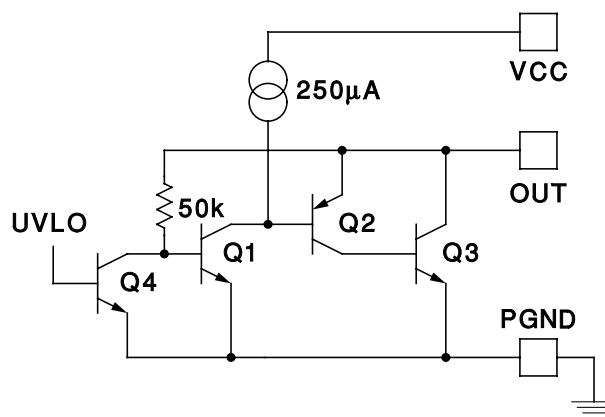
ACTIVE LOW OUTPUTS DURING UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.



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Figure 6. Output Voltage vs Output Current



UDG-95106

Figure 7. Output V and I During UVLO

CONTROL METHODS

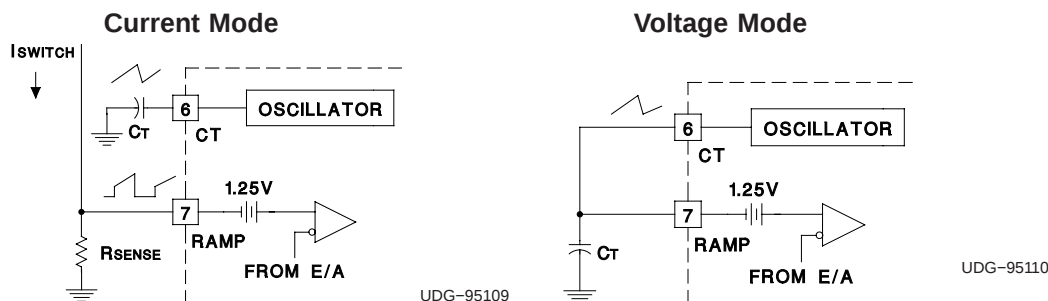


Figure 8. Control Methods

SYNCHRONIZATION

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10 ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that the CLK/LEB pin no longer accepts an incoming synchronizing signal.

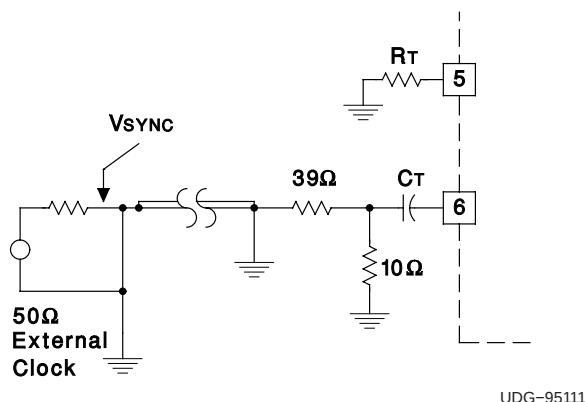


Figure 9. General Oscillator Synchronization

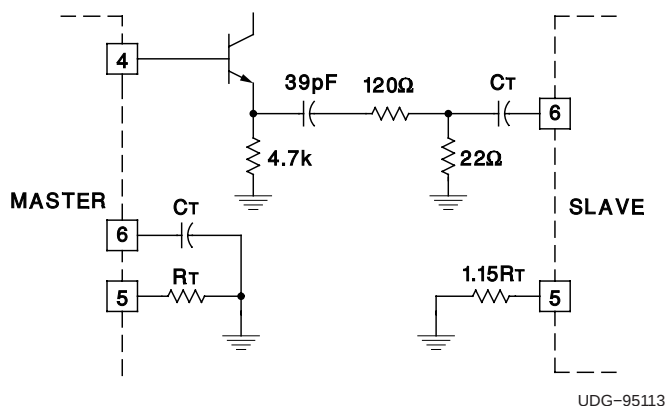
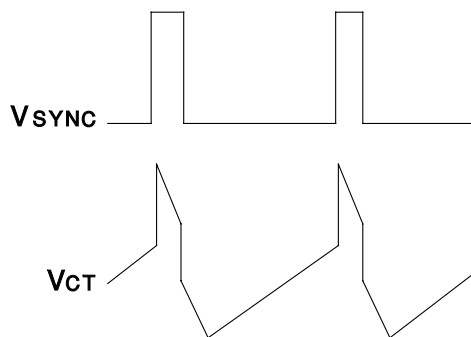


Figure 10. Two Unit Interface



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Figure 11. Operational Waveforms

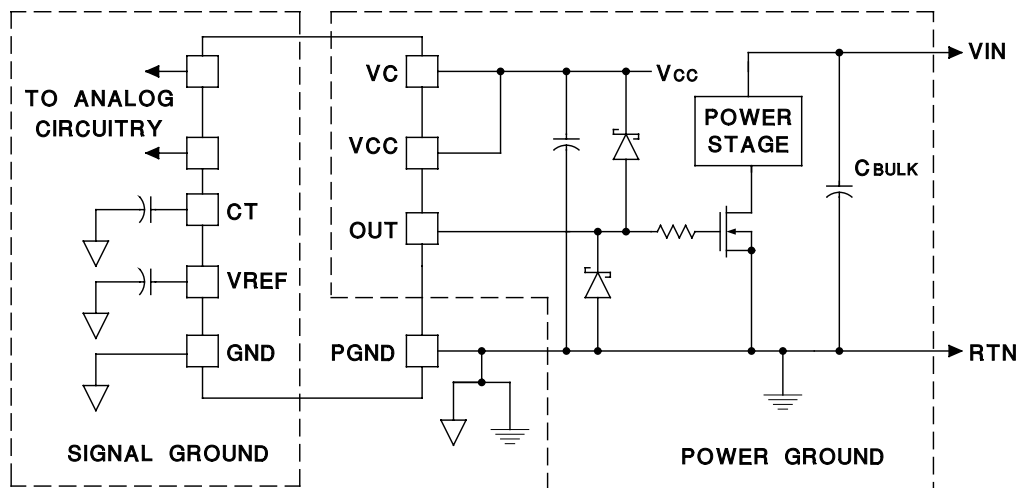
Although they are *single-ended* devices, two output drivers are available on the UC3823A and UC3823B devices. These can be *paralleled* by the use of a 0.5 Ω (noninductive) resistor connected in series with each output for a combined peak current of 4 A.



Figure 12. Power MOSFET Drive Circuit

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1-mF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.

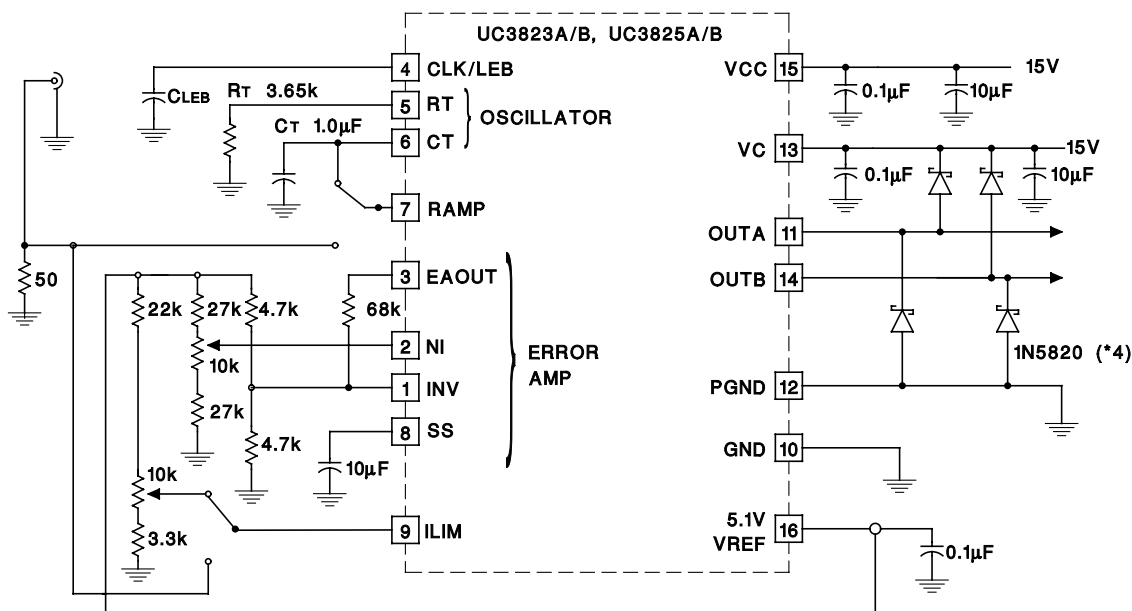


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Figure 13. Ground Planes Diagram

OPEN LOOP TEST CIRCUIT

This test fixture is useful for exercising many functions of this device family and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.



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Figure 14. Open Loop Test Circuit Schematic

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

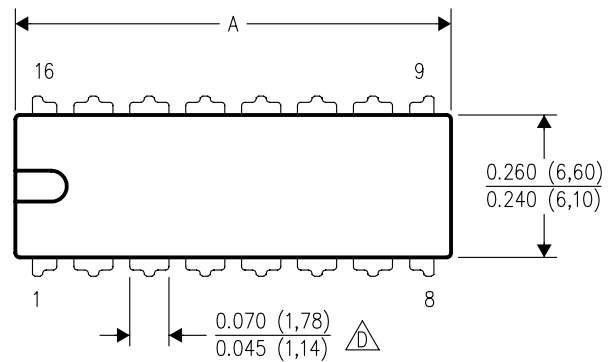


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

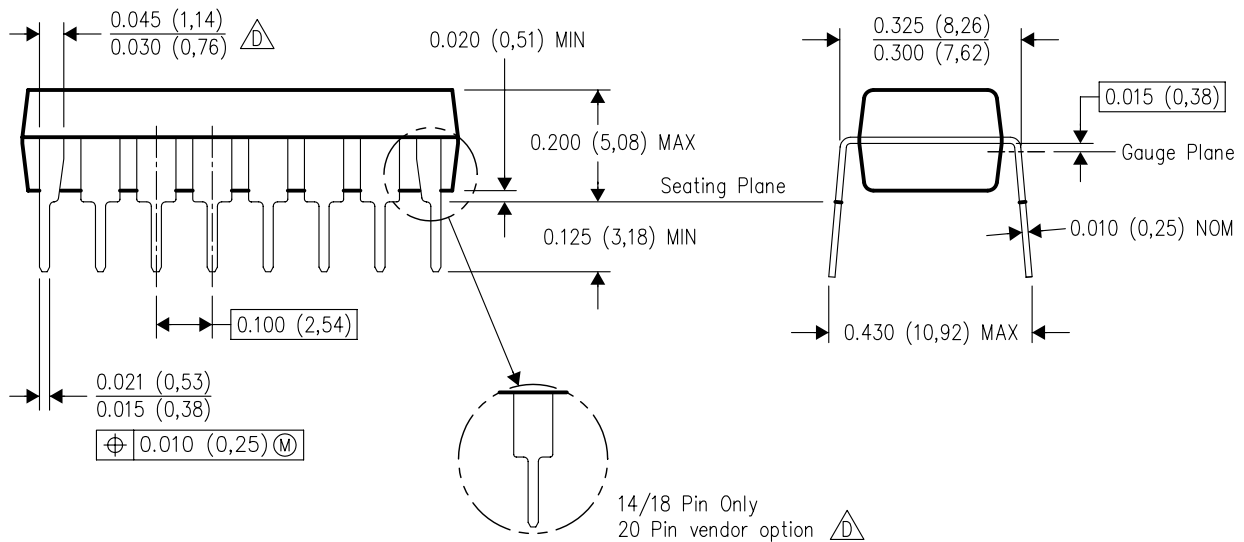
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

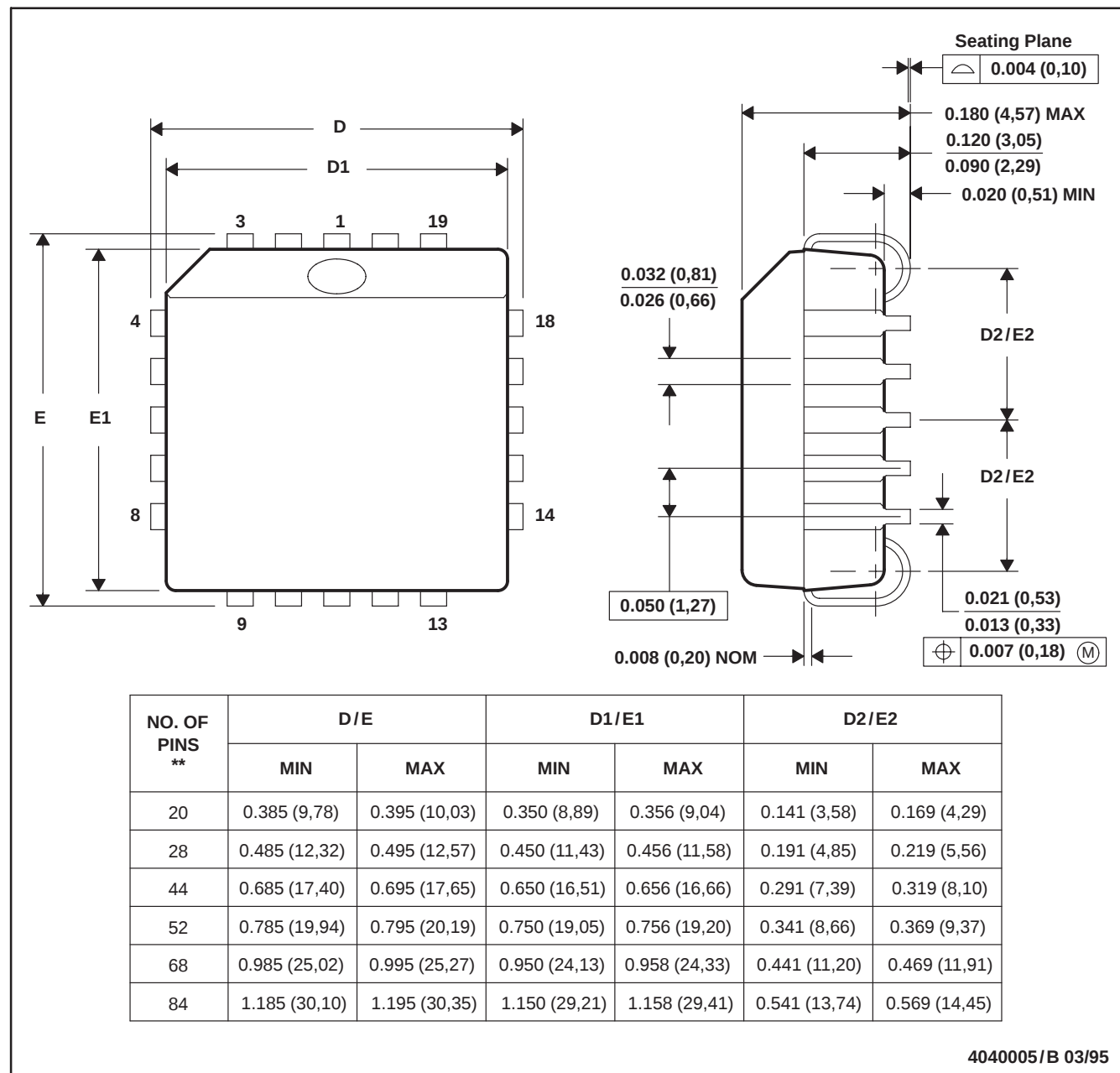
NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

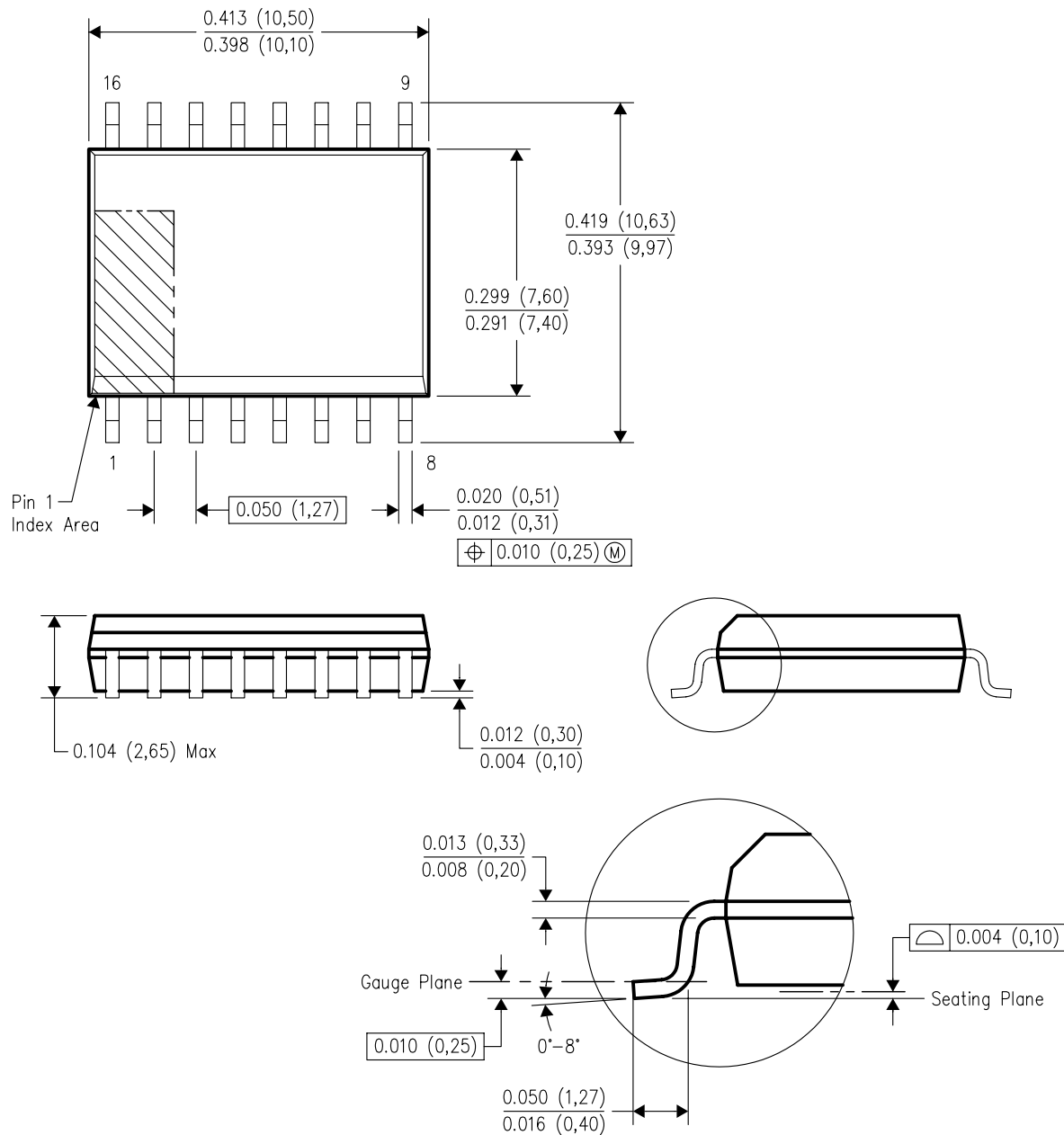
20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

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