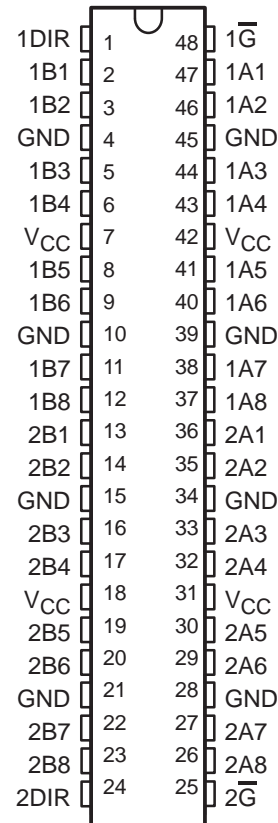


# SN54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus*™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V<sub>CC</sub> and GND Configuration to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings, Thin Shrink Small-Outline (DGG) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

SN54ACT16245 . . . WD PACKAGE  
74ACT16245 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The SN54ACT16245 and 74ACT16245 are 16-bit bus transceivers organized as dual-octal noninverting 3-state transceivers and designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The enable ( $\overline{G}$ ) input can be used to disable the devices so that the buses are effectively isolated.

The SN54ACT16245 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74ACT16245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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 **TEXAS  
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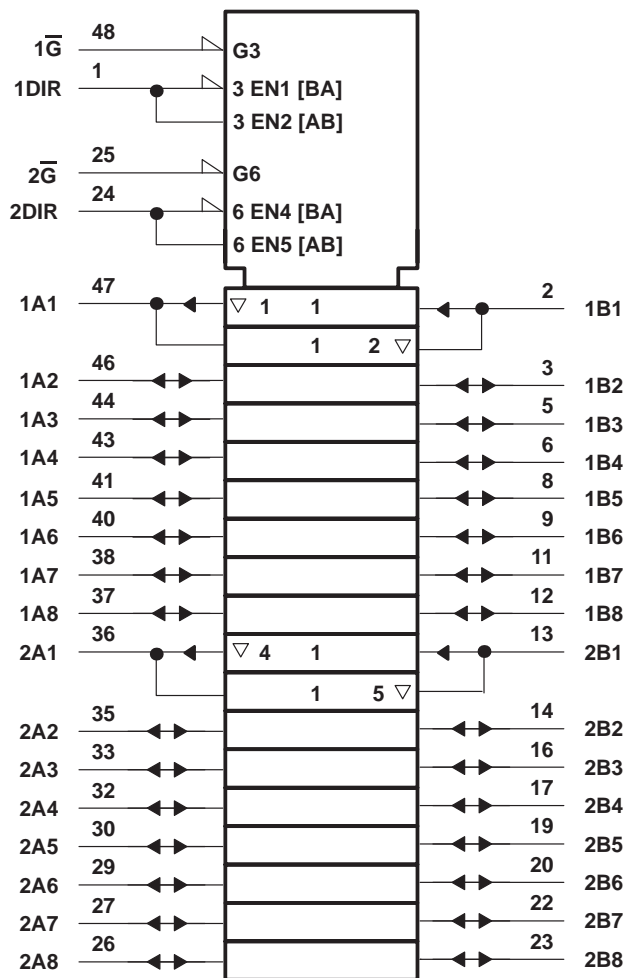
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# SN54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

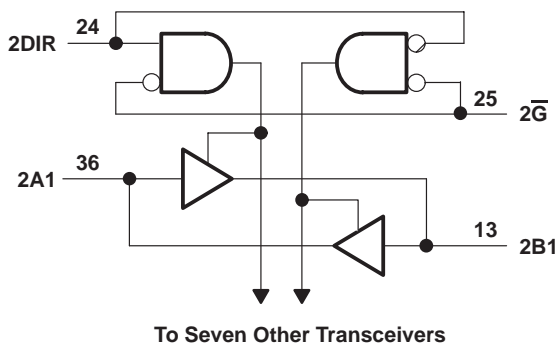
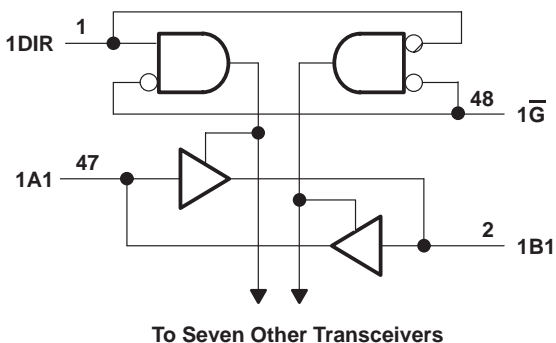
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# SN54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package .....	0.85 W
DL package .....	1.2 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## recommended operating conditions (see Note 3)

		SN54ACT16245		74ACT16245		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage (see Note 4)	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–24	mA
$I_{OL}$	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

- NOTES: 3. Unused inputs should be tied to  $V_{CC}$  through a pullup resistor of approximately 5 kΩ or greater to keep them from floating.  
 4. All  $V_{CC}$  and GND pins must be connected to the proper voltage power supply.



# SN54ACT16245, 74ACT16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54ACT16245		74ACT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		4.4	V	
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.94			3.94		3.8		
		5.5 V	4.94			4.94		4.8		
	I <sub>OH</sub> = -50 mA <sup>†</sup>	5.5 V				3.85				
I <sub>OH</sub> = -75 mA <sup>†</sup>	5.5 V						3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	0.1	V	
		5.5 V			0.1		0.1	0.1		
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V					1.65			
I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V						1.65			
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND			±0.1		±1	±1	μA	
I <sub>OZ</sub>	A or B ports <sup>‡</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND			±0.5		±10	±5	μA	
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0			8		160	80	μA	
ΔI <sub>CC</sub> <sup>§</sup>		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>			0.9		1	1	mA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND			4.5				pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND			16				pF	

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current I<sub>I</sub>.

<sup>§</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

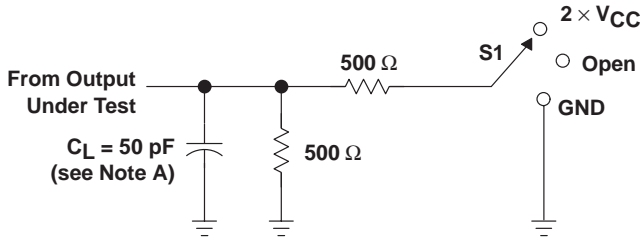
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN54ACT16245		74ACT16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	3.2	6.9	9.3	3.2	11.5	3.2	10.5	ns
t <sub>PHL</sub>			2.6	6.4	9.2	2.6	11.1	2.6	10.2	
t <sub>PZH</sub>	$\bar{G}$	B or A	2.7	6.4	9.1	2.7	10.9	2.7	10	ns
t <sub>PZL</sub>			3.4	7.4	10.5	3.4	12.6	3.4	11.6	
t <sub>PHZ</sub>	$\bar{G}$	B or A	5.8	9.2	11.6	5.8	13.4	5.8	12.6	ns
t <sub>PLZ</sub>			5.5	8.5	10.8	5.5	12.7	5.5	11.8	

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	52	pF
		Outputs disabled	10	

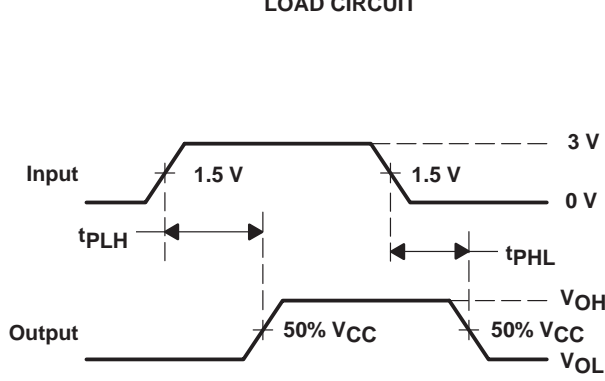


PARAMETER MEASUREMENT INFORMATION

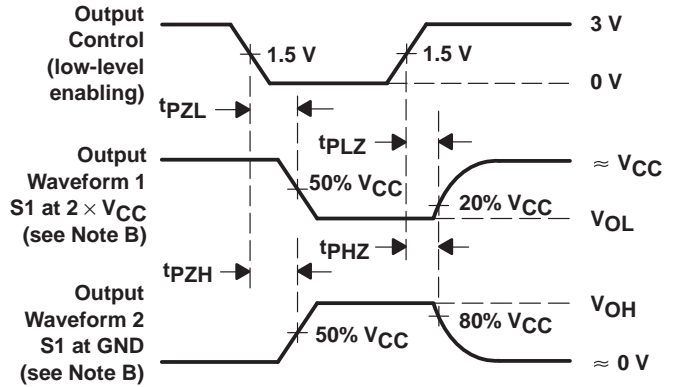


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9202301MXA	ACTIVE	CFP	WD	48	1	None	Call TI	Level-NC-NC-NC
74ACT16245DGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
74ACT16245DL	ACTIVE	SSOP	DL	48	25	None	CU NIPDAU	Level-1-235C-UNLIM
74ACT16245DLR	ACTIVE	SSOP	DL	48	1000	None	CU NIPDAU	Level-1-235C-UNLIM
SNJ54ACT16245WD	ACTIVE	CFP	WD	48	1	None	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

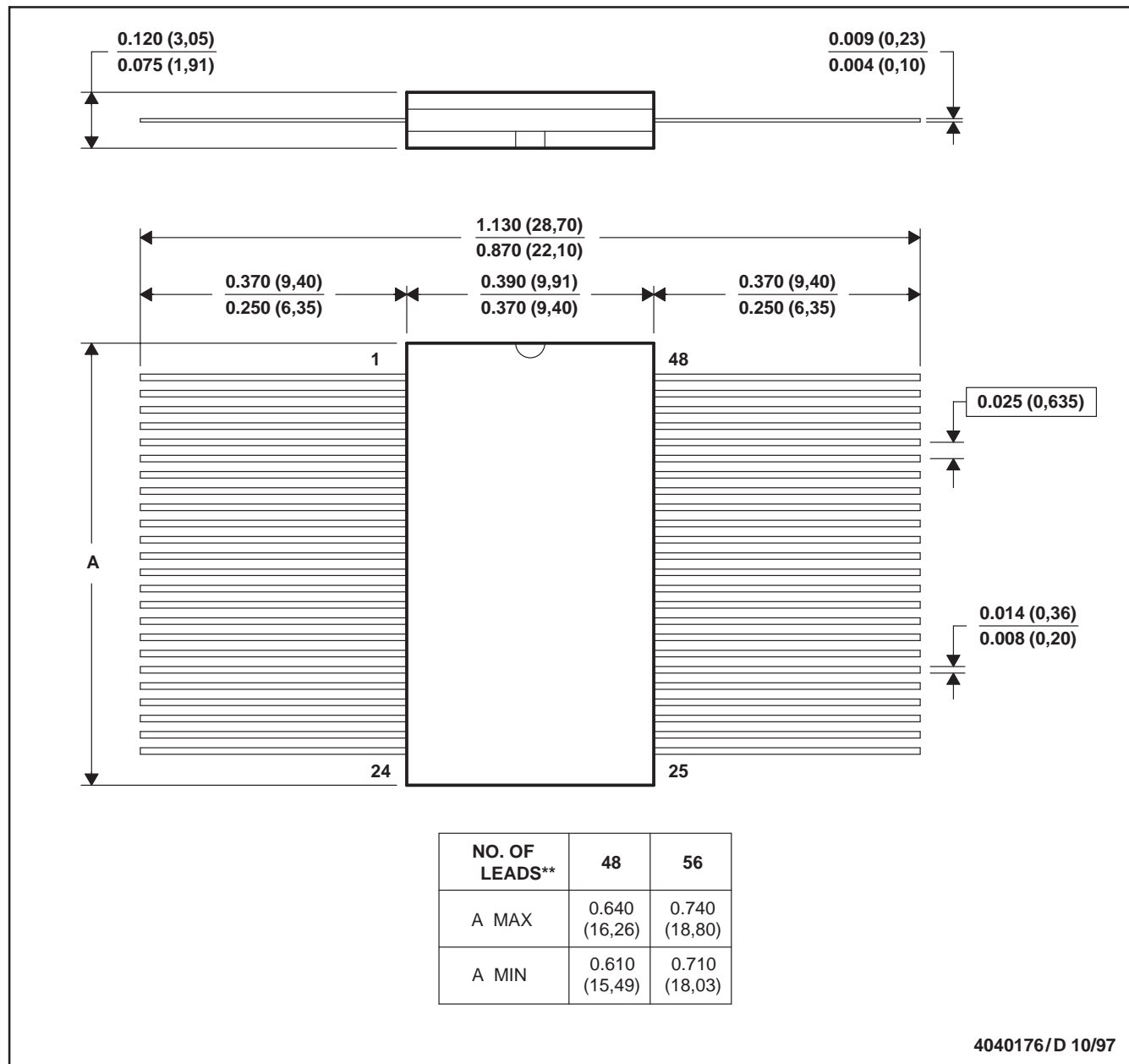
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WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN

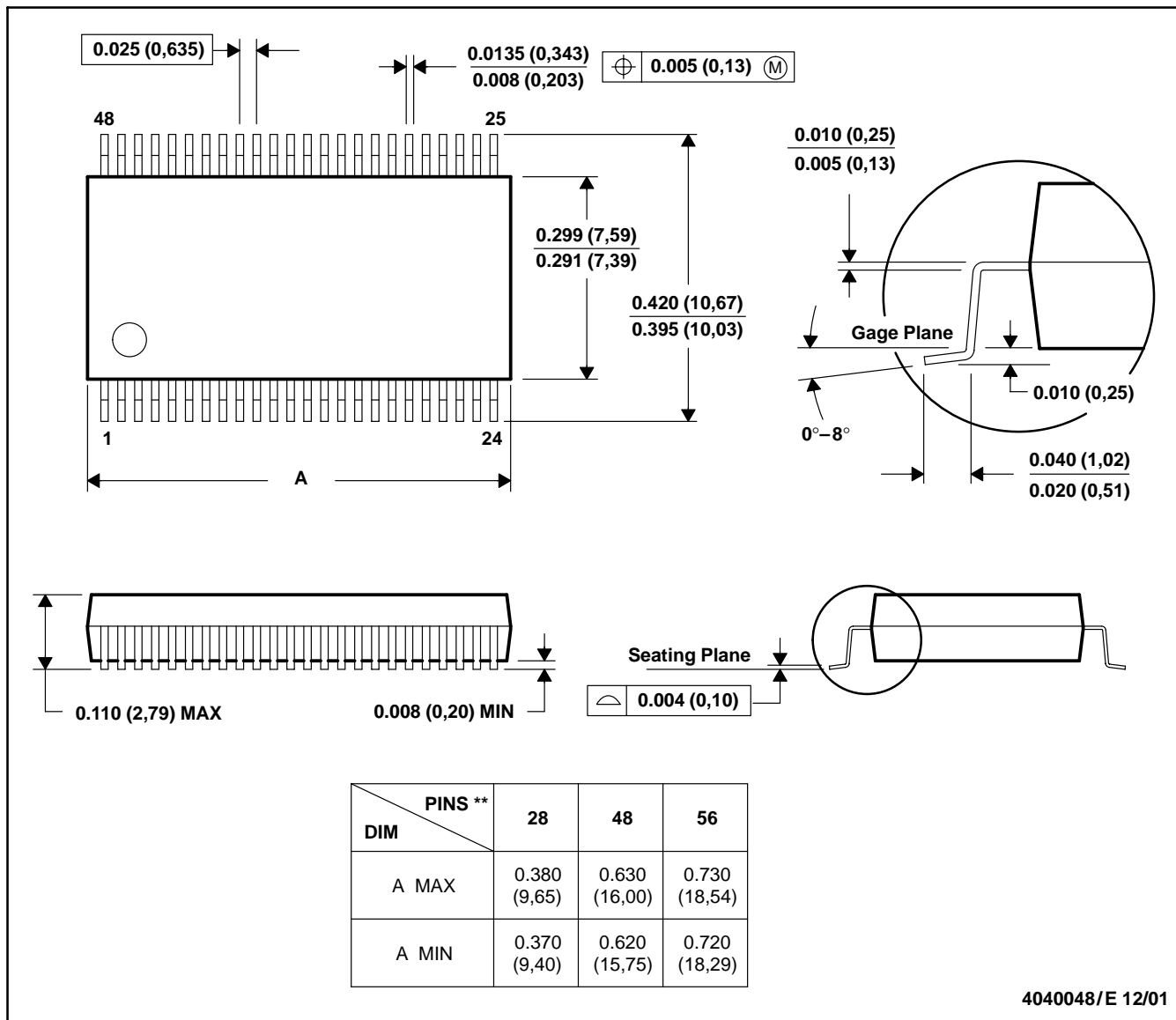


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

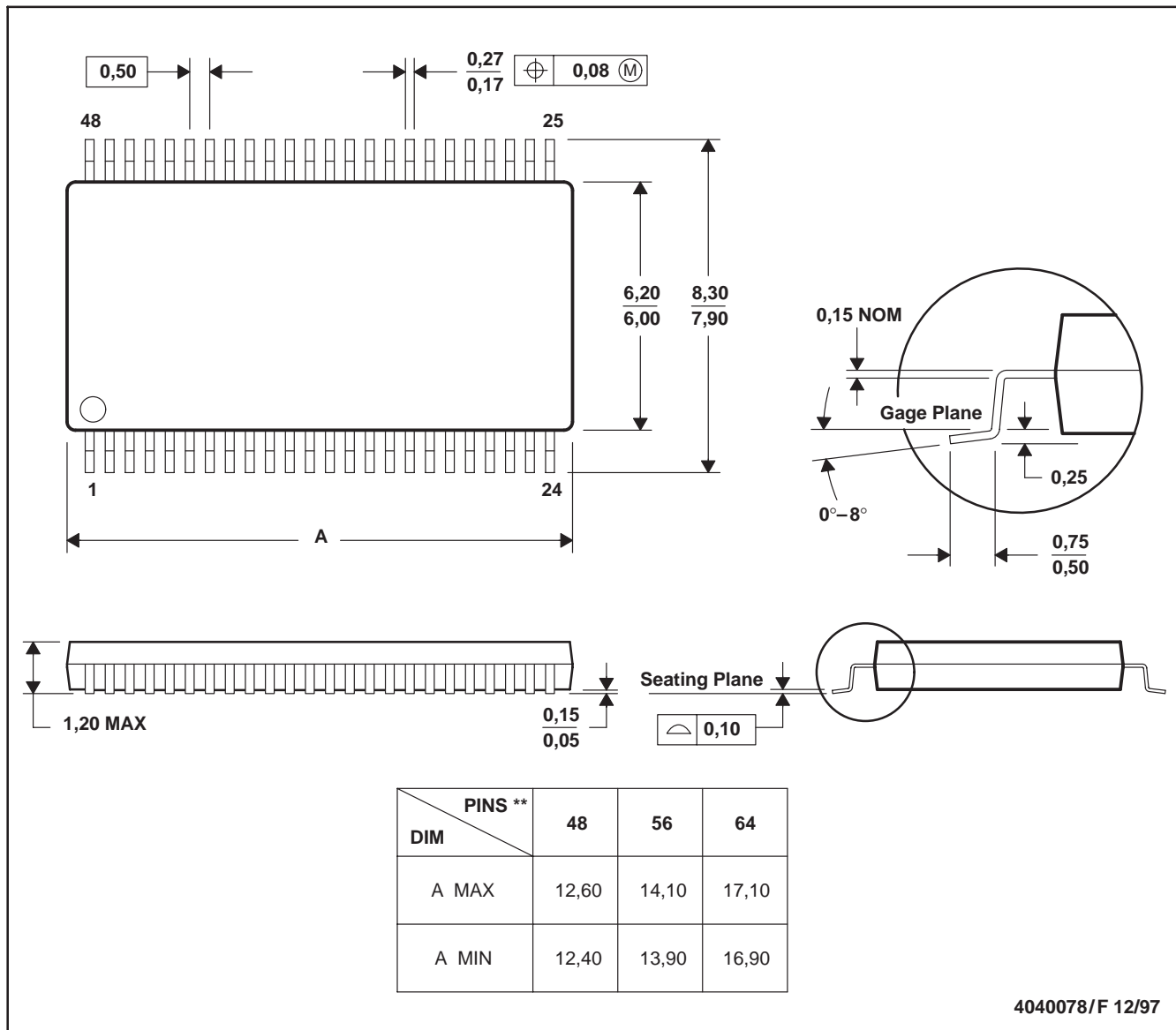


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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