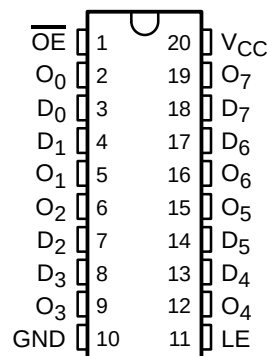


CY54FCT373T, CY74FCT373T 8-BIT LATCHES WITH 3-STATE OUTPUTS

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- Function and Pinout Compatible With FCT and F Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- 3-State Outputs
- CY54FCT373T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT373T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current

CY54FCT373T . . . D PACKAGE
CY74FCT373T . . . Q OR SO PACKAGE
(TOP VIEW)



description

The 'FCT373T devices consist of eight latches with 3-state outputs for bus-organized applications. When the latch-enable (LE) input is high, the flip-flops appear transparent to the data. Data that meets the required setup times are latched when LE transitions from high to low. Data appears on the bus when the output-enable ($\overline{OE}$) input is low. When $\overline{OE}$ is high, the bus output is in the high-impedance state. In this mode, data can be entered into the latches.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



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**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	4.7	CY74FCT373CTQCT	FCT373C
	SOIC – SO	Tube	4.7	CY74FCT373CTSOC	FCT373C
		Tape and reel	4.7	CY74FCT373CTSUCT	
	QSOP – Q	Tape and reel	5.2	CY74FCT373ATQCT	FCT373A
	SOIC – SO	Tube	5.2	CY74FCT373ATSOC	FCT373
		Tape and reel	5.2	CY74FCT373ATSUCT	
	SOIC – SO	Tube	8	CY74FCT373TSOC	FCT373
		Tape and reel	8	CY74FCT373TSUCT	
–55°C to 125°C	CDIP – D	Tube	5.6	CY54FCT373ATDMB	

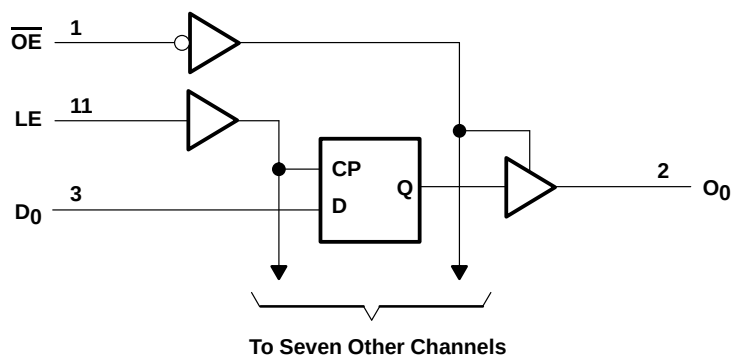
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUT O
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

H = High logic level, L = Low logic level,
X = Don'tcare, Z=High-impedance state,
 Q_n = Previous state of flip flops (Q_{n-1})

logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

	CY54FCT373T			CY74FCT373T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			–12			–32	mA
I_{OL} Low-level output current			32			64	mA
T_A Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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8-BIT LATCHES

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT373T			CY74FCT373T			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$	-0.7	-1.2					V
	$V_{CC} = 4.75 \text{ V}$, $I_{IN} = -18 \text{ mA}$				-0.7	-1.2		
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75 \text{ V}$				2			
					2.4	3.3		
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 32 \text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 64 \text{ mA}$				0.3	0.55		
V_{hys}	All inputs	0.2			0.2			V
I_I	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = V_{CC}$			5				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{CC}$						5	
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.7 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 2.7 \text{ V}$						± 1	
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.5 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 0.5 \text{ V}$						± 1	
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$			10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$						10	
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$			-10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$						-10	
$I_{OS}^{\ddagger}$	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0 \text{ V}$				-60	-120	-225	
I_{off}	$V_{CC} = 0 \text{ V}$, $V_{OUT} = 4.5 \text{ V}$			± 1			± 1	μA
I_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.1	0.2		
ΔI_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 3.4 \text{ V}^{\S}$, $f_1 = 0$, Outputs open	0.5	2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 3.4 \text{ V}^{\S}$, $f_1 = 0$, Outputs open				0.5	2		

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

[§] Per TTL-driven input ($V_{IN} = 3.4 \text{ V}$); all other inputs at V_{CC} or GND

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT373T			CY74FCT373T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I _{CCD} ¶	V _{CC} = 5.5 V, Outputs open, One input switching at 50% duty cycle, $\overline{OE}$ = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.06	0.12				mA/ MHz	
	V _{CC} = 5.25 V, Outputs open, One input switching at 50% duty cycle, $\overline{OE}$ = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V						0.06	0.12		
I _C [#]	V _{CC} = 5.5 V, Outputs open, $\overline{OE}$ = GND, LE = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4				mA	
			V _{IN} = 3.4 V or GND	1	2.4					
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	1.3	2.6					
			V _{IN} = 3.4 V or GND	3.3	10.6					
	V _{CC} = 5.25 V, Outputs open, $\overline{OE}$ = GND, LE = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V				0.7	1.4		
			V _{IN} = 3.4 V or GND				1	2.4		
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V				1.3	2.6		
			V _{IN} = 3.4 V or GND				3.3	10.6		
C _i				6	10		6	10	pF	
C _o				8	12		8	12	pF	

[†] Typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[¶] This parameter is derived for use in total power-supply calculations.

[#] $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4$ V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

^{||} Values for these conditions are examples of the I_{CC} formula.

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8-BIT LATCHES

WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FCT373T		CY54FCT373AT		UNIT
		MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	6		6		ns
t_{SU}	Setup time, data before LE $\uparrow$	2		2		ns
t_H	Hold time, data after LE $\uparrow$	1.5		1.5		ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY74FCT373T		CY74FCT373AT		CY74FCT373CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	6		5		5		ns
t_{SU}	Setup time, data before LE $\uparrow$	2		2		2		ns
t_H	Hold time, data after LE $\uparrow$	1.5		1.5		1.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

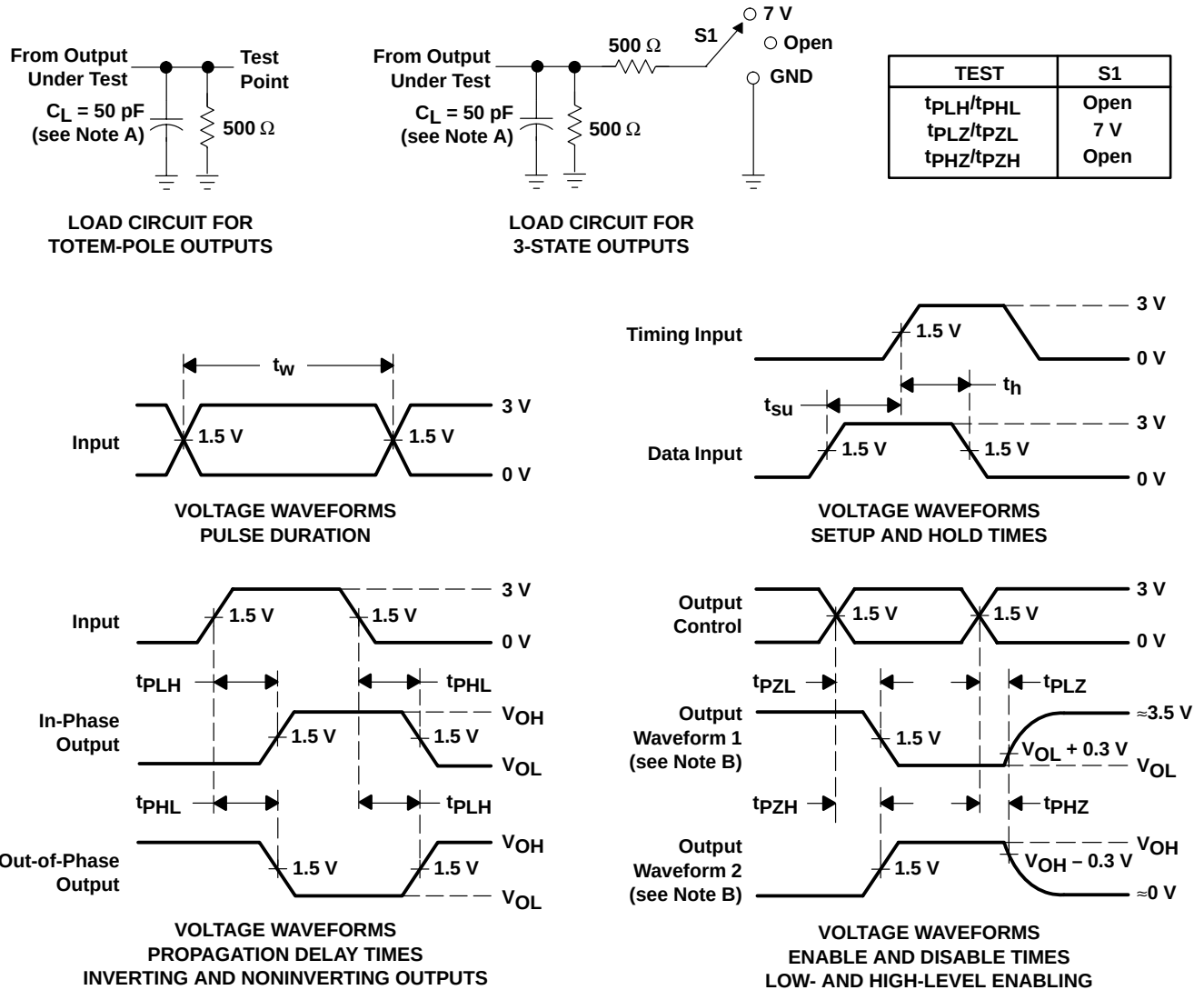
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT373AT		UNIT
			MIN	MAX	
t_{PLH}	D	O	1.5	5.6	ns
t_{PHL}			1.5	5.6	
t_{PLH}	LE	O	2	9.8	ns
t_{PHL}			2	9.8	
t_{PZH}	$\overline{OE}$	O	1.5	7.5	ns
t_{PZL}			1.5	7.5	
t_{PHZ}	$\overline{OE}$	O	1.5	6.5	ns
t_{PLZ}			1.5	6.5	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT373T		CY74FCT373AT		CY74FCT373CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	O	1.5	8	1.5	5.2	1.5	4.7	ns
t_{PHL}			1.5	8	1.5	5.2	1.5	4.7	
t_{PLH}	LE	O	2	13	2	8.5	2	5.5	ns
t_{PHL}			2	13	2	8.5	2	5.5	
t_{PZH}	$\overline{OE}$	O	1.5	12	1.5	6.5	1.5	5.5	ns
t_{PZL}			1.5	12	1.5	6.5	1.5	5.5	
t_{PHZ}	$\overline{OE}$	O	1.5	7.5	1.5	5.5	1.5	5	ns
t_{PLZ}			1.5	7.5	1.5	5.5	1.5	5	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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