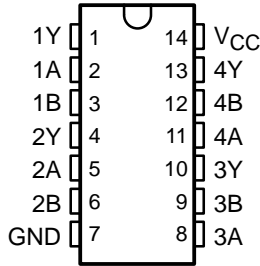


SN54AHCT02, SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

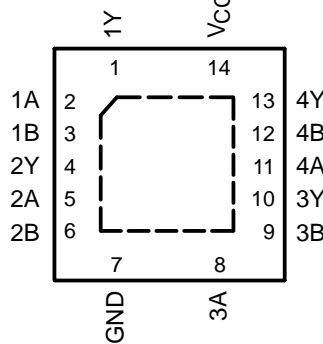
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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

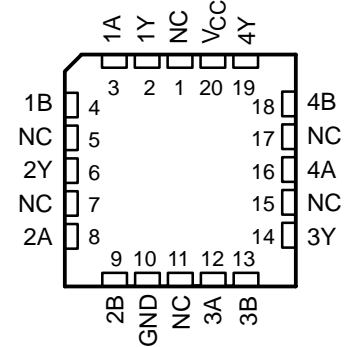
SN54AHCT02... J OR W PACKAGE
SN74AHCT02... D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHCT02... RGY PACKAGE
(TOP VIEW)



SN54AHCT02... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AHCT02RGYR	HB02
	PDIP – N	Tube	SN74AHCT02N	SN74AHCT02N
	SOIC – D	Tube	SN74AHCT02D	AHCT02
		Tape and reel	SN74AHCT02DR	
	SOP – NS	Tape and reel	SN74AHCT02NSR	AHCT02
	SSOP – DB	Tape and reel	SN74AHCT02DBR	HB02
	TSSOP – PW	Tube	SN74AHCT02PW	HB02
Tape and reel		SN74AHCT02PWR		
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74AHCT02DGV	HB02
	CDIP – J	Tube	SNJ54AHCT02J	SNJ54AHCT02J
	CFP – W	Tube	SNJ54AHCT02W	SNJ54AHCT02W
	LCCC – FK	Tube	SNJ54AHCT02FK	SNJ54AHCT02FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

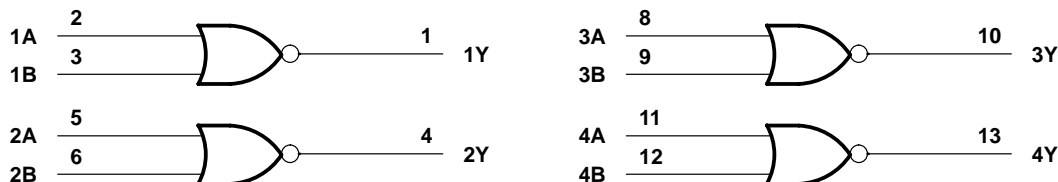
SN54AHCT02, SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54AHCT02, SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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recommended operating conditions (see Note 4)

		SN54AHCT02		SN74AHCT02		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-8		-8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT02		SN74AHCT02		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1			0.1	V	
	I _{OL} = 8 mA				0.36		0.44	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20	20	μA	
ΔI _{CC} †	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			1.35		1.5	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V		4	10			10	pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHCT02		SN74AHCT02		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	2.4**	5.5**		1**	6.5**	1	6.5	ns
t _{PHL}				3.5**	5.5**		1**	6.5**	1	6.5	
t _{PLH}	A or B	Y	C _L = 50 pF	3.4	7.5		1	8.5	1	8.5	ns
t _{PHL}				4.5	7.5		1	8.5	1	8.5	

** On products compliant to MIL-PRF-38535, this parameter is not production tested.



SN54AHCT02, SN74AHCT02 QUADRUPLE 2-INPUT POSITIVE-NOR GATES

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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74AHCT02			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}			-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

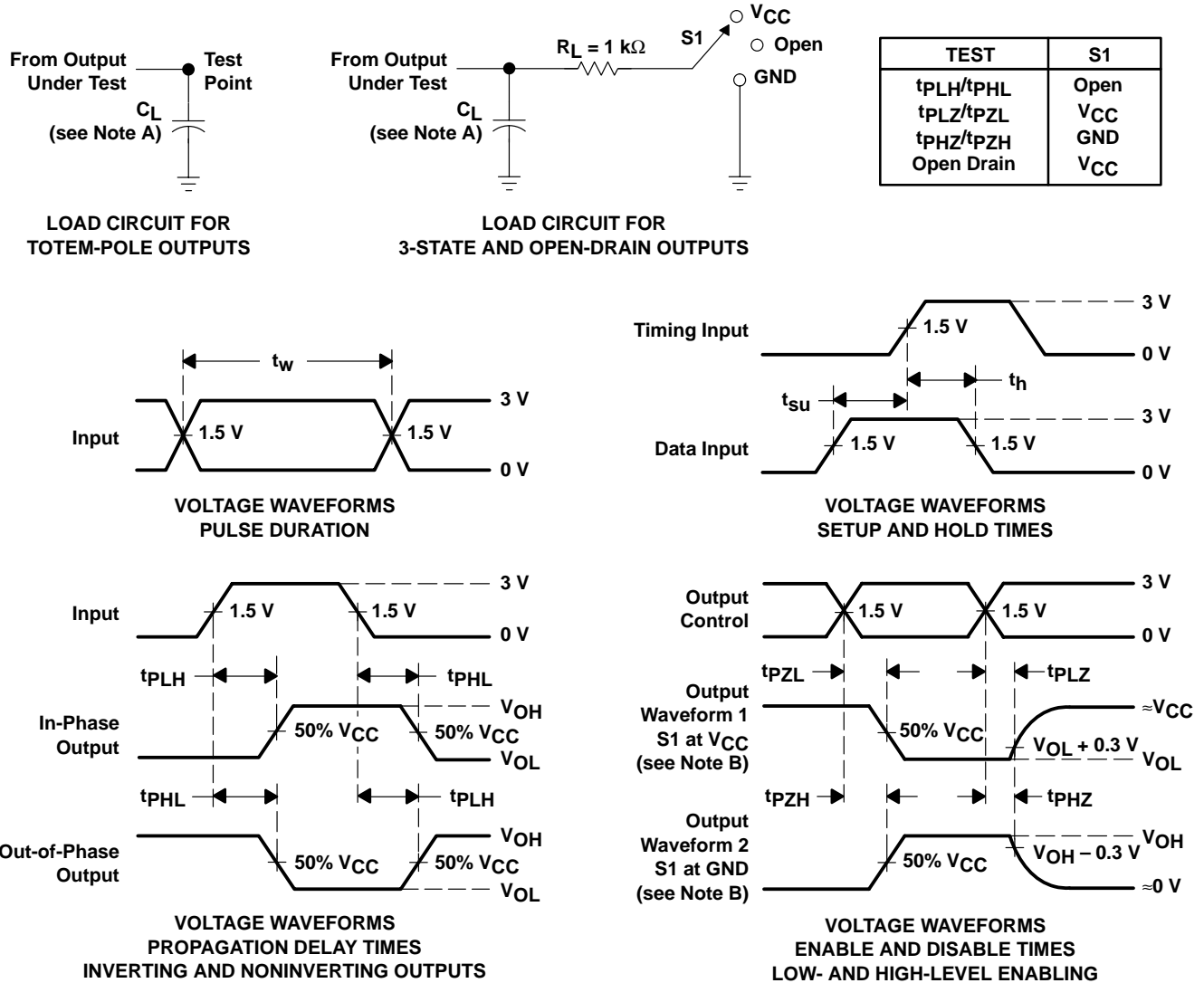
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	17	pF



PARAMETER MEASUREMENT INFORMATION





Input

t_w

1.5 V

3 V

0 V

VOLTAGE WAVEFORMS PULSE DURATION



Timing Input

3 V

1.5 V

0 V

t_{su}

t_h

Data Input

3 V

1.5 V

0 V

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



Input

3 V

1.5 V

0 V

t_{PLH}

t_{PHL}

In-Phase Output

$50\% V_{CC}$

V_{OH}

V_{OL}

t_{PHL}

t_{PLH}

Out-of-Phase Output

$50\% V_{CC}$

V_{OH}

V_{OL}

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



Output Control

3 V

1.5 V

0 V

t_{PZL}

t_{PLZ}

Output Waveform 1 S1 at VCC (see Note B)

$50\% V_{CC}$

$\approx V_{CC}$

$V_{OL} + 0.3\text{ V}$

V_{OL}

t_{PZH}

t_{PHZ}

Output Waveform 2 S1 at GND (see Note B)

$50\% V_{CC}$

$V_{OH} - 0.3\text{ V}$

V_{OH}

$\approx 0\text{ V}$

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9757101Q2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9757101QCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
5962-9757101QDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SN74AHCT02D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHCT02DBLE	OBSOLETE	SSOP	DB	14		None	Call TI	Call TI
SN74AHCT02DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHCT02DGVR	ACTIVE	TVSOP	DGV	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHCT02DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHCT02N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AHCT02NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHCT02PW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHCT02PWLE	OBSOLETE	TSSOP	PW	14		None	Call TI	Call TI
SN74AHCT02PWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHCT02RGYR	ACTIVE	QFN	RGY	14	1000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR
SNJ54AHCT02FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54AHCT02J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54AHCT02W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

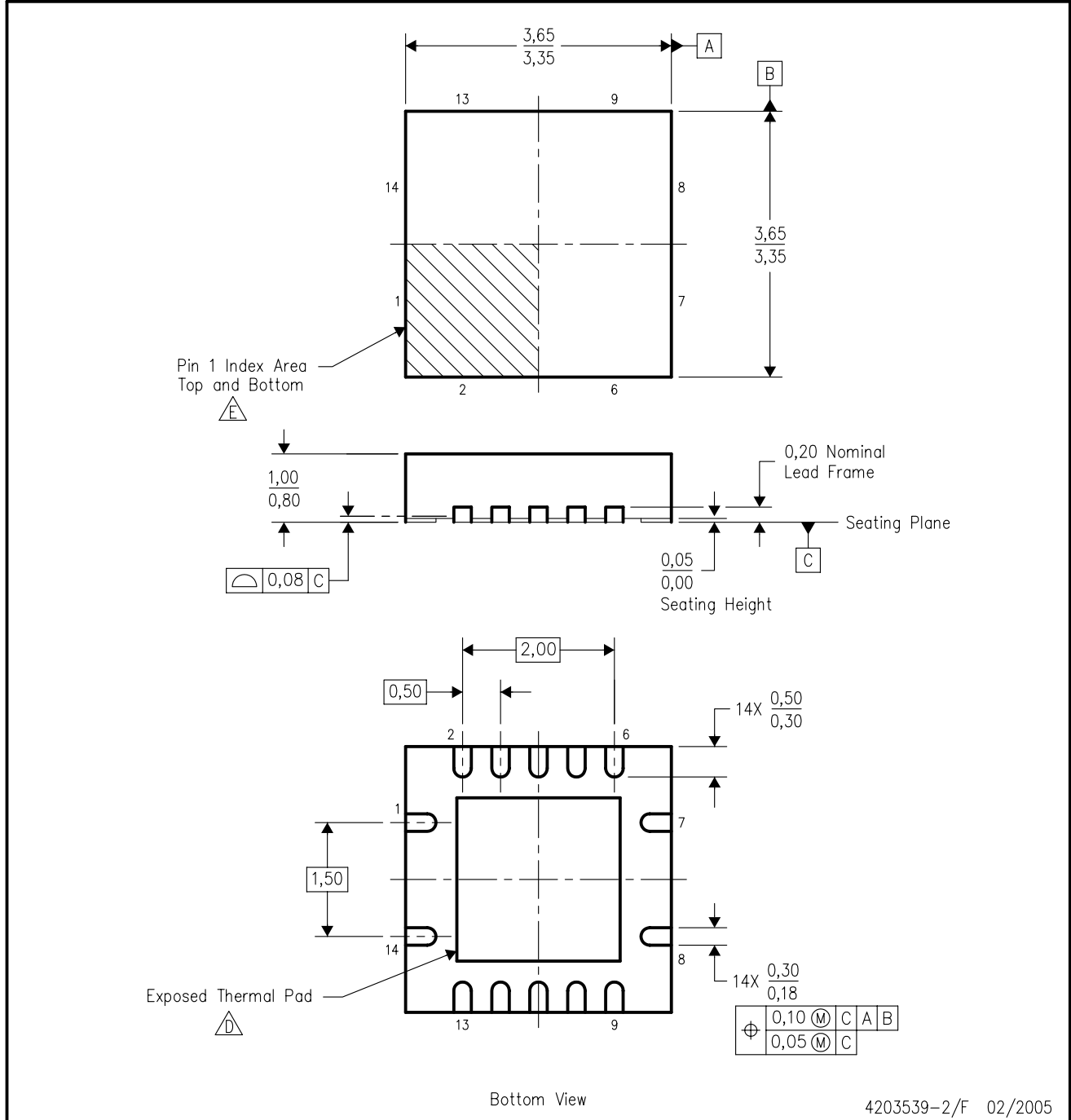
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
- ⚠ The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- ⚠ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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