

54AC16245, 74AC16245 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS235A – MARCH 1990 – REVISED APRIL 1996

- Members of the Texas Instruments *Widebus*™ Family
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Configuration Minimizes High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) Package, 300-mil Shrink Small-Outline (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Pin Spacings

description

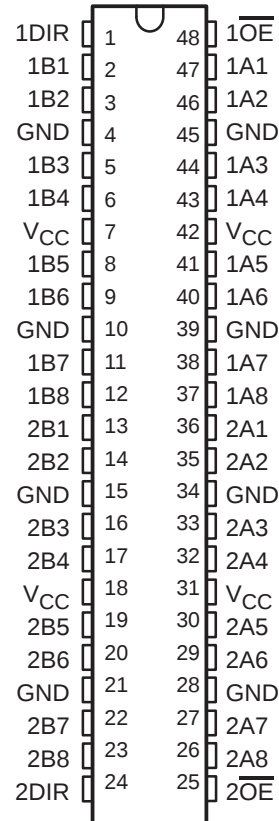
The 'AC16245 are 16-bit bus transceivers organized as dual-octal noninverting 3-state transceivers designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The output-enable input ($\overline{OE}$) can be used to disable the devices so that the buses are effectively isolated.

The 74AC16245 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16245 is characterized for operation from –40°C to 85°C.

54AC16245 . . . WD PACKAGE
74AC16245 . . . DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to bus
H	X	Isolation



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

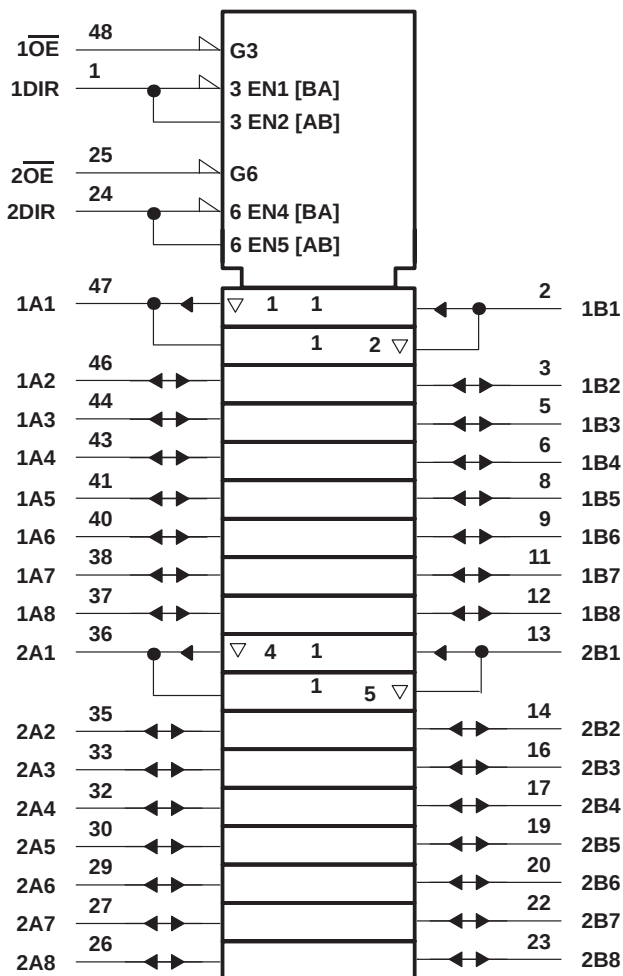
**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

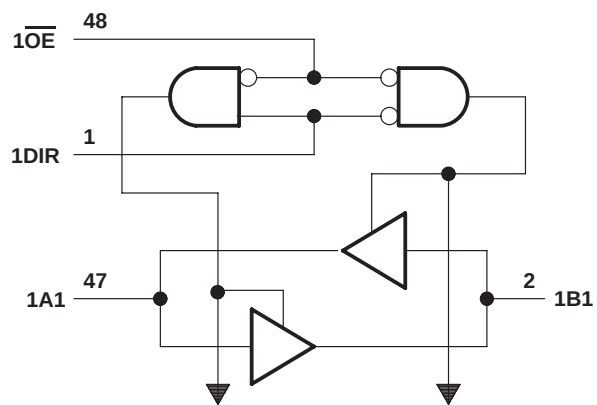
54AC16245, 74AC16245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
 SCAS235A – MARCH 1990 – REVISED APRIL 1996

logic symbol†

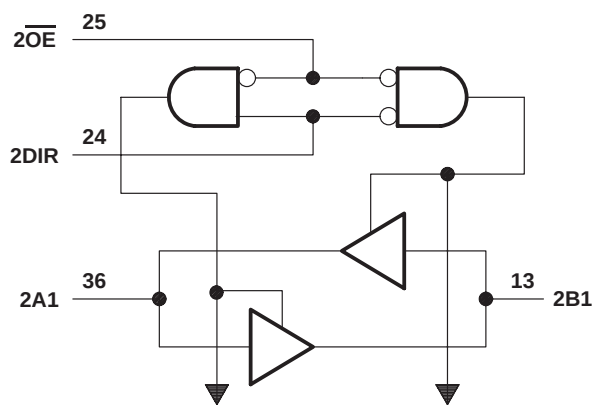


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Transceivers



To Seven Other Transceivers

54AC16245, 74AC16245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCAS235A – MARCH 1990 – REVISED APRIL 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			54AC16245			74AC16245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 4)		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V	0.9			0.9			V
		V _{CC} = 4.5 V	1.35			1.35			
		V _{CC} = 5.5 V	1.65			1.65			
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
I _{OH}	High-level output current	V _{CC} = 3 V	−4			−4			mA
		V _{CC} = 4.5 V	−24			−24			
		V _{CC} = 5.5 V	−24			−24			
I _{OL}	Low-level output current	V _{CC} = 3 V	12			12			mA
		V _{CC} = 4.5 V	24			24			
		V _{CC} = 5.5 V	24			24			
Δt/Δv	Input transition rise or fall rate		0	10		0	10		ns/V
T _A	Operating free-air temperature		−55	125		−40	85		°C

- NOTES: 3. All unused pins (input and I/O) must be held high or low to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage power supply.

54AC16245, 74AC16245
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
 SCAS235A – MARCH 1990 – REVISED APRIL 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC16245		74AC16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
		5.5 V	4.94			4.8		4.8		
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.44		0.44	
		4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
I _I	I _{OL} = 24 mA	3 V			0.36		0.44		0.44	µA
		4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.44		0.44	
	I _{OL} = 75 mA†	3 V					1.65		1.65	
		4.5 V					1.65		1.65	
		5.5 V					1.65		1.65	
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1		±1	µA
I _{OZ}	V _I = V _{CC} or GND	5.5 V			±0.5		±5		±5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8		80		80	µA
C _i	V _I = V _{CC} or GND	5 V		4.5						pF
C ₀	V _I = V _{CC} or GND	5 V		16						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC16245		74AC16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	2.5	7.6	10.4	2.5	11.9	2.5	11.9	ns
t _{PHL}			3.1	9	12.3	3.1	13.5	3.1	13.5	
t _{PZH}	$\overline{\text{OE}}$	A or B	2.8	8.6	11.8	2.8	13.2	2.8	13.2	ns
t _{PZL}			3.9	12	16.2	3.9	18	3.9	18	
t _{PHZ}	$\overline{\text{OE}}$	A or B	5.3	8.4	10.4	5.3	11.2	5.3	11.2	ns
t _{PLZ}			4.4	7.7	9.7	4.4	10.3	4.4	10.3	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = 25°C			54AC16245		74AC16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	2	4.6	6.9	2	7.9	2	7.9	ns
t _{PHL}			2.5	5.2	7.9	2.5	8.9	2.5	8.9	
t _{PZH}	$\overline{\text{OE}}$	A or B	2.3	4.9	7.5	2.3	8.6	2.3	8.6	ns
t _{PZL}			3	6.2	9.5	3	10.7	3	10.7	
t _{PHZ}	$\overline{\text{OE}}$	A or B	5	7.2	9.1	5	9.8	5	9.8	ns
t _{PLZ}			4.2	6.2	8.1	4.2	8.7	4.2	8.7	

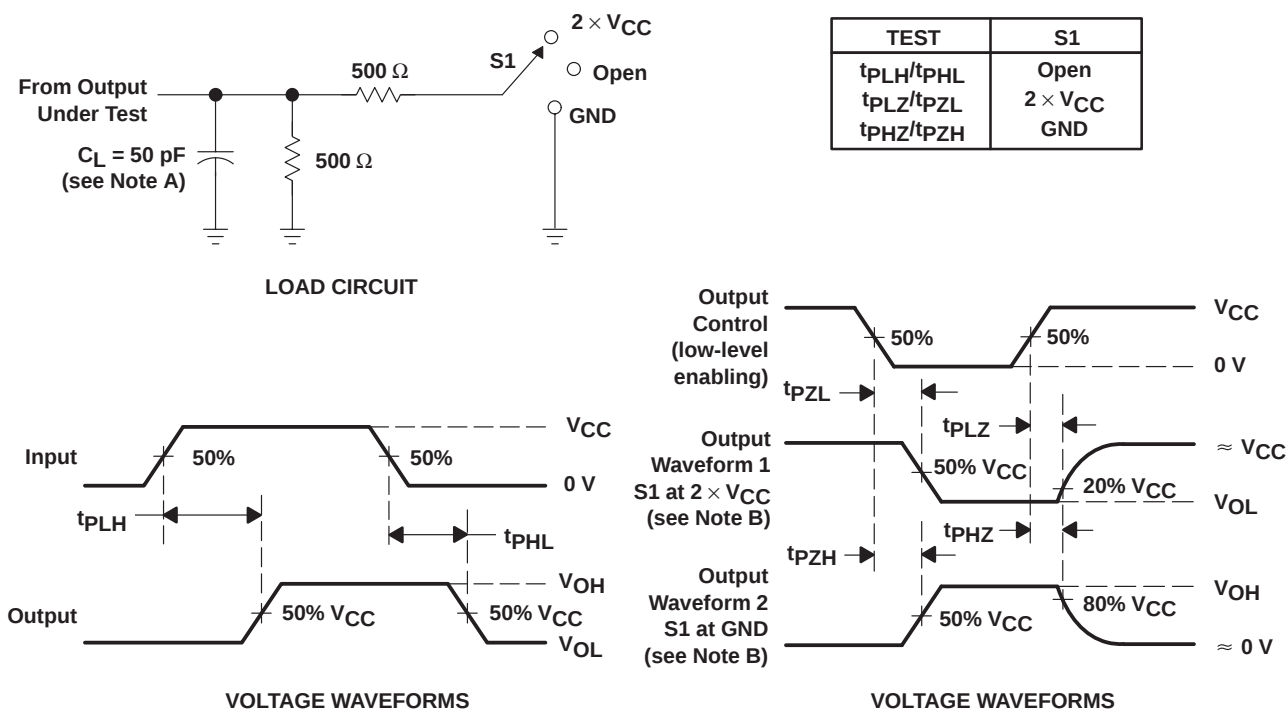
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$	43	pF
	Outputs enabled		8	

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.