

FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 5 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

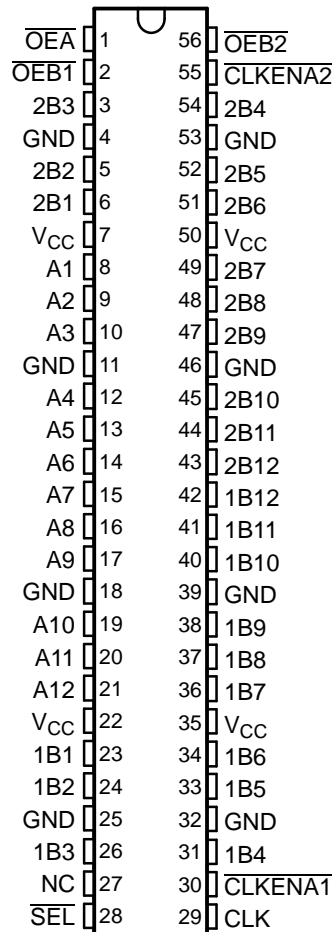
DESCRIPTION/ORDERING INFORMATION

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16269 is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (\overline{CLKENA}) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select (\overline{SEL}) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (\overline{OEA} , $\overline{OEB1}$, $\overline{OEB2}$).

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH16269DL	ALVCH16269
		Tape and reel	SN74ALVCH16269DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH16269DGGR	ALVCH16269
	VFBGA - GQL	Tape and reel	SN74ALVCH16269KR	VH269
	VFBGA - ZQL (Pb-free)		74ALVCH16269ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN74ALVCH16269
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

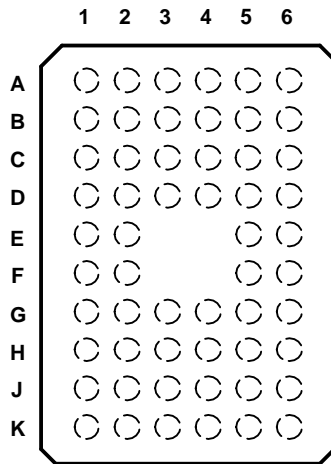
SCES019N–JULY 1995–REVISED JULY 2004

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to \overline{OE} being routed through a register, the active state of the outputs cannot be determined before the arrival of the first clock pulse.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

GQL OR ZQL PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	2B3	$\overline{OEB1}$	\overline{OEA}	$\overline{OEB2}$	$\overline{CLKENA2}$	2B4
B	2B1	2B2	GND	GND	2B5	2B6
C	A2	A1	V_{CC}	V_{CC}	2B7	2B8
D	A4	A3	GND	GND	2B9	2B10
E	A6	A5			2B11	2B12
F	A7	A8			1B11	1B12
G	A9	A10	GND	GND	1B9	1B10
H	A11	A12	V_{CC}	V_{CC}	1B7	1B8
J	1B1	1B2	GND	GND	1B5	1B6
K	1B3	NC	\overline{SEL}	CLK	$\overline{CLKENA1}$	1B4

FUNCTION TABLES

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE\bar{A}}$	$\overline{OE\bar{B}}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OE\bar{B}} = L$)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
L	H	↑	L	L	2B ₀ ⁽¹⁾
L	H	↑	H	H	2B ₀ ⁽¹⁾
L	L	↑	L	L	L
L	L	↑	H	H	H
H	L	↑	L	1B ₀ ⁽¹⁾	L
H	L	↑	H	1B ₀ ⁽¹⁾	H
H	H	X	X	1B ₀ ⁽¹⁾	2B ₀ ⁽¹⁾

- (1) Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OE\bar{A}} = L$)

INPUTS				OUTPUT
CLK	\overline{SEL}	1B	2B	A
X	H	X	X	A ₀ ⁽¹⁾
X	L	X	X	A ₀ ⁽¹⁾
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

- (1) Output level before the indicated steady-state input conditions were established

SN74ALVCH16269
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES019N—JULY 1995—REVISED JULY 2004

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DL packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	4.6	V
V _I	Input voltage range	Except I/O ports ⁽²⁾		V
		-0.5	V _{CC} + 0.5	
V _O	Output voltage range ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50
				mA
I _{OK}	Output clamp current	V _O < 0		-50
				mA
I _O	Continuous output current		±50	mA
	Continuous current through each V _{CC} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package		81
		DL package		74
		GQL/ZQL package		42
				°C/W
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V		V
		V _{CC} = 2.3 V to 2.7 V		
		V _{CC} = 2.7 V to 3.6 V		
		0.65 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		V
		V _{CC} = 2.3 V to 2.7 V		
		V _{CC} = 2.7 V to 3.6 V		
			0.35 × V _{CC}	
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		mA
		V _{CC} = 2.3 V		
		V _{CC} = 2.7 V		
		V _{CC} = 3 V		
			-4	
			-12	
			-12	
			-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		mA
		V _{CC} = 2.3 V		
		V _{CC} = 2.7 V		
		V _{CC} = 3 V		
			4	
			12	
			12	
			24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH16269
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS

SCES019N–JULY 1995–REVISED JULY 2004

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V
		I _{OH} = -4 mA	1.65 V	1.2			
		I _{OH} = -6 mA	2.3 V	2			
		I _{OH} = -12 mA	2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
	I _{OH} = -24 mA	3 V	2				
V _{OL}		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 6 mA	2.3 V			0.4	
		I _{OL} = 12 mA	2.3 V			0.7	
			2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
I _I		V _I = V _{CC} or GND	3.6 V			±5	μA
I _{I(hold)}		V _I = 0.58 V	1.65 V	25			μA
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V	2.3 V	-45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		V _I = 0 to 3.6 V ⁽²⁾	3.6 V			±500	
I _{OZ} ⁽³⁾		V _O = V _{CC} or GND	3.6 V			±10	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA
ΔI _{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3.5			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	9			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	(1)		135		135		135		MHz
t_w	Pulse duration, CLK high or low	(1)		3.3		3.3		3.3		ns
t_{su}	Setup time	A data before CLK \uparrow		(1)		2		1.7		ns
		B data before CLK \uparrow		(1)		2.2		1.8		
		$\overline{\text{SEL}}$ before CLK \uparrow		(1)		1.6		1.3		
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK \uparrow		(1)		1		0.9		
		$\overline{\text{OE}}$ before CLK \uparrow		(1)		1.5		1.3		
t_h	Hold time	A data after CLK \uparrow		(1)		0.7		0.6		ns
		B data after CLK \uparrow		(1)		0.7		0.6		
		$\overline{\text{SEL}}$ after CLK \uparrow		(1)		1.1		0.7		
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK \uparrow		(1)		1		1.1		
		$\overline{\text{OE}}$ after CLK \uparrow		(1)		0.8		0.8		

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		135		135		135		MHz
t_{pd}	CLK	B	(1)		1	8.2	7.3		1	6.2	ns
		A	(1)		1	6.4	5.8		1	5	
t_{en}	CLK	B	(1)		1	7.9	6.7		1	6.1	ns
		A	(1)		1	7.6	6.2		1	5.9	
t_{dis}	CLK	B	(1)		1	8.1	6.9		1	6.1	ns
		A	(1)		1	7.5	6.8		1	5.6	

(1) This information was not available at the time of publication.

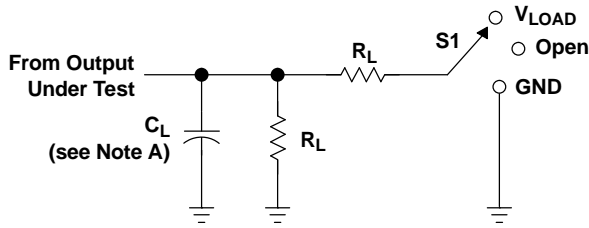
OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per exchanger	All outputs enabled	(1)	87	120	pF
		All outputs disabled	(1)	80.5	118	

(1) This information was not available at the time of publication.

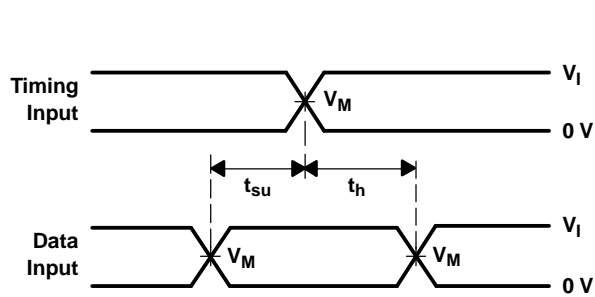
PARAMETER MEASUREMENT INFORMATION



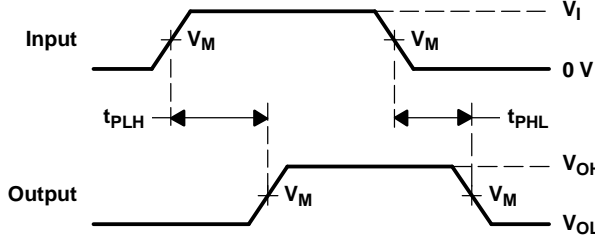
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{LOAD} GND

LOAD CIRCUIT

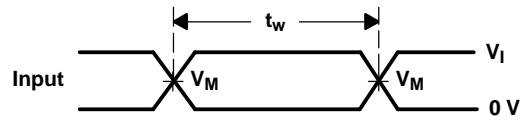
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.2 V$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3 V \pm 0.3 V$	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



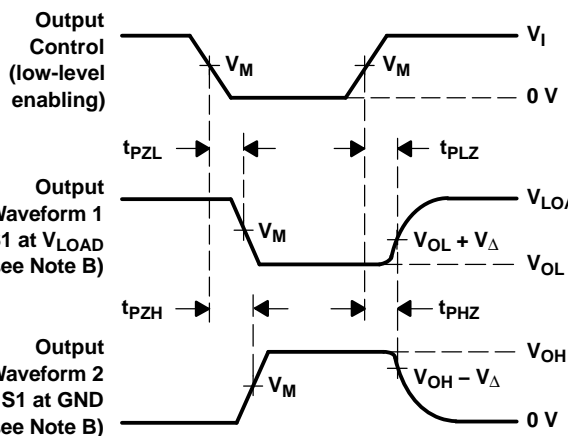
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCH16269ZQLR	ACTIVE	VFBGA	ZQL	56	1000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74ALVCH16269DGGR	ACTIVE	TSSOP	DGG	56	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74ALVCH16269DL	ACTIVE	SSOP	DL	56	20	None	CU NIPDAU	Level-1-235C-UNLIM
SN74ALVCH16269DLR	ACTIVE	SSOP	DL	56	1000	None	CU NIPDAU	Level-1-235C-UNLIM
SN74ALVCH16269KR	ACTIVE	VFBGA	GQL	56	1000	None	SNPB	Level-1-240C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

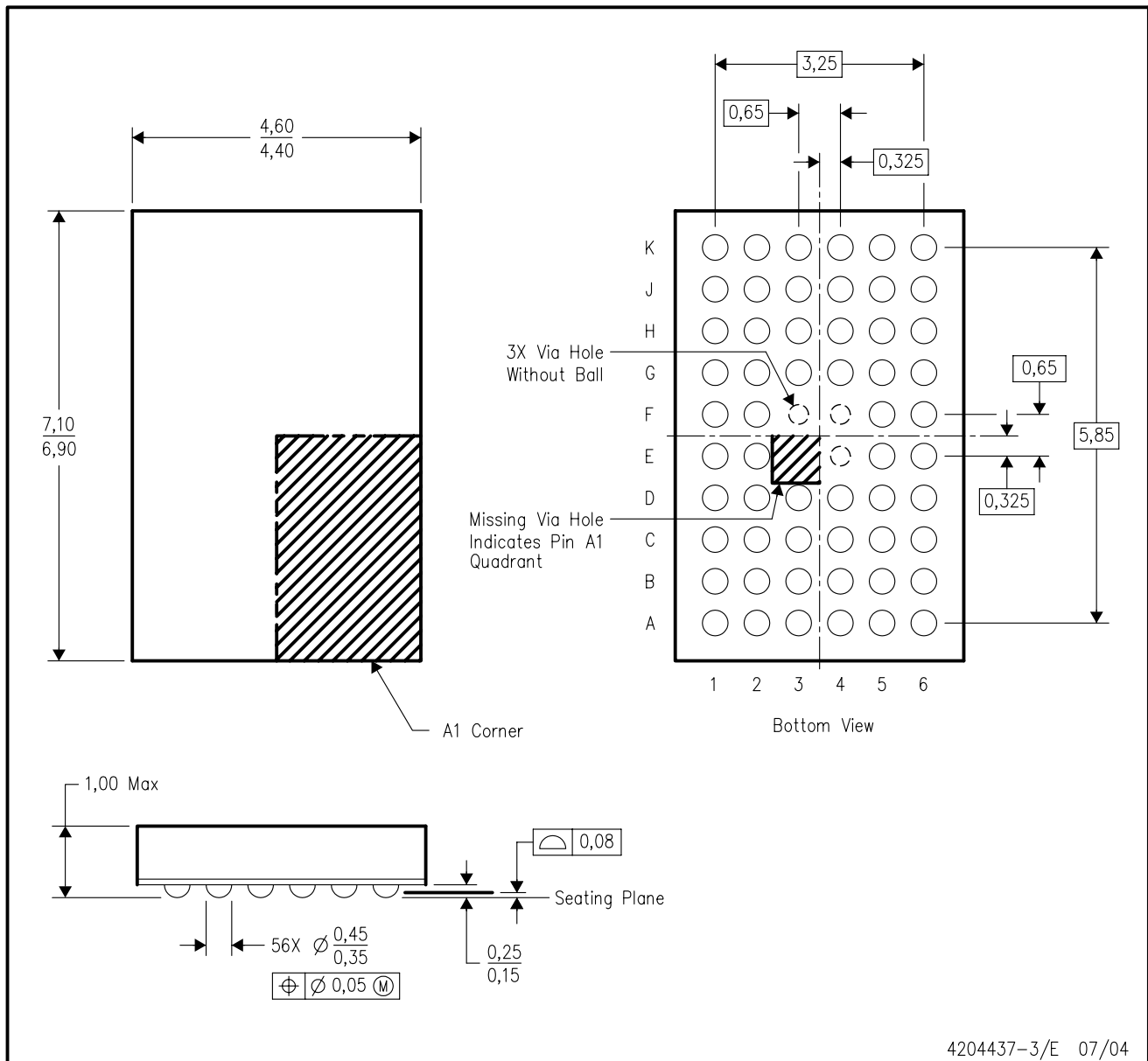
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

ZQL (R-PBGA-N56)

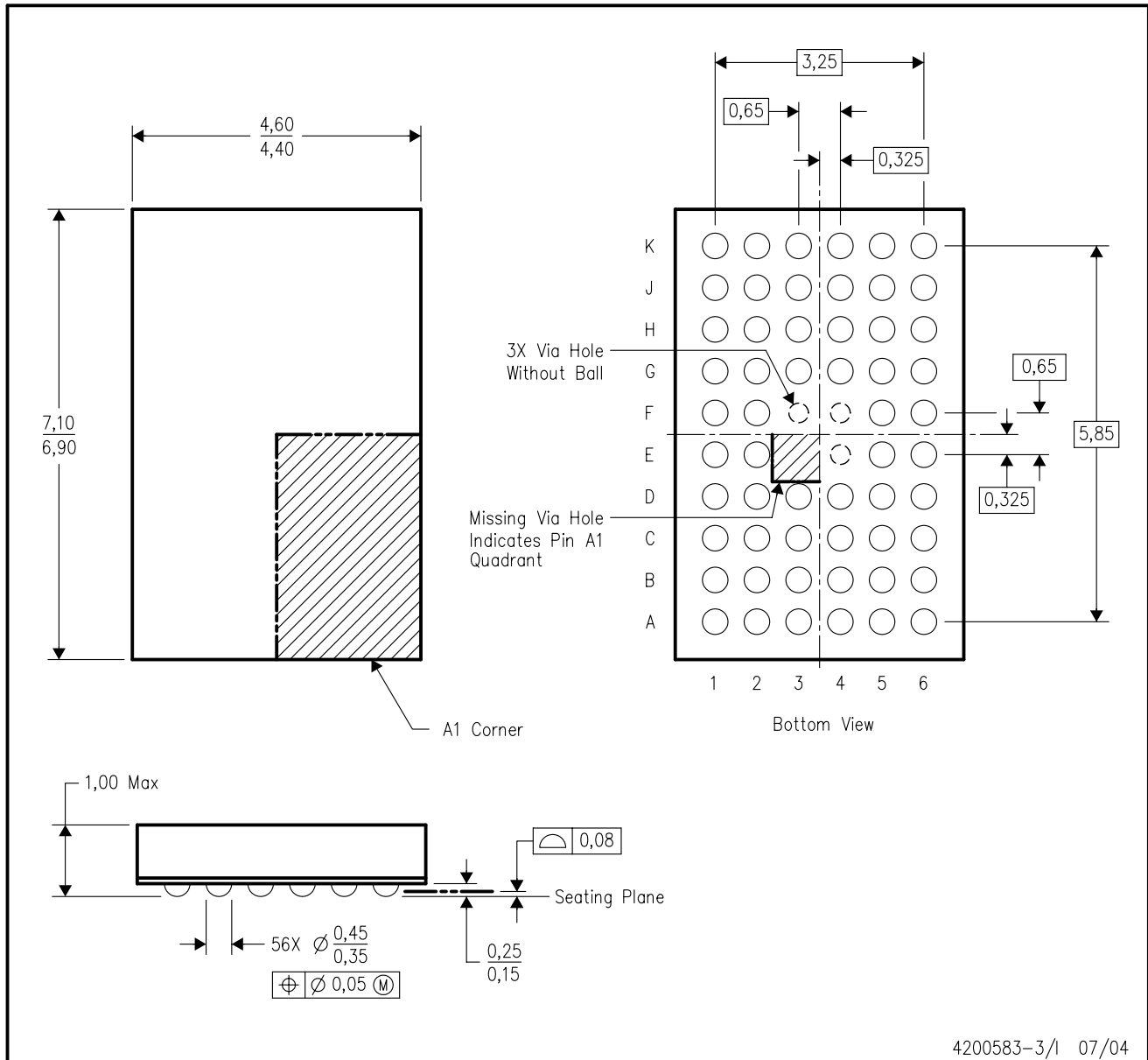
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4200583-3/1 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265