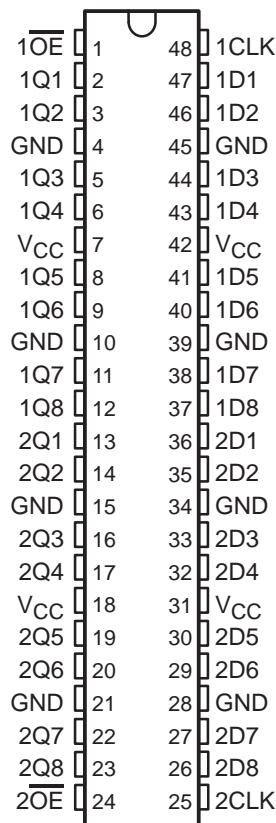


SN54ALVTH16374, SN74ALVTH16374 2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- **State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **High Drive (–24/24 mA at 2.5-V and –32/64 mA at 3.3-V V_{CC})**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **High-Impedance State During Power Up and Power Down Prevents Driver Conflict**
- **Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating**
- **Auto3-State Eliminates Bus Current Loading When Output Exceeds $V_{CC} + 0.5$ V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

SN54ALVTH16374 . . . WD PACKAGE
SN74ALVTH16374 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'ALVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the flip-flops store the logic levels set up at the data (D) inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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 **TEXAS
INSTRUMENTS**

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SN54ALVTH16374, SN74ALVTH16374

2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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description (continued)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ALVTH16374 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALVTH16374 is characterized for operation from -40°C to 85°C .

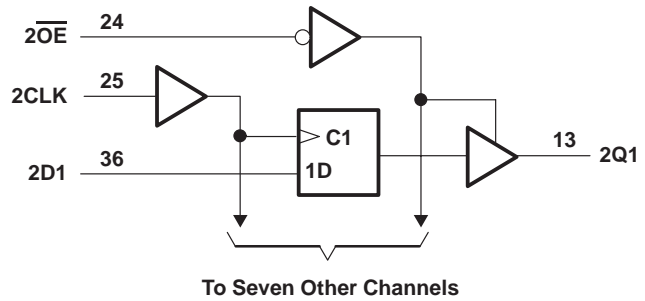
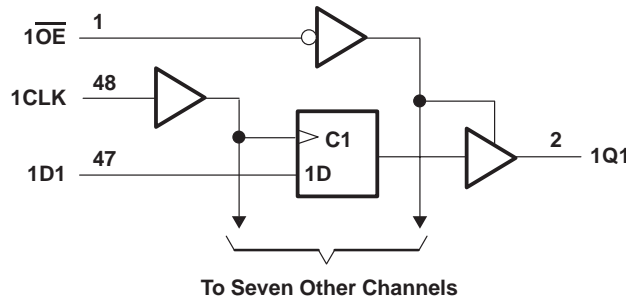
FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

SN54ALVTH16374, SN74ALVTH16374 2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to 7 V
Output current in the low state, I_{OL} : SN54ALVTH16374	96 mA
SN74ALVTH16374	128 mA
Output current in the high state, I_{OH} : SN54ALVTH16374	-48 mA
SN74ALVTH16374	-64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	89°C/W
DGV package	93°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (see Note 3)

		SN54ALVTH16374			SN74ALVTH16374			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	2.3		2.7	2.3		2.7	V
V_{IH}	High-level input voltage	1.7			1.7			V
V_{IL}	Low-level input voltage			0.7			0.7	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			-6			-8	mA
I_{OL}	Low-level output current			6			8	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1 \text{ kHz}$			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
	Outputs enabled							
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s}/\text{V}$
T_A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54ALVTH16374, SN74ALVTH16374
2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

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recommended operating conditions, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Note 3)

		SN54ALVTH16374			SN74ALVTH16374			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	3		3.6	3		3.6	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0	V_{CC}	5.5	0	V_{CC}	5.5	V
I_{OH}	High-level output current			-24			-32	mA
I_{OL}	Low-level output current			24			32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{ kHz}$			48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
T_A	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ALVTH16374, SN74ALVTH16374 2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN54ALVTH16374		SN74ALVTH16374		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V_{IK}		$V_{CC} = 2.3 \text{ V}$, $I_I = -18 \text{ mA}$	-1.2		-1.2		V	
V_{OH}		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$		$V_{CC}-0.2$		V	
		$V_{CC} = 2.3 \text{ V}$	1.8		1.8			
V_{OL}		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$, $I_{OL} = 100 \mu\text{A}$	0.2		0.2		V	
		$V_{CC} = 2.3 \text{ V}$	$I_{OL} = 6 \text{ mA}$	0.4				
			$I_{OL} = 8 \text{ mA}$			0.4		
			$I_{OL} = 18 \text{ mA}$	0.5				
			$I_{OL} = 24 \text{ mA}$			0.5		
I_I	Control inputs	$V_{CC} = 2.7 \text{ V}$, $V_I = V_{CC} \text{ or GND}$	± 1		± 1		μA	
		$V_{CC} = 0 \text{ or } 2.7 \text{ V}$, $V_I = 5.5 \text{ V}$	10		10			
	Data inputs	$V_{CC} = 2.7 \text{ V}$	$V_I = 5.5 \text{ V}$	10		10		
			$V_I = V_{CC}$	1		1		
		$V_I = 0$	-5		-5			
I_{off}		$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$			± 100		μA	
I_{BHL}^\ddagger		$V_{CC} = 2.3 \text{ V}$, $V_I = 0.7 \text{ V}$	115		115		μA	
I_{BHH}^\S		$V_{CC} = 2.3 \text{ V}$, $V_I = 1.7 \text{ V}$	-10		-10		μA	
I_{BHLO}^\P		$V_{CC} = 2.7 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$	300		300		μA	
$I_{BHHO}^\#$		$V_{CC} = 2.7 \text{ V}$, $V_I = 0 \text{ to } V_{CC}$	-300		-300		μA	
I_{EX}^\parallel		$V_{CC} = 2.3 \text{ V}$, $V_O = 5.5 \text{ V}$	125		125		μA	
$I_{OZ(PU/PD)}^*$		$V_{CC} \leq 1.2 \text{ V}$, $V_O = 0.5 \text{ V to } V_{CC}$, $V_I = \text{GND or } V_{CC}$, $\overline{OE} = \text{don't care}$	± 100		± 100		μA	
I_{OZH}		$V_{CC} = 2.7 \text{ V}$	5		5		μA	
I_{OZL}		$V_{CC} = 2.7 \text{ V}$	-5		-5		μA	
I_{CC}		$V_{CC} = 2.7 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high	0.04	0.1	0.04	0.1	mA
			Outputs low	2.3	4.5	2.3	4.5	
			Outputs disabled	0.04	0.1	0.04	0.1	
C_i		$V_{CC} = 2.5 \text{ V}$, $V_I = 2.5 \text{ V or } 0$	3.5		3.5		pF	
C_o		$V_{CC} = 2.5 \text{ V}$, $V_O = 2.5 \text{ V or } 0$	6		6		pF	

† All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

* High-impedance state during power up or power down

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2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALVTH16374		SN74ALVTH16374		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 3 \text{ V}$, $I_I = -18 \text{ mA}$		-1.2		-1.2		V	
V_{OH}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V	
	$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2		2			
V_{OL}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, $I_{OL} = 100 \mu\text{A}$		0.2		0.2		V	
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$			0.4			
		$I_{OL} = 24 \text{ mA}$	0.5					
		$I_{OL} = 32 \text{ mA}$			0.5			
		$I_{OL} = 48 \text{ mA}$	0.55					
		$I_{OL} = 64 \text{ mA}$			0.55			
I_I	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ or GND	± 1		± 1		μA	
		$V_{CC} = 0$ or 3.6 V , $V_I = 5.5 \text{ V}$	10		10			
	Data inputs	$V_{CC} = 3.6 \text{ V}$	$V_I = 5.5 \text{ V}$	10		10		
			$V_I = V_{CC}$	1		1		
		$V_I = 0$	-5		-5			
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V			± 100		μA	
I_{BHL}^\ddagger	$V_{CC} = 3 \text{ V}$,	$V_I = 0.8 \text{ V}$	75		75		μA	
I_{BHH}^\S	$V_{CC} = 3 \text{ V}$,	$V_I = 2 \text{ V}$	-75		-75		μA	
I_{BHLO}^\P	$V_{CC} = 3.6 \text{ V}$,	$V_I = 0$ to V_{CC}	500		500		μA	
$I_{BHHO}^\#$	$V_{CC} = 3.6 \text{ V}$,	$V_I = 0$ to V_{CC}	-500		-500		μA	
I_{EX}^\parallel	$V_{CC} = 3 \text{ V}$,	$V_O = 5.5 \text{ V}$	125		125		μA	
$I_{OZ(PU/PD)}^\star$	$V_{CC} \leq 1.2 \text{ V}$, $V_O = 0.5 \text{ V}$ to V_{CC} , $V_I = \text{GND}$ or V_{CC} , $\overline{OE} = \text{don't care}$		± 100		± 100		μA	
I_{OZH}	$V_{CC} = 3.6 \text{ V}$	$V_O = 3 \text{ V}$, $V_I = 0.8 \text{ V}$ or 2 V	5		5		μA	
I_{OZL}	$V_{CC} = 3.6 \text{ V}$	$V_O = 0.5 \text{ V}$, $V_I = 0.8 \text{ V}$ or 2 V	-5		-5		μA	
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high	0.07	0.1	0.07	0.1	mA	
		Outputs low	3.2	5	3.2	5		
		Outputs disabled	0.07	0.1	0.07	0.1		
ΔI_{CC}^\square	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND		0.4		0.4		mA	
C_i	$V_{CC} = 3.3 \text{ V}$,	$V_I = 3.3 \text{ V}$ or 0	3.5		3.5		pF	
C_o	$V_{CC} = 3.3 \text{ V}$,	$V_O = 3.3 \text{ V}$ or 0	6		6		pF	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

|| Current into an output in the high state when $V_O > V_{CC}$

* High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54ALVTH16374, SN74ALVTH16374 2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

		SN54ALVTH16374		SN74ALVTH16374		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	150		150		MHz
t_w	Pulse duration, CLK high or low	1.5		1.5		ns
t_{su}	Setup time, data before CLK \uparrow	Data high	1.1	1		ns
		Data low	1.4	1.3		
t_h	Hold time, data after CLK \uparrow	Data high	0.6	0.5		ns
		Data low	0.9	0.8		

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 2)

		SN54ALVTH16374		SN74ALVTH16374		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	250		250		MHz
t_w	Pulse duration, CLK high or low	1.5		1.5		ns
t_{su}	Setup time, data before CLK \uparrow	Data high	1.1	1		ns
		Data low	1.6	1.5		
t_h	Hold time, data after CLK \uparrow	Data high	0.6	0.5		ns
		Data low	1.1	1		

switching characteristics over recommended operating free-air temperature range, $C_L = 30\text{ pF}$, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16374		SN74ALVTH16374		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{PLH}	CLK	Q	1.4	3.9	1.5	3.8	ns
t_{PHL}			1.4	3.9	1.5	3.8	
t_{PZH}	$\overline{\text{OE}}$	Q	1	4.2	1	4.1	ns
t_{PZL}			1	3.8	1	3.7	
t_{PHZ}	$\overline{\text{OE}}$	Q	1.7	4.3	1.8	4.2	ns
t_{PLZ}			1	3.5	1	3.4	

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16374		SN74ALVTH16374		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			250		250		MHz
t_{PLH}	CLK	Q	1	3.4	1	3.2	ns
t_{PHL}			1	3.3	1	3.2	
t_{PZH}	$\overline{\text{OE}}$	Q	1	3.9	1	3.8	ns
t_{PZL}			1	3.4	1	3.3	
t_{PHZ}	$\overline{\text{OE}}$	Q	1	4.7	1	4.6	ns
t_{PLZ}			1	4.4	1	4.2	

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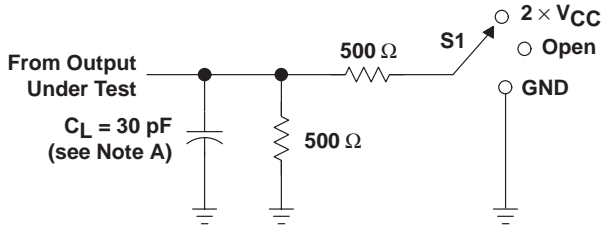


SN54ALVTH16374, SN74ALVTH16374
2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
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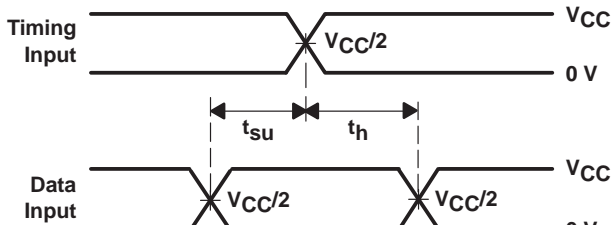
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

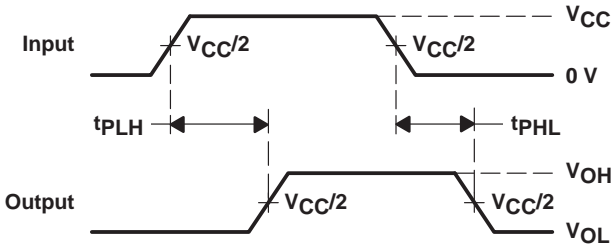


LOAD CIRCUIT

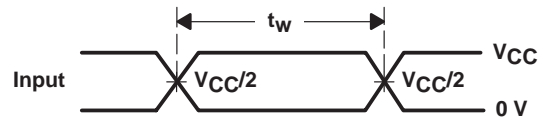
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



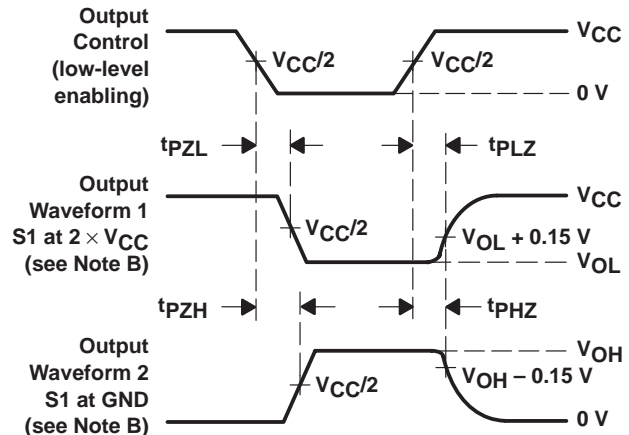
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

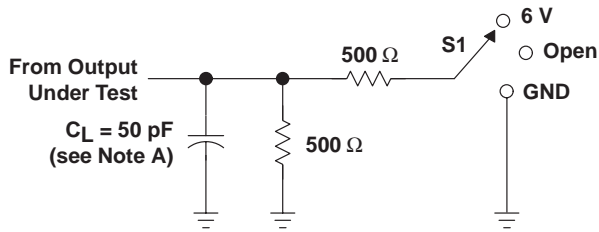
Figure 1. Load Circuit and Voltage Waveforms

SN54ALVTH16374, SN74ALVTH16374
2.5-V/3.3-V 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCES068F – JUNE 1996 – REVISED JANUARY 1999

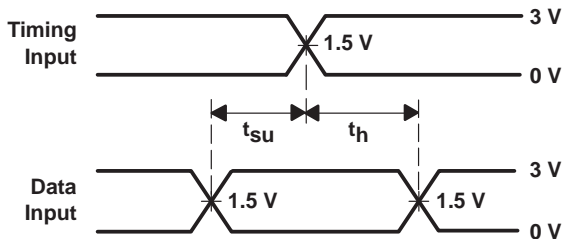
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

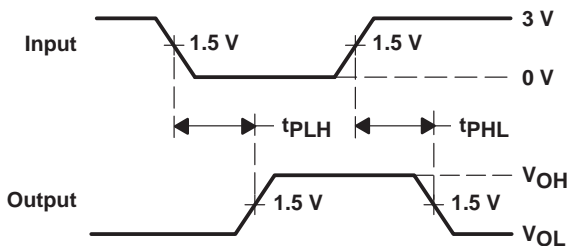


LOAD CIRCUIT

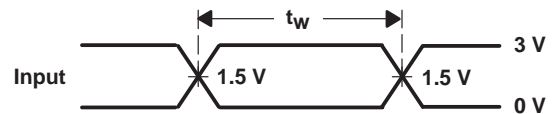
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



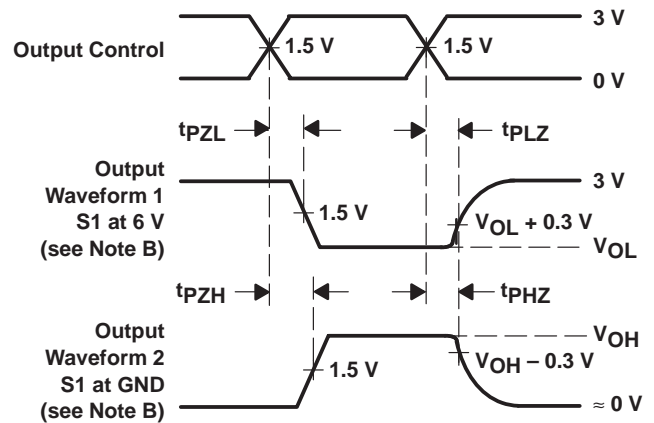
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVTH16374ZQLR	ACTIVE	VFPGA	ZQL	56	1000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74ALVTH16374DL	ACTIVE	SSOP	DL	48	25	None	CU NIPDAU	Level-1-235C-UNLIM
SN74ALVTH16374DLR	ACTIVE	SSOP	DL	48	1000	None	CU NIPDAU	Level-1-235C-UNLIM
SN74ALVTH16374GR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74ALVTH16374KR	ACTIVE	VFPGA	GQL	56	1000	None	SNPB	Level-1-240C-UNLIM
SN74ALVTH16374VR	ACTIVE	TVSOP	DGV	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

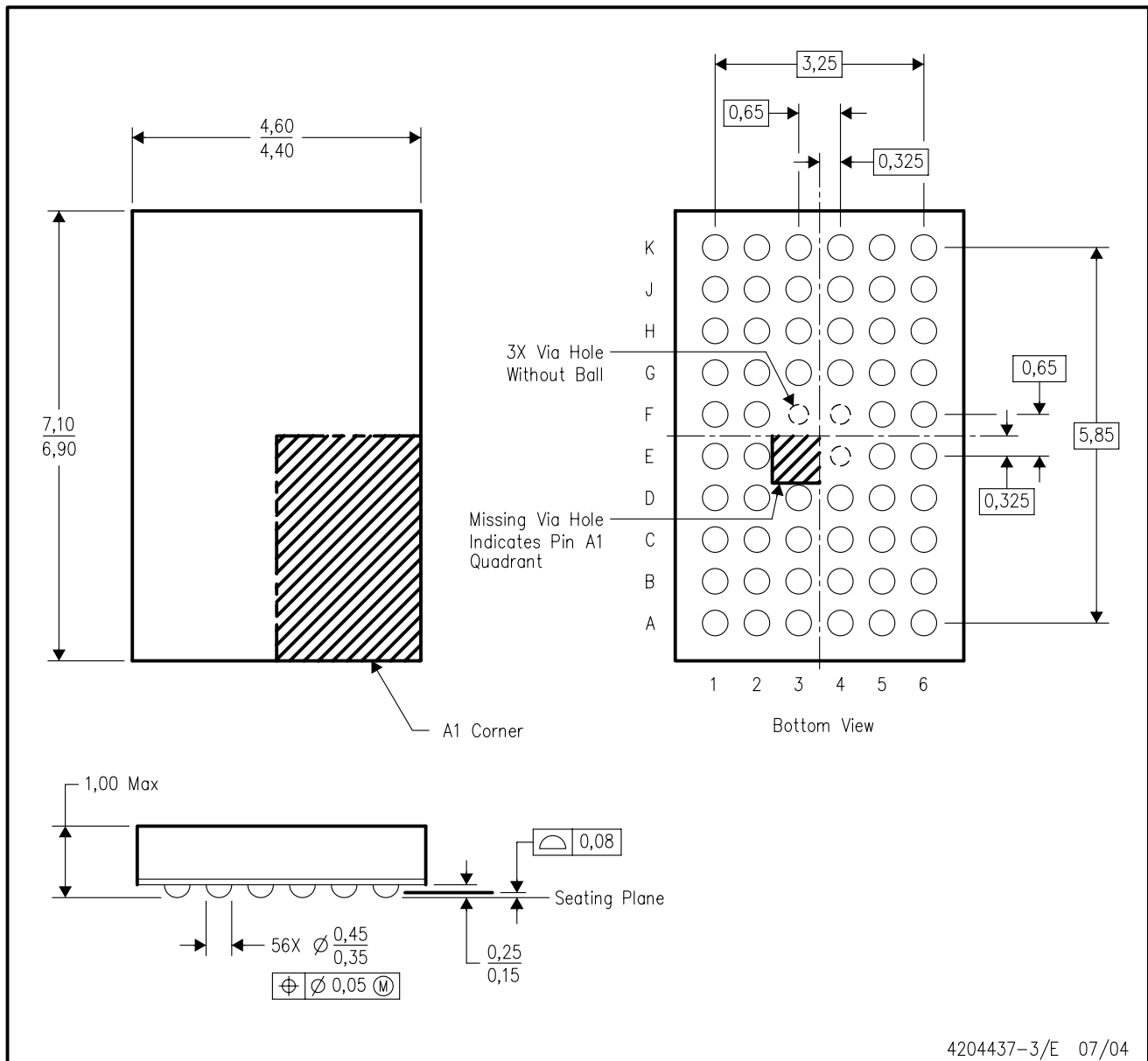
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

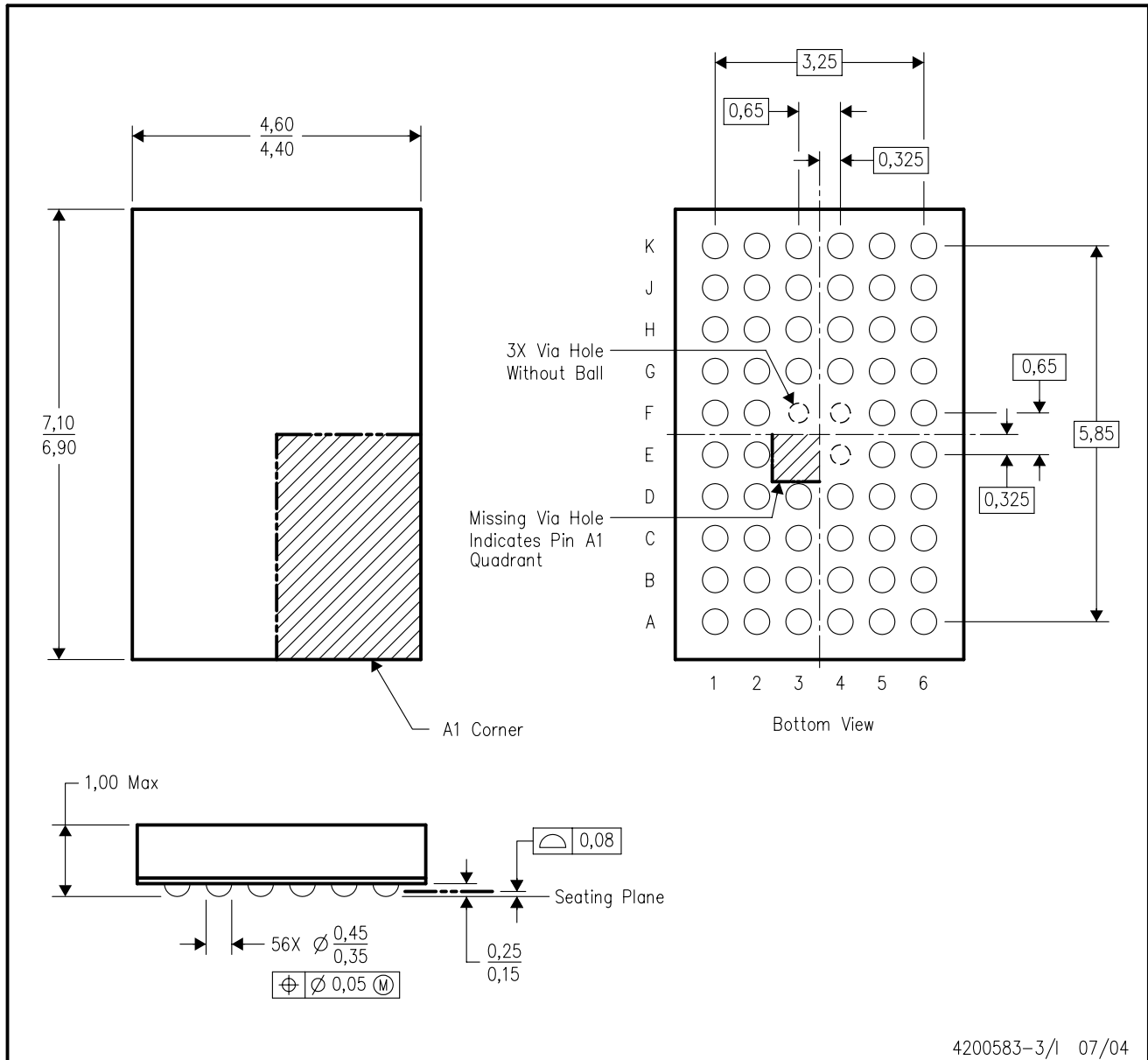


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

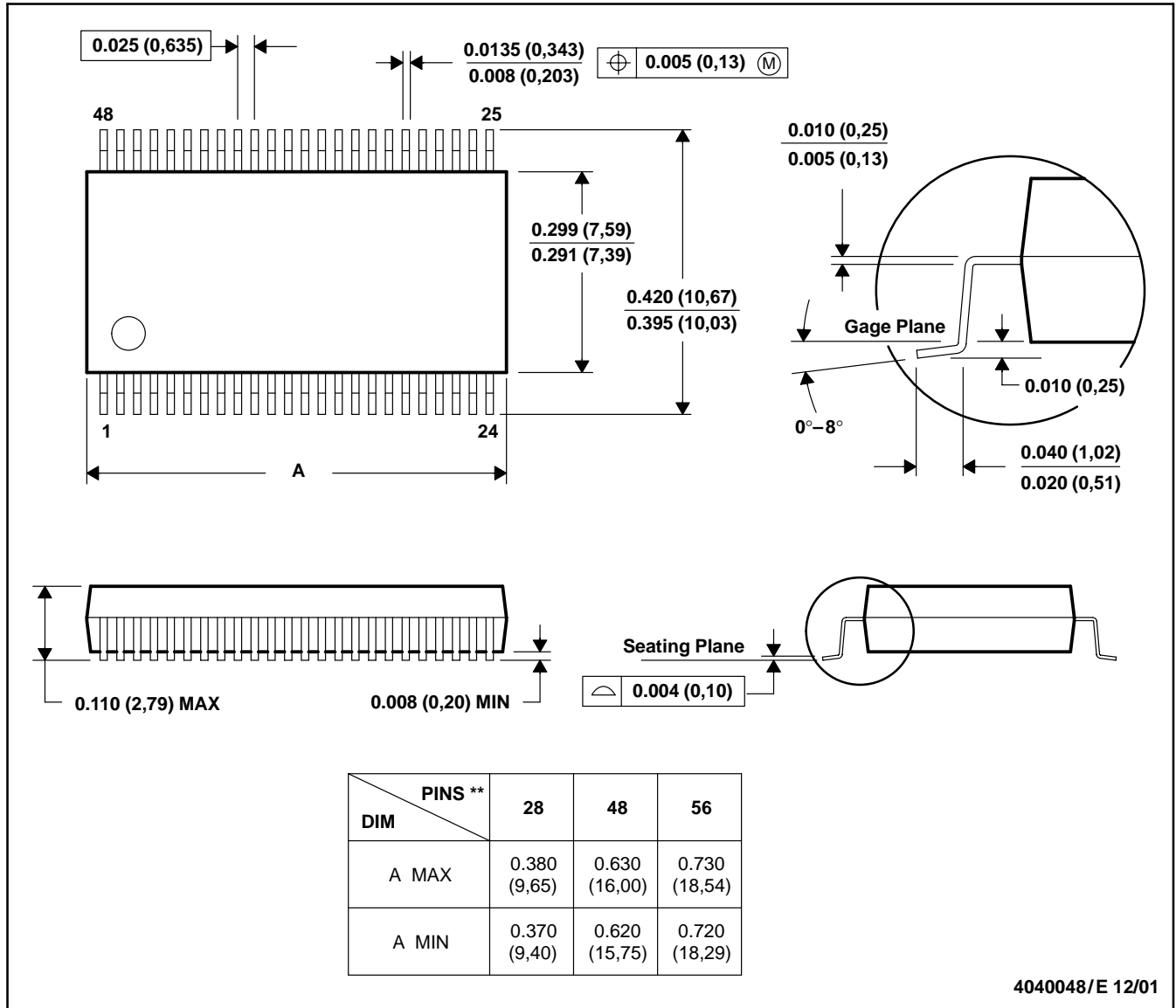


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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