

CD4073B, CD4081B, CD4082B Types

CMOS AND Gates

High-Voltage Types (20-Volt Rating)

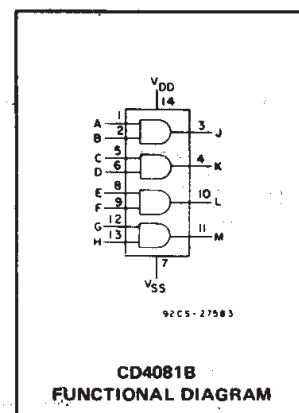
CD4073B Triple 3-Input AND Gate
CD4081B Quad 2-Input AND Gate
CD4082B Dual 4-Input AND Gate

■ CD4073B, CD4081B and CD-4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

The CD4073B, CD4081B, and CD4082B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Medium-Speed Operation – t_{PLH} , $t_{PHL} = 60$ ns (typ.) at $V_{DD} = 10$ V
- 100% tested for quiescent current at 20 V
- Maximum input current of $1 \mu A$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ C$ to $+100^\circ C$ 500mW

For $T_A = +100^\circ C$ to $+125^\circ C$ Derate Linearly at 12mW/ $^\circ C$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

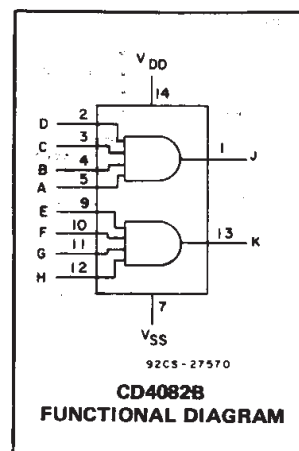
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) $-55^\circ C$ to $+125^\circ C$

STORAGE TEMPERATURE RANGE (T_{stg}) $-65^\circ C$ to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max $+265^\circ C$



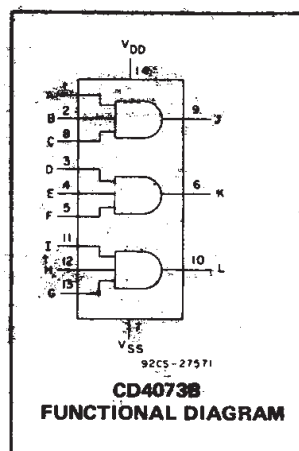
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$, Input $t_r, t_f = 20$ ns, and $C_L = 50$ pF, $R_L = 200$ k Ω

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS	
		V _{DD} Volts	TYP.		MAX.
Propagation Delay Time, t _{PHL} , t _{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t _{THL} , t _{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C _{IN}	Any Input	—	5	7.5	pF



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STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μA
	—	0,10	10	0.5	0.5	15	15	—	0.01	0.5	
	—	0,15	15	1	1	30	30	—	0.01	1	
	—	0,20	20	5	5	150	150	—	0.02	5	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5	—	5	1.5				—	—	1.5	V
	1	—	10	3				—	—	3	
	1.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1.9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

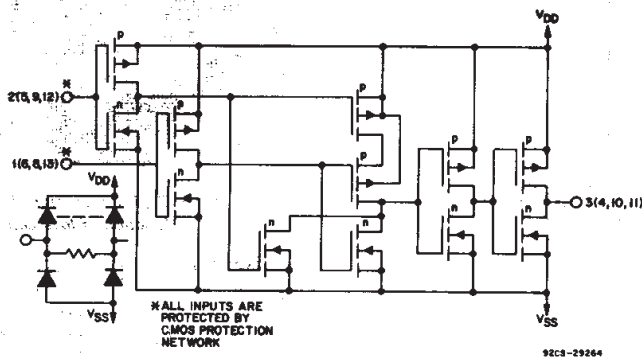


Fig. 1 — Schematic diagram for CD4081B (1 of 4 identical gates).



Fig. 2 — Logic diagram for CD4081B (1 of 4 identical gates).

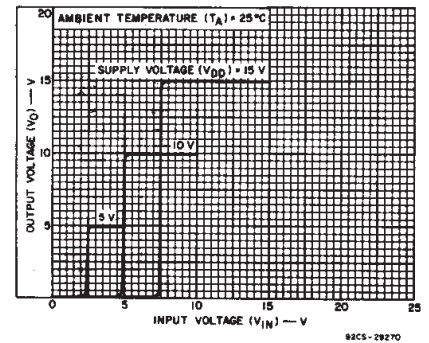


Fig. 3 — Typical voltage transfer characteristics.



Fig. 4 — Typical propagation delay time as a function of load capacitance.

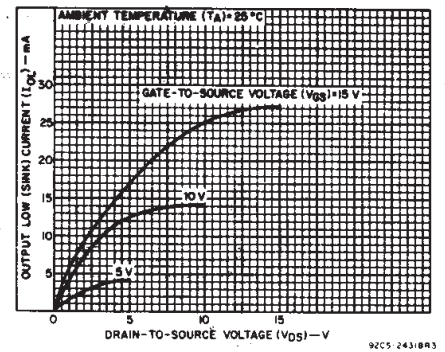


Fig. 5 — Typical output low (sink) current characteristics.

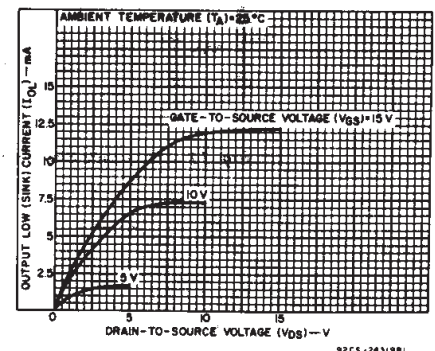


Fig. 6 — Minimum output low (sink) current characteristics.

CD4073B, CD4081B, CD4082B Types



Fig. 7 — Schematic diagram for CD4082B (1 of 2 identical gates).



Fig. 9 — Logic diagram for CD4082B (1 of 2 identical gates).



Fig. 11 — Schematic diagram for CD4073B (1 of 3 identical gates).

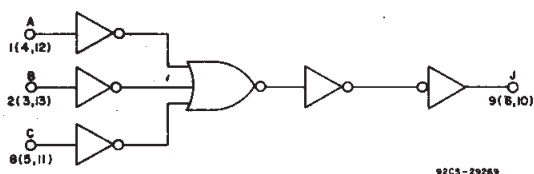


Fig. 13 — Logic diagram for CD4073B (1 of 3 identical gates).



Fig. 8 — Typical output high (source) current characteristics.

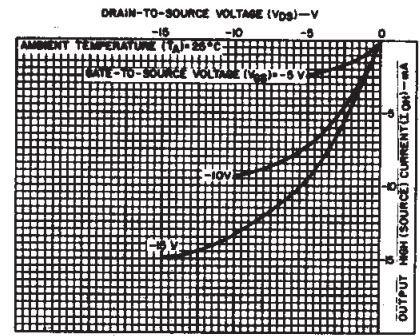


Fig. 10 — Minimum output high (source) current characteristics.

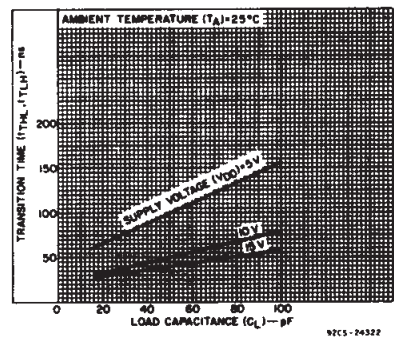


Fig. 12 — Typical transition time as a function of load capacitance

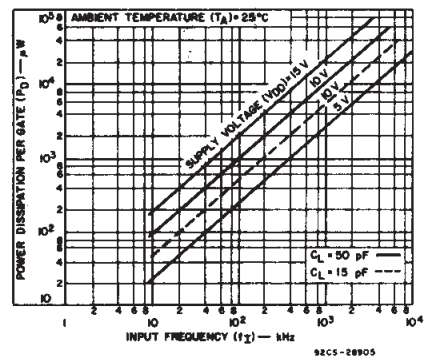


Fig. 14 — Typical dynamic power dissipation per gate as a function of frequency.

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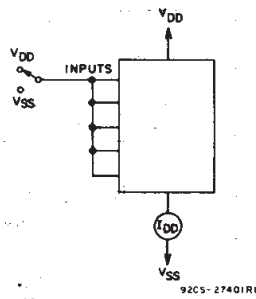


Fig. 15 - Quiescent device current test circuit.



Fig. 16 - Input current test circuit.

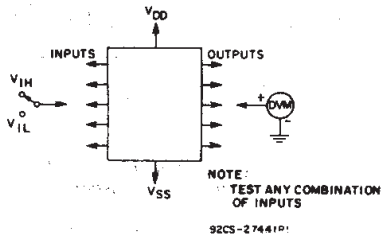
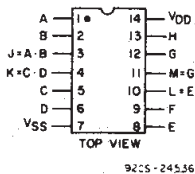
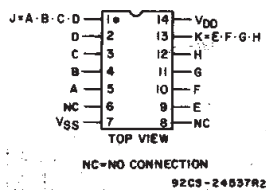


Fig. 17 - Input-voltage test circuit.

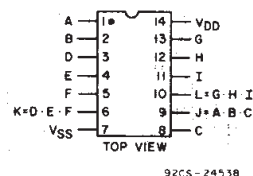
TERMINAL ASSIGNMENTS



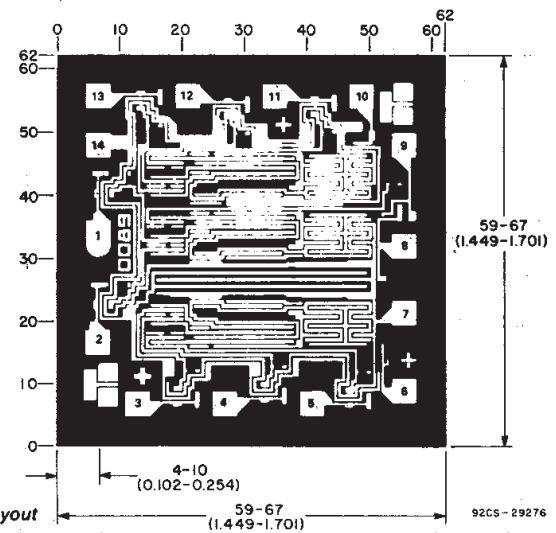
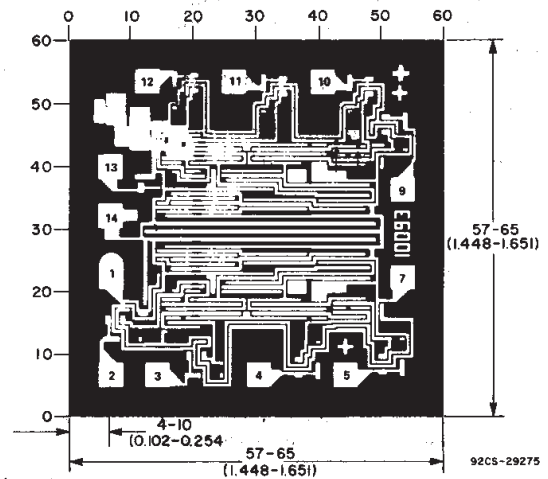
CD4081B



CD4082B



CD4073B



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
7702402CA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
7705102CA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
7705902CA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4073BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4073BF	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4073BF3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4073BM	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4073BM96	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4073BMT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4073BNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4073BPW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4073BPWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4081BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4081BF	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4081BF3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4081BFB3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4081BM	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4081BM96	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4081BMT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4081BNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4081BPW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4081BPWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4082BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4082BF	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4082BF3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4082BM	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4082BM96	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4082BMT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4082BNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4082BPW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4082BPWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
JM38510/17001BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/17002BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/17003BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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