

# DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

SLLS093D – OCTOBER 1972 – REVISED APRIL 1998

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- Short-Circuit Protection of Outputs
- Output Clamp Diodes to Terminate Line Transients
- High-Current Outputs
- Quad Inputs
- Single-Ended or Differential AND/NAND Outputs
- Designed for Use With Dual Differential Drivers SN55182 and SN75182
- Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830

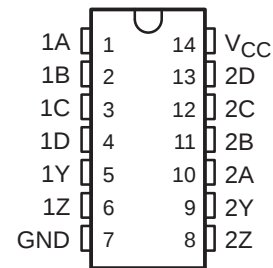
## description

The DS8830, SN55183, and SN75183 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. These devices can be used as TTL expander/phase splitters, because the output stages are similar to TTL totem-pole outputs.

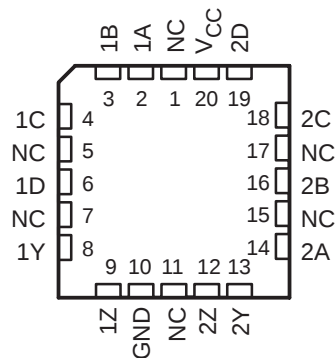
The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55183 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The DS8830 and SN75183 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN55183 . . . J OR W PACKAGE  
SN75183 . . . D OR N PACKAGE  
DS8830 . . . N PACKAGE  
(TOP VIEW)



SN55183 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

**THE DS8830 AND SN55183 ARE  
NOT RECOMMENDED FOR NEW DESIGNS**



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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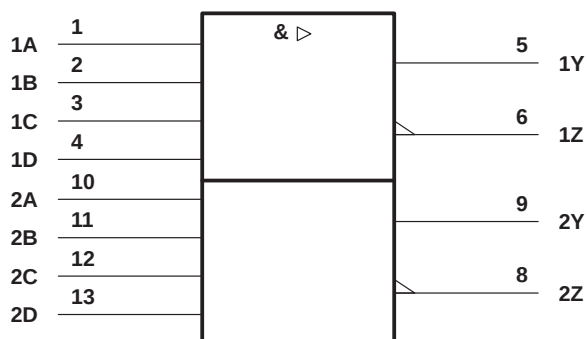
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# DS8830, SN55183, SN75183

## DUAL DIFFERENTIAL LINE DRIVERS

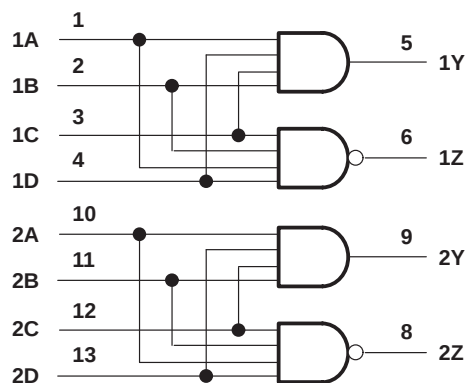
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, N, and W packages.

### logic diagram (positive logic)



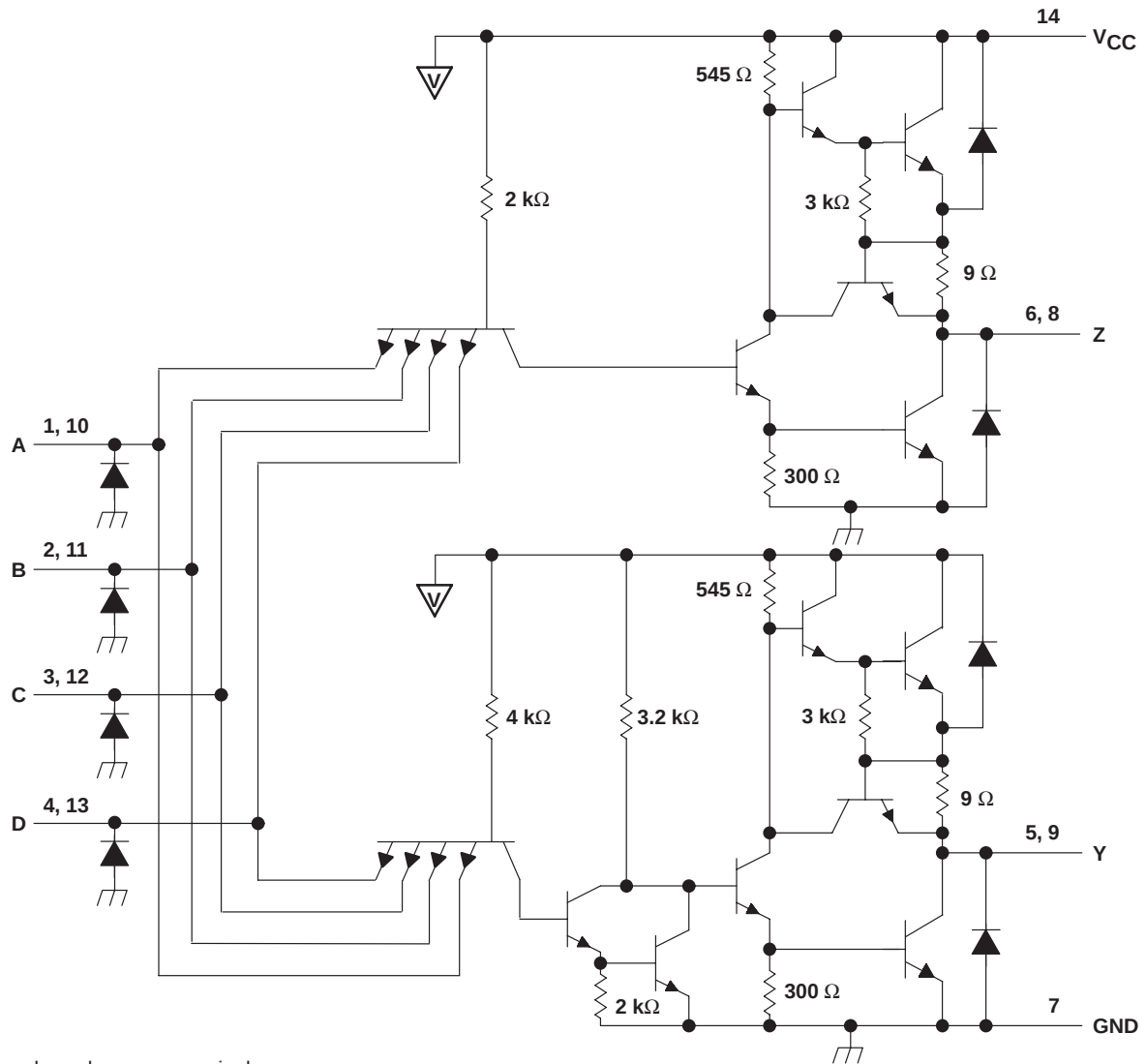
Positive logic:  $y = ABCD$ ,  $Z = \overline{ABCD}$

Pin numbers shown are for the D, J, N, and W packages.

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## schematic (each driver)



Resistor values shown are nominal.  
Pin numbers shown are for the D, J, N, and W packages.

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## DUAL DIFFERENTIAL LINE DRIVERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                              |                              |
|------------------------------------------------------------------------------|------------------------------|
| Supply voltage, $V_{CC}$ (see Note 1)                                        | 7 V                          |
| Input voltage, $V_I$                                                         | 5.5 V                        |
| Duration of output short circuit (see Note 2)                                | 1 s                          |
| Continuous total power dissipation                                           | See Dissipation Rating Table |
| Storage temperature range, $T_{stg}$                                         | –65°C to 150°C               |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | 260°C                        |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package      | 300°C                        |
| Case temperature for 60 seconds, $T_C$ : FK package                          | 260°C                        |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.  
2. Not more than one output should be shorted to ground at any one time.

DISSIPATION RATING TABLE

| PACKAGE         | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 125^\circ\text{C}$<br>POWER RATING |
|-----------------|---------------------------------------------|---------------------------------------------------|------------------------------------------|-------------------------------------------|
| D               | 950 mW                                      | 7.6 mW/°C                                         | 608 mW                                   | –                                         |
| FK <sup>‡</sup> | 1375 mW                                     | 11.0 mW/°C                                        | 880 mW                                   | 275 mW                                    |
| J <sup>‡</sup>  | 1375 mW                                     | 11.0 mW/°C                                        | 880 mW                                   | 275 mW                                    |
| N               | 1150 mW                                     | 9.2 mW/°C                                         | 736 mW                                   | –                                         |
| W <sup>‡</sup>  | 1000 mW                                     | 8.0 mW/°C                                         | 640 mW                                   | 200 mW                                    |

<sup>‡</sup> In the FK, J, and W packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

### recommended operating conditions

|                                       | SN55183 |     |     | DS8830,<br>SN75183 |     |      | UNIT |
|---------------------------------------|---------|-----|-----|--------------------|-----|------|------|
|                                       | MIN     | NOM | MAX | MIN                | NOM | MAX  |      |
| Supply voltage, $V_{CC}$              | 4.5     | 5   | 5.5 | 4.75               | 5   | 5.25 | V    |
| High-level input voltage, $V_{IH}$    | 2       |     |     | 2                  |     |      | V    |
| Low-level input voltage, $V_{IL}$     |         |     | 0.8 |                    |     | 0.8  | V    |
| High-level output current, $I_{OH}$   |         |     | –40 |                    |     | –40  | mA   |
| Low-level output current, $I_{OL}$    |         |     | 40  |                    |     | 40   | mA   |
| Operating free-air temperature, $T_A$ | –55     |     | 125 | 0                  |     | 70   | °C   |



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**electrical characteristics over recommended ranges of  $V_{CC}$  and operating free-air temperature (unless otherwise noted)**

| PARAMETER |                                           |                  | TEST CONDITIONS                                                |                           | MIN | TYP <sup>†</sup> | MAX  | UNIT          |
|-----------|-------------------------------------------|------------------|----------------------------------------------------------------|---------------------------|-----|------------------|------|---------------|
| $V_{OH}$  | High-level output voltage                 | Y (AND) outputs  | $V_{IH} = 2\text{ V}$                                          | $I_{OH} = -0.8\text{ mA}$ | 2.4 |                  |      | V             |
|           |                                           |                  |                                                                | $I_{OH} = -40\text{ mA}$  | 1.8 | 3.3              |      |               |
| $V_{OL}$  | Low-level output voltage                  | Y (AND) outputs  | $V_{IL} = 0.8\text{ V}$                                        | $I_{OL} = 32\text{ mA}$   |     | 0.2              |      | V             |
|           |                                           |                  |                                                                | $I_{OL} = 40\text{ mA}$   |     | 0.22             | 0.4  |               |
| $V_{OH}$  | High-level output voltage                 | Z (NAND) outputs | $V_{IL} = 0.8\text{ V}$                                        | $I_{OH} = -0.8\text{ mA}$ | 2.4 |                  |      | V             |
|           |                                           |                  |                                                                | $I_{OH} = -40\text{ mA}$  | 1.8 | 3.3              |      |               |
| $V_{OL}$  | Low-level output voltage                  | Z (NAND) outputs | $V_{IH} = 2\text{ V}$                                          | $I_{OL} = 32\text{ mA}$   |     | 0.2              |      | V             |
|           |                                           |                  |                                                                | $I_{OL} = 40\text{ mA}$   |     | 0.22             | 0.4  |               |
| $I_{IH}$  | High-level input current                  |                  | $V_{IH} = 2.4\text{ V}$                                        |                           |     |                  | 120  | $\mu\text{A}$ |
| $I_I$     | Input current at maximum input voltage    |                  | $V_{IH} = 5.5\text{ V}$                                        |                           |     |                  | 2    | mA            |
| $I_{IL}$  | Low-level input current                   |                  | $V_{IL} = 0.4\text{ V}$                                        |                           |     |                  | -4.8 | mA            |
| $I_{OS}$  | Short-circuit output current <sup>‡</sup> |                  | $V_{CC} = 5\text{ V}$ , $T_A = 125^\circ\text{C}$ <sup>§</sup> |                           | -40 | -100             | -120 | mA            |
| $I_{CC}$  | Supply current (average per driver)       |                  | $V_{CC} = 5\text{ V}$ , All inputs at 5 V, No load             |                           |     | 10               | 18   | mA            |

<sup>†</sup> All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

<sup>§</sup>  $T_A = 125^\circ\text{C}$  is applicable to SN55183 only.

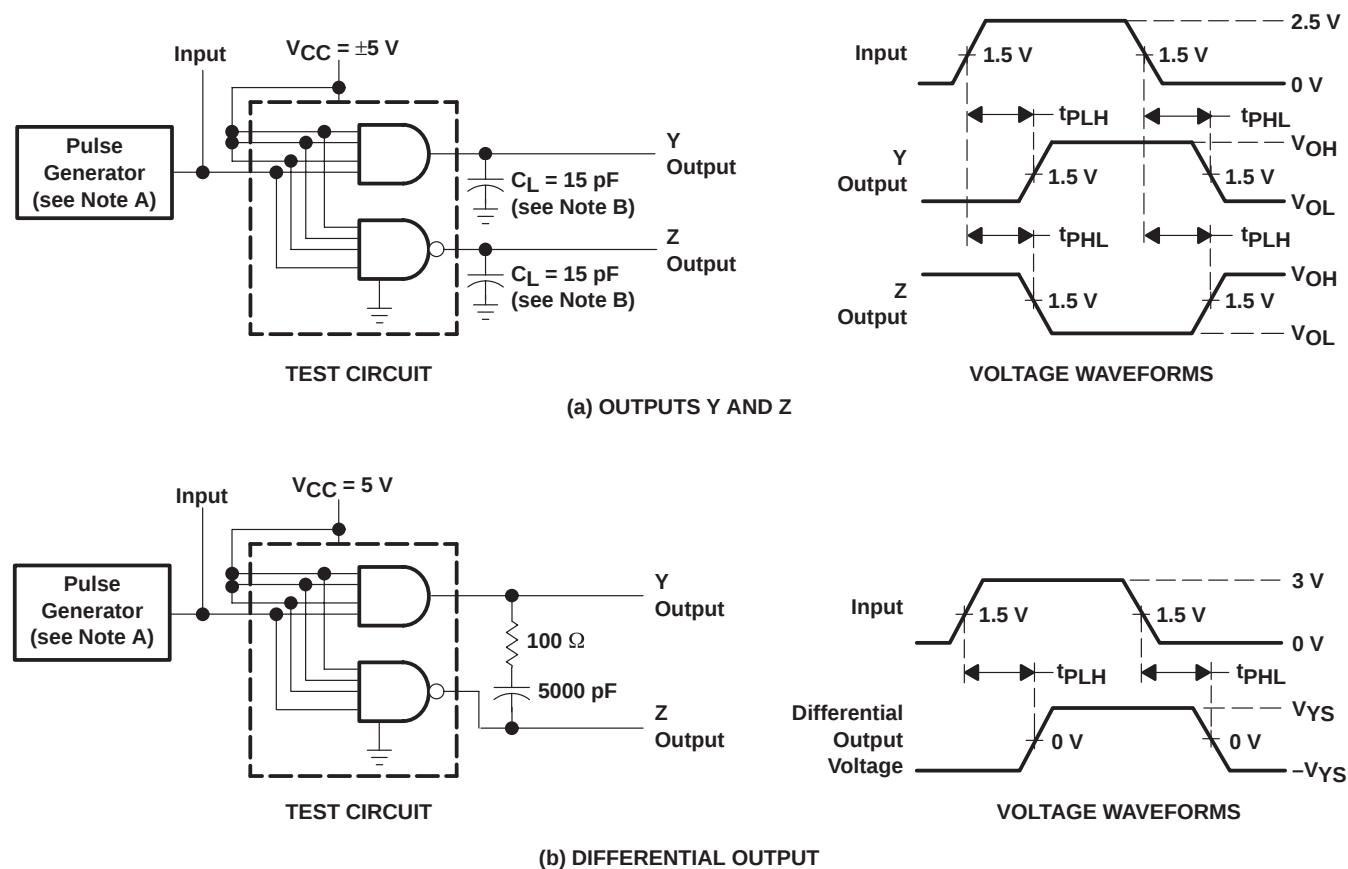
**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

| PARAMETER |                                                                   | TEST CONDITIONS                                                                                      |                                           | MIN | TYP | MAX | UNIT |
|-----------|-------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|-------------------------------------------|-----|-----|-----|------|
| $t_{PLH}$ | Propagation delay time, low- to high-level Y output               | AND gates                                                                                            | $C_L = 15\text{ pF}$ ,<br>See Figure 1(a) |     | 8   | 12  | ns   |
| $t_{PHL}$ | Propagation delay time, high- to low-level Y output               | AND gates                                                                                            | $C_L = 15\text{ pF}$ ,<br>See Figure 1(a) |     | 12  | 18  | ns   |
| $t_{PLH}$ | Propagation delay time, low- to high-level Z output               | NAND gates                                                                                           | $C_L = 15\text{ pF}$ ,<br>See Figure 1(a) |     | 6   | 12  | ns   |
| $t_{PHL}$ | Propagation delay time, high- to low-level Z output               | NAND gates                                                                                           | $C_L = 15\text{ pF}$ ,<br>See Figure 1(a) |     | 6   | 8   | ns   |
| $t_{PLH}$ | Propagation delay time,<br>low- to high-level differential output | Y output with respect to Z output,<br>$R_L = 100\ \Omega$ in series with 5000 pF,<br>See Figure 1(b) |                                           |     | 9   | 16  | ns   |
| $t_{PHL}$ | Propagation delay time,<br>high- to low-level differential output | Y output with respect to Z output,<br>$R_L = 100\ \Omega$ in series with 5000 pF,<br>See Figure 1(b) |                                           |     | 8   | 16  | ns   |

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generators have the following characteristics:  $Z_O = 50\ \Omega$ ,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ ,  $t_W = 0.5\ \mu\text{s}$ ,  $\text{PRR} \leq 1\text{ MHz}$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. Waveforms are monitored on an oscilloscope with  $r_i \geq 1\text{ M}\Omega$ .

Figure 1. Test Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS†

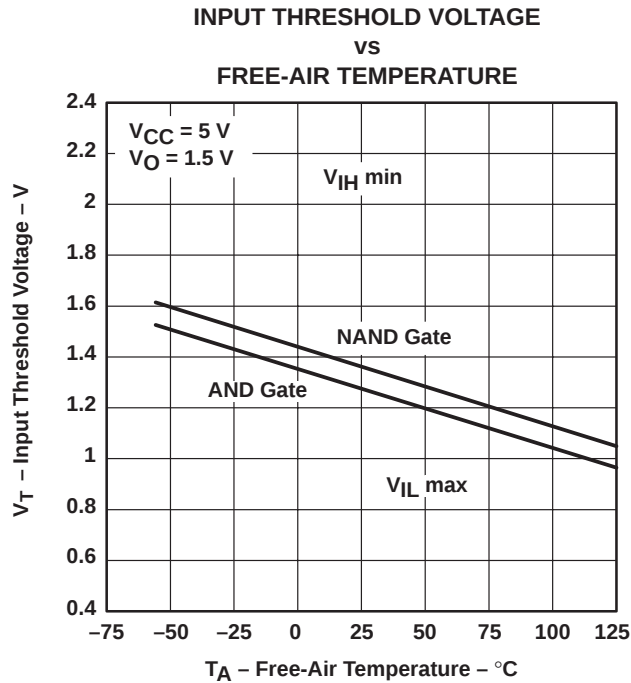


Figure 2

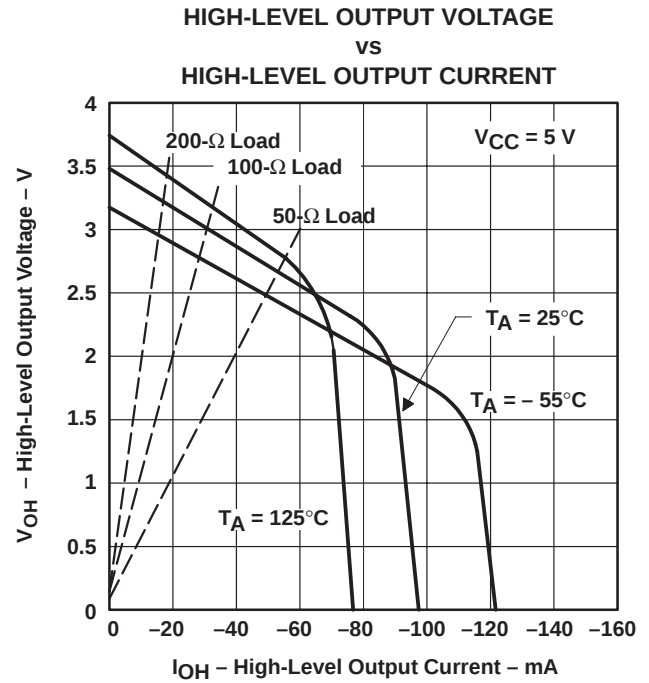


Figure 3

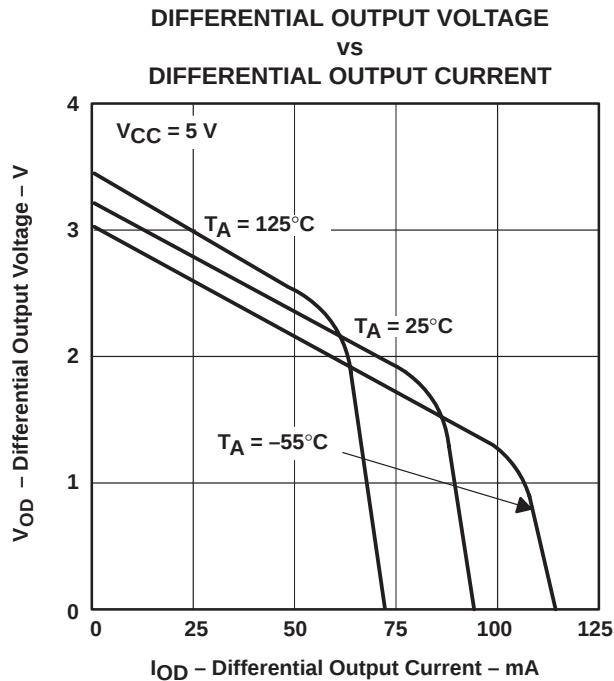


Figure 4

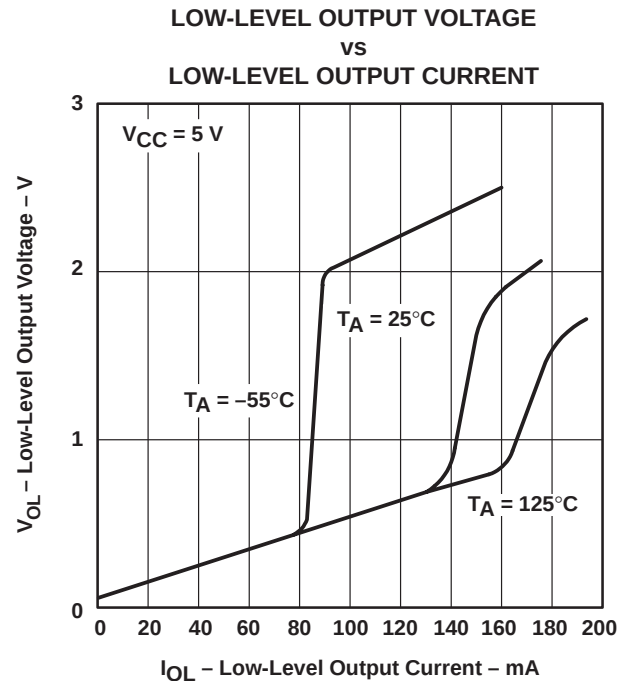


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS†

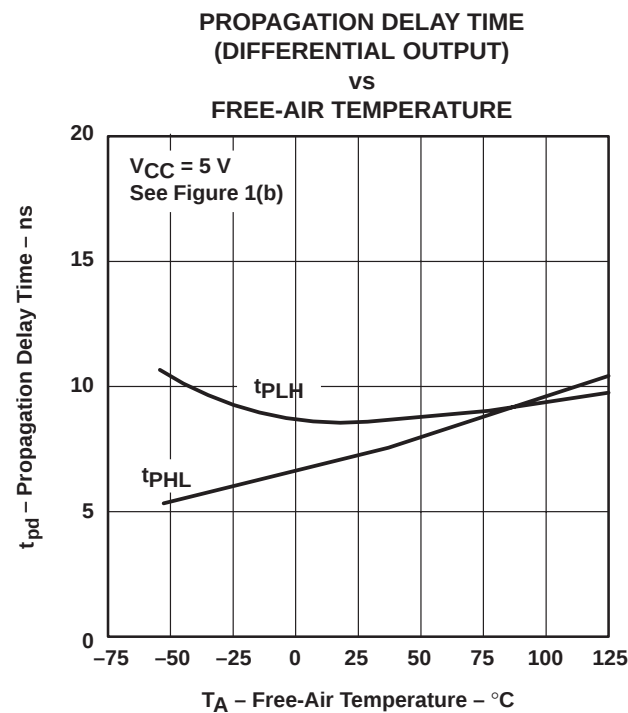


Figure 6

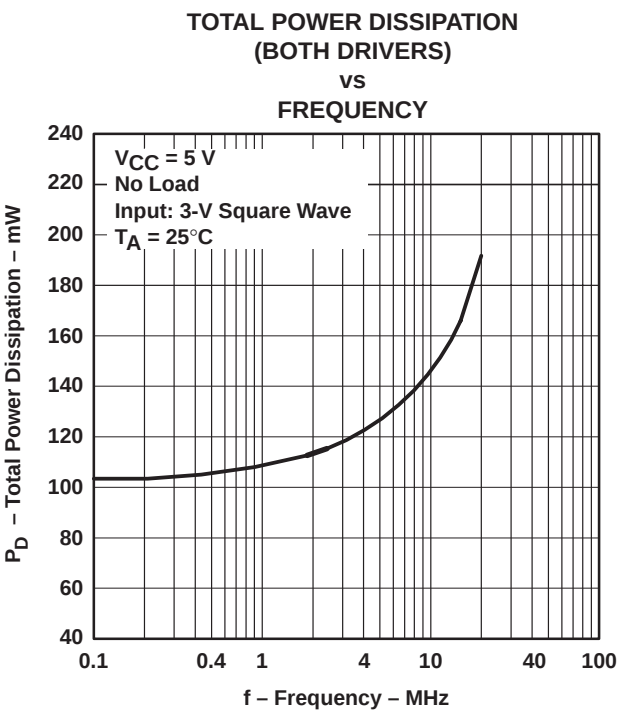
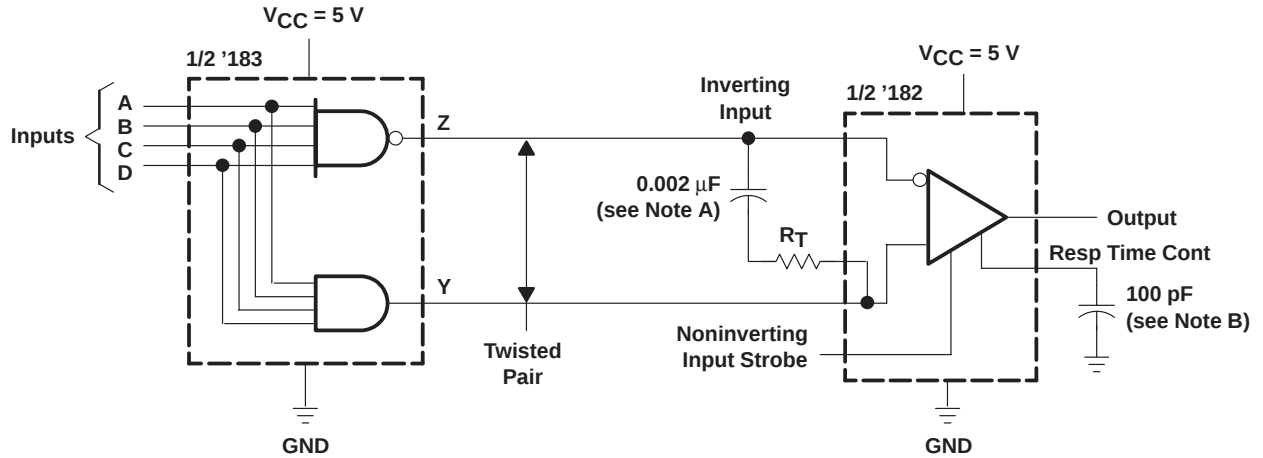


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

## APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let  $f = 5 \text{ MHz}$   
 $C = 0.002 \mu\text{F}$

$$Z_{(\text{circuit})} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(\text{circuit})} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

**Figure 8. Transmission of Digital Data Over Twisted-Pair Line**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup>               |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--------------------------------------------|
| 7900901CA        | ACTIVE                | CDIP         | J               | 14   | 1           | None                    | A42 SNPB         | Level-NC-NC-NC                             |
| 7900901DA        | ACTIVE                | CFP          | W               | 14   | 1           | None                    | A42 SNPB         | Level-NC-NC-NC                             |
| DS8830N          | OBSOLETE              | PDIP         | N               | 14   |             | None                    | Call TI          | Call TI                                    |
| SN55183J         | ACTIVE                | CDIP         | J               | 14   | 1           | None                    | A42 SNPB         | Level-NC-NC-NC                             |
| SN75183D         | ACTIVE                | SOIC         | D               | 14   | 50          | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| SN75183DR        | ACTIVE                | SOIC         | D               | 14   | 2500        | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| SN75183N         | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC                             |
| SN75183NSR       | ACTIVE                | SO           | NS              | 14   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| SNJ55183FK       | ACTIVE                | LCCC         | FK              | 20   | 1           | None                    | POST-PLATE       | Level-NC-NC-NC                             |
| SNJ55183J        | ACTIVE                | CDIP         | J               | 14   | 1           | None                    | A42 SNPB         | Level-NC-NC-NC                             |
| SNJ55183W        | ACTIVE                | CFP          | W               | 14   | 1           | None                    | A42 SNPB         | Level-NC-NC-NC                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

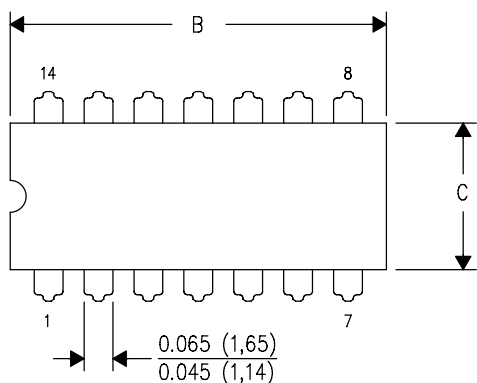
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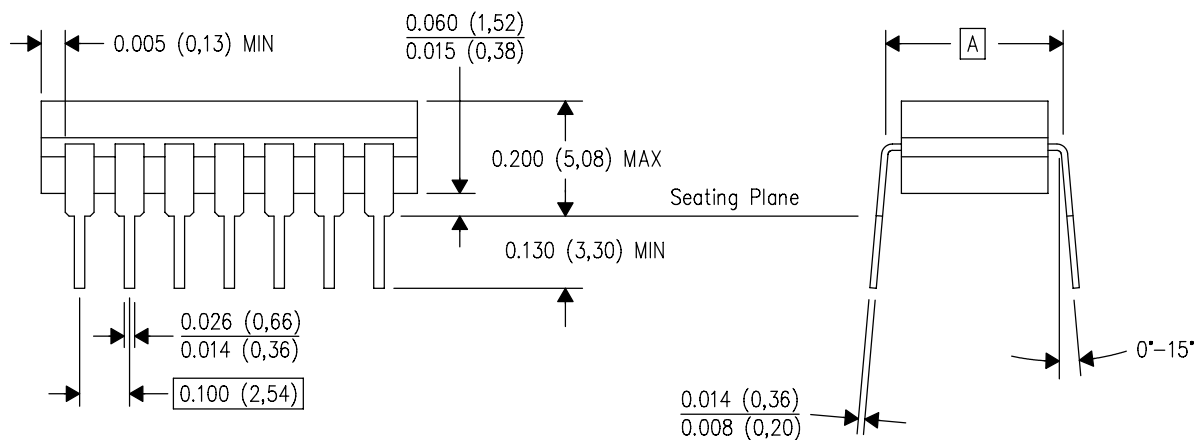
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |

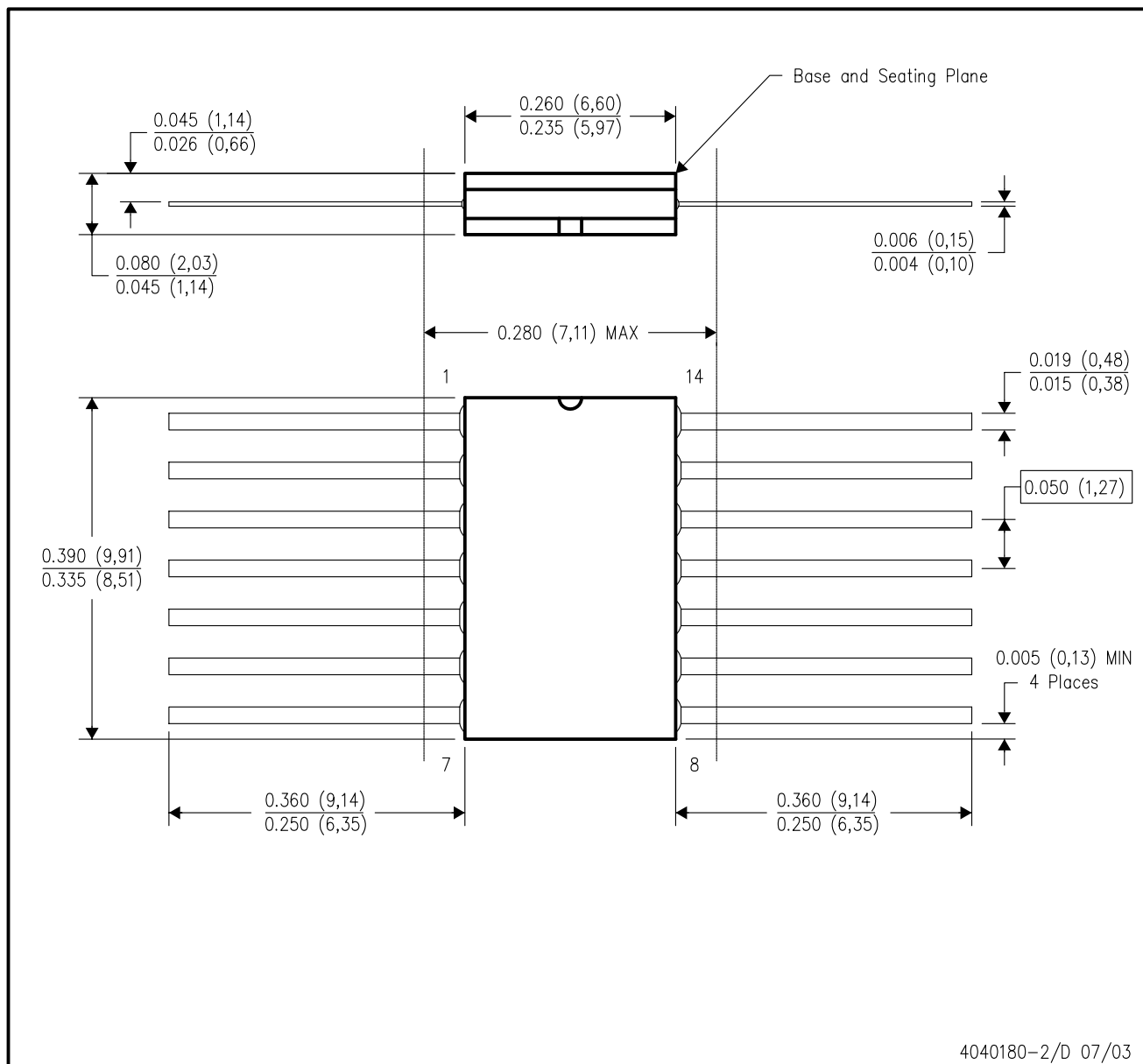


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

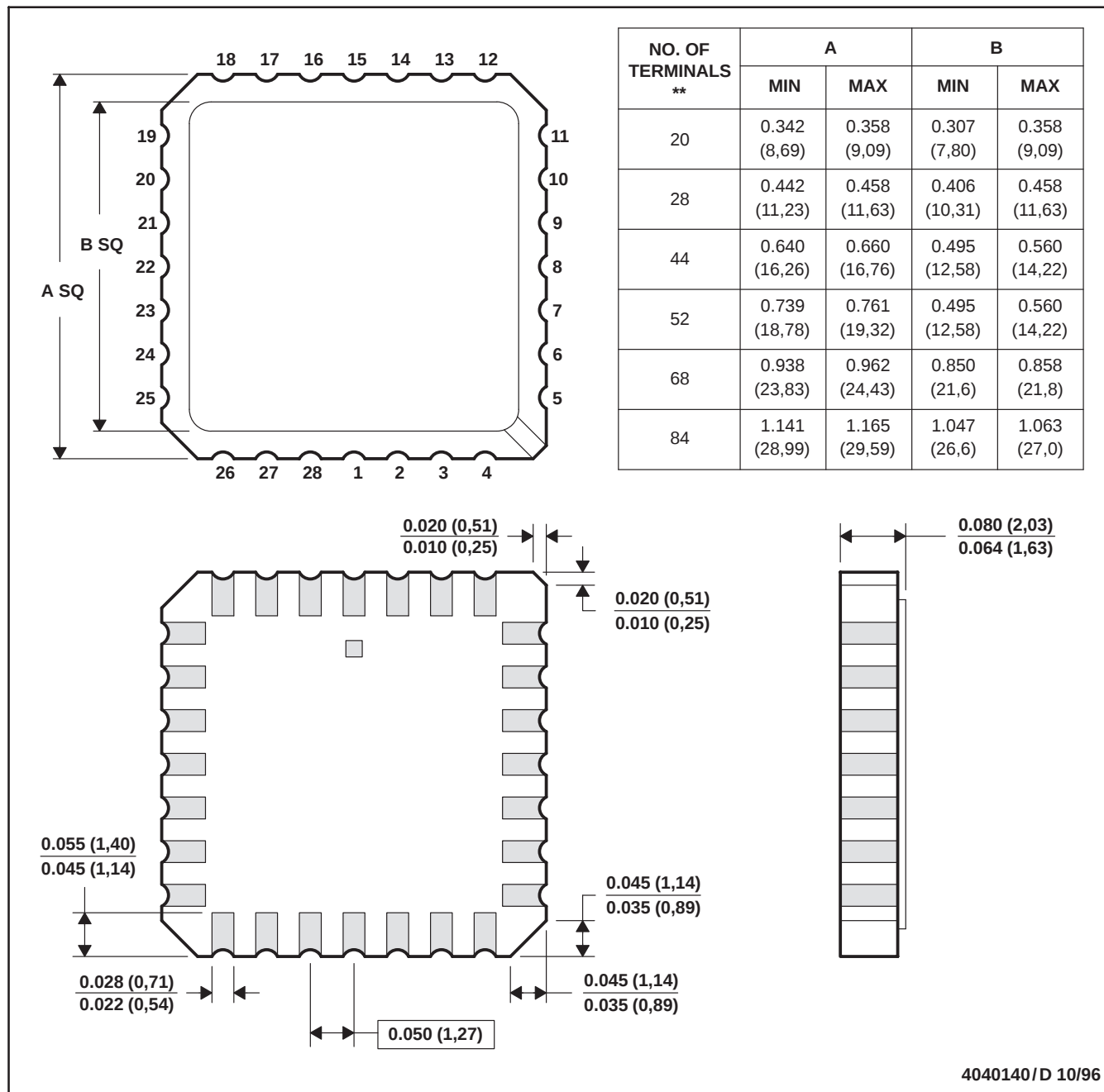


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

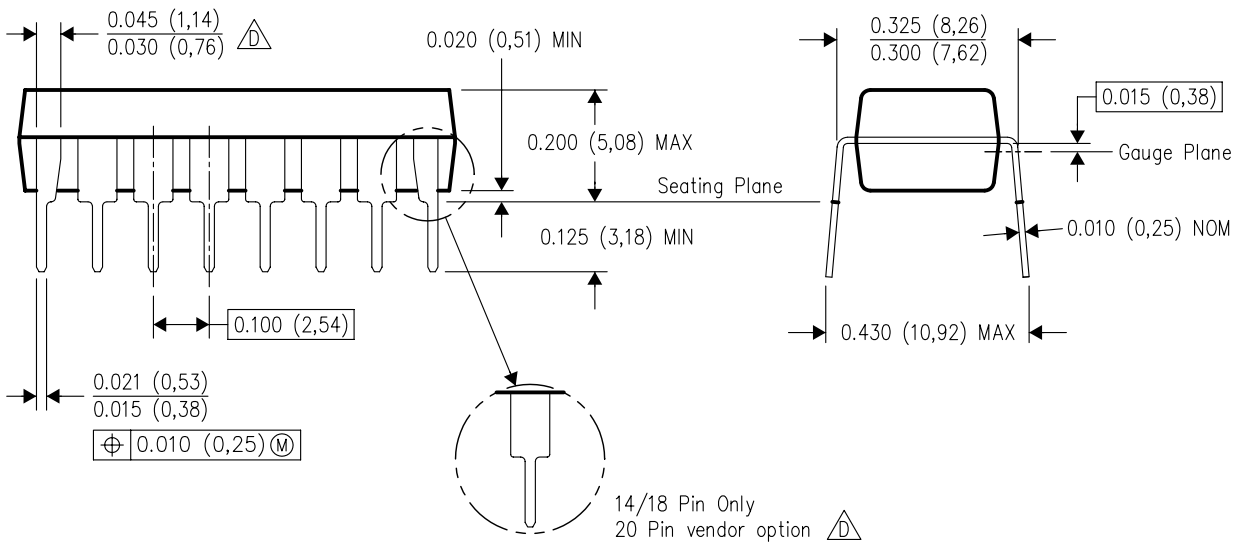
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



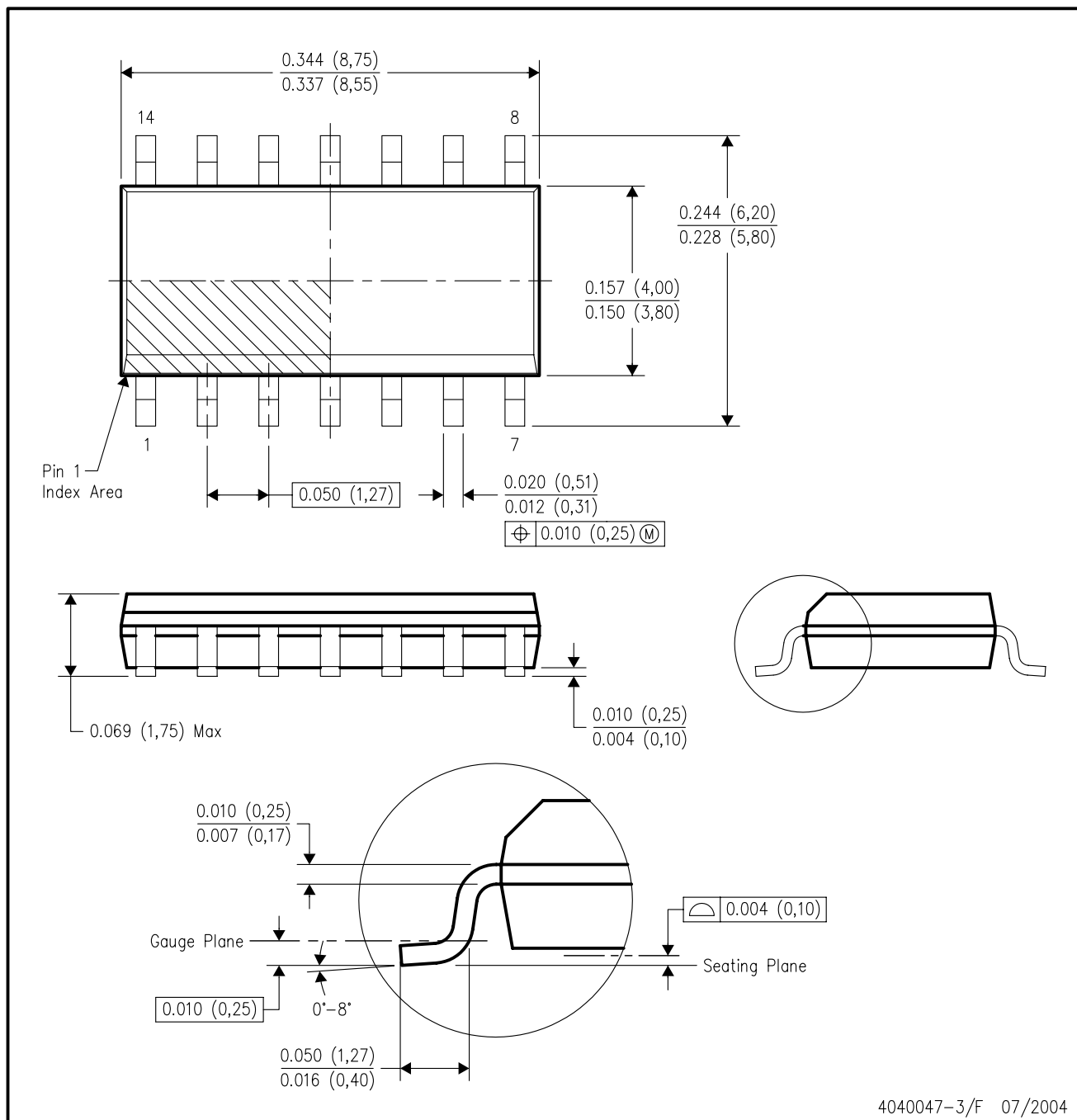
14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G14)

## PLASTIC SMALL-OUTLINE PACKAGE



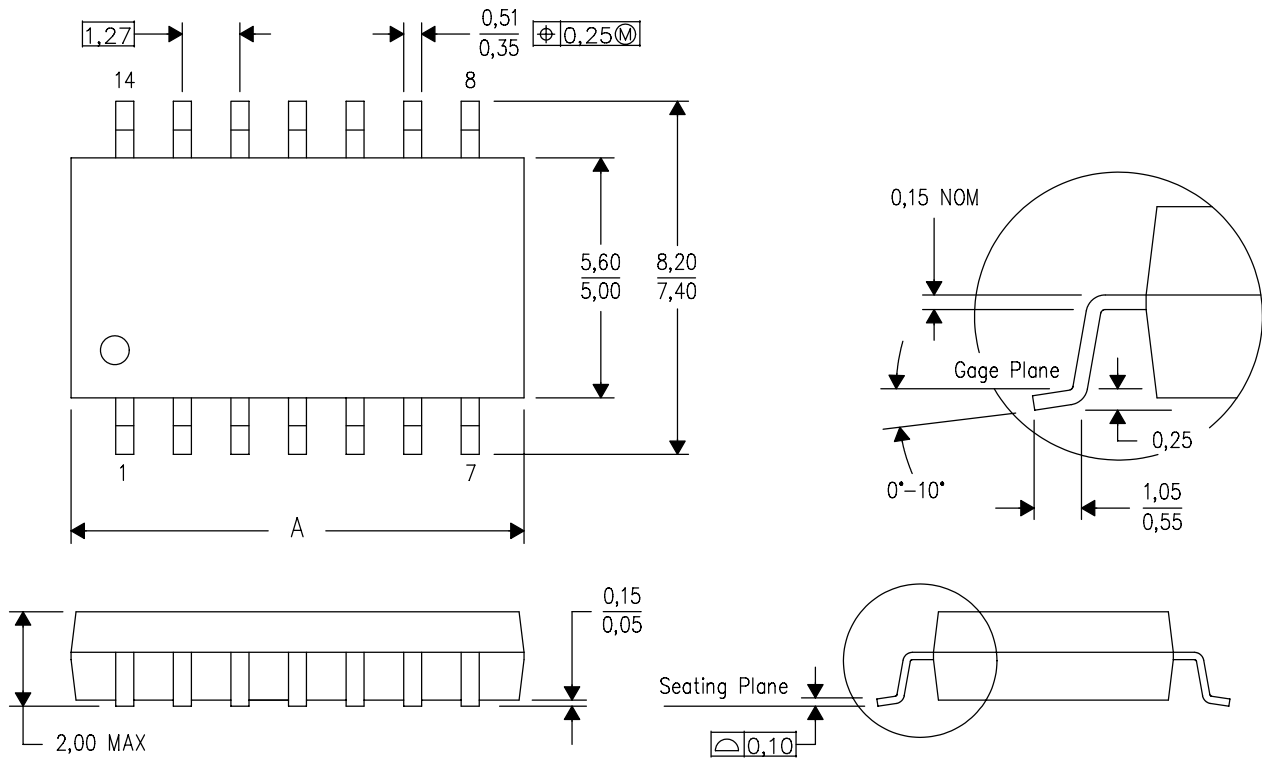
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# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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