

# CMOS Presettable Up/Down Counter

Binary or BCD-Decade

High-Voltage Types (20-Volt Rating)

■ CD4029B consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single **CLOCK**, **CARRY-IN (CLOCK ENABLE)**, **BINARY/DECADE**, **UP/DOWN**, **PRESET ENABLE**, and four individual **JAM** signals. **Q1, Q2, Q3, Q4** and a **CARRY OUT** signal are provided as outputs.

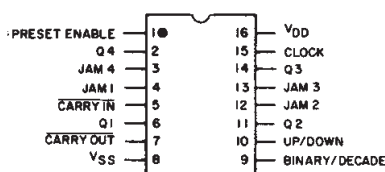
A high **PRESET ENABLE** signal allows information on the **JAM INPUTS** to preset the counter to any state asynchronously with the clock. A low on each **JAM** line, when the **PRESET-ENABLE** signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the **CARRY-IN** and **PRESET ENABLE** signals are low. Advancement is inhibited when the **CARRY-IN** or **PRESET ENABLE** signals are high. The **CARRY-OUT** signal is normally high and goes low when the counter reaches its maximum count in the **UP** mode or the minimum count in the **DOWN** mode provided the **CARRY-IN** signal is low. The **CARRY-IN** signal in the low state can thus be considered a **CLOCK ENABLE**. The **CARRY-IN** terminal must be connected to **VSS** when not in use.

Binary counting is accomplished when the **BINARY/DECADE** input is high; the counter counts in the decade mode when the **BINARY/DECADE** input is low. The counter counts up when the **UP/DOWN** input is high, and down when the **UP/DOWN** input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 17.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

The CD4029B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

CD4029B Terminal Diagram

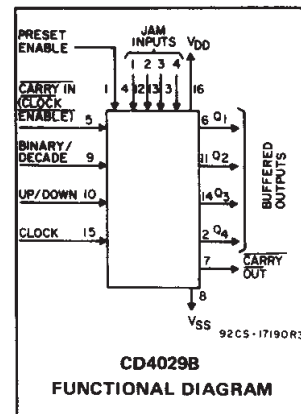


92CS-24472R1

# CD4029B Types

**Features:**

- Medium-speed operation . . . 8 MHz (typ.)  
@  $C_L = 50$  pF and  $V_{DD} - V_{SS} = 10$  V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of  $1 \mu A$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range)
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



**Applications:**

- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Magnitude and sign generation
- Up/Down decade counting
- Difference counting

**RECOMMENDED OPERATING CONDITIONS at  $T_A = 25^\circ C$ , Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)	—	3	18	V
Setup Time $t_{SU}$ : Carry-In	5	200	—	ns
	10	70	—	
	15	60	—	
U/D or B/D	5	340	—	ns
	10	140	—	
	15	100	—	
Clock Pulse Width, $t_W$	5	180	—	ns
	10	90	—	
	15	60	—	
Preset Enable Pulse Width, $t_W$	5	130	—	ns
	10	70	—	
	15	50	—	
Clock Input Frequency, $f_{CL}$	5	—	2	MHz
	10	—	4	
	15	—	5.5	
Clock Rise and Fall Time, $t_{r,CL}$ , $t_{f,CL}$	5	—	15	$\mu s$
	10	—	15	
	15	—	15	

# CD4029B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10\text{mA}$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max	$+265^\circ\text{C}$

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ( $^\circ\text{C}$ )							UNITS
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, $I_{DD}$ Max.	-	0.5	5	5	5	150	150	-	0.04	5	$\mu\text{A}$
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current $I_{OL}$ Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, $I_{OH}$ Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, $V_{OL}$ Max.	-	0.5	5	0.05				-	0	0.05	V
	-	0.10	10	0.05				-	0	0.05	
	-	0.15	15	0.05				-	0	0.05	
Output Voltage: High-Level, $V_{OH}$ Min.	-	0.5	5	4.95				4.95	5	-	V
	-	0.10	10	9.95				9.95	10	-	
	-	0.15	15	14.95				14.95	15	-	
Input Low Voltage $V_{IL}$ Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, $V_{IH}$ Min.	0.5, 4.5	-	5	3.5				3.5	-	-	V
	1.9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current $I_{IN}$ Max.	-	0.18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu\text{A}$

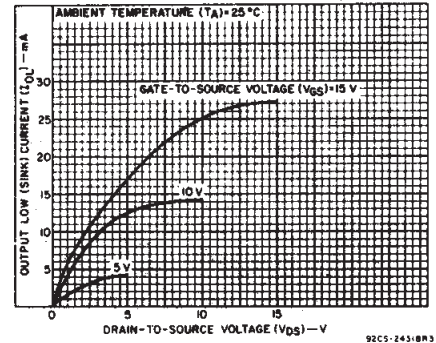


Fig. 1 - Typical output low (sink) current characteristics.

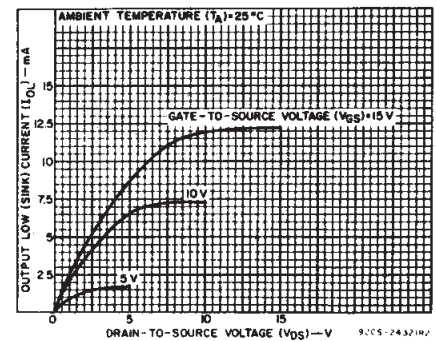


Fig. 2 - Minimum output low (sink) current characteristics.

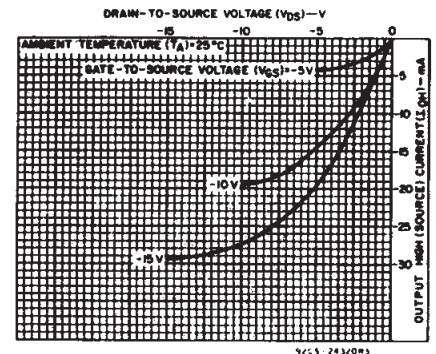


Fig. 3 - Typical output high (source) current characteristics.

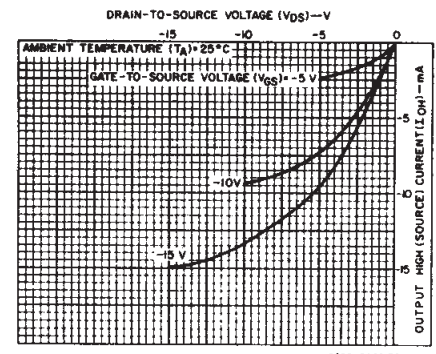


Fig. 4 - Minimum output high (source) current characteristics.

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# CD4029B Types

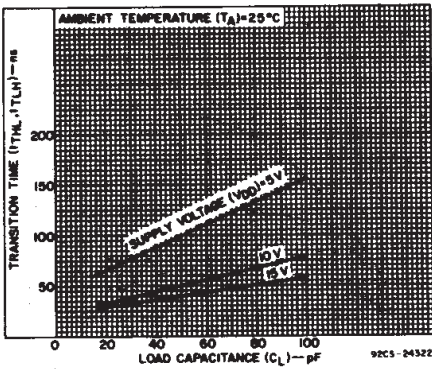


Fig. 5 - Typical transition time as a function of load capacitance.

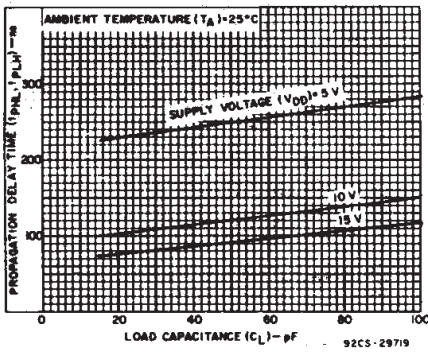


Fig. 6 - Typical propagation delay times as a function of load capacitance (Q output).

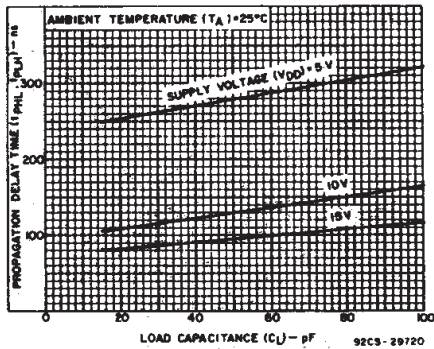


Fig. 7 - Typical propagation delay time as a function of load capacitance (carry output).

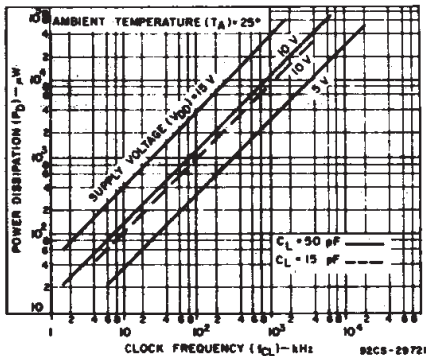
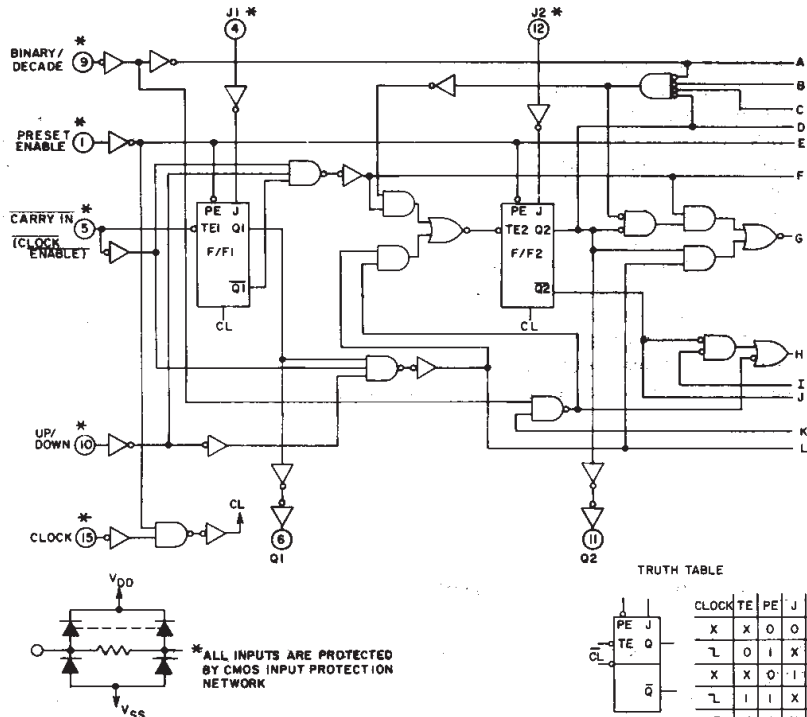


Fig. 8 - Typical power dissipation as a function of frequency.



TRUTH TABLE

CLOCK	TE	PE	J	Q	Q̄
X	X	0	0	0	1
L	0	1	X	Q	Q̄
X	X	0	1	1	0
L	1	1	X	Q̄	NC
L	X	1	X	Q	Q̄

X-DON'T CARE

92CL-28675R1

Fig. 9 - Logic diagram.

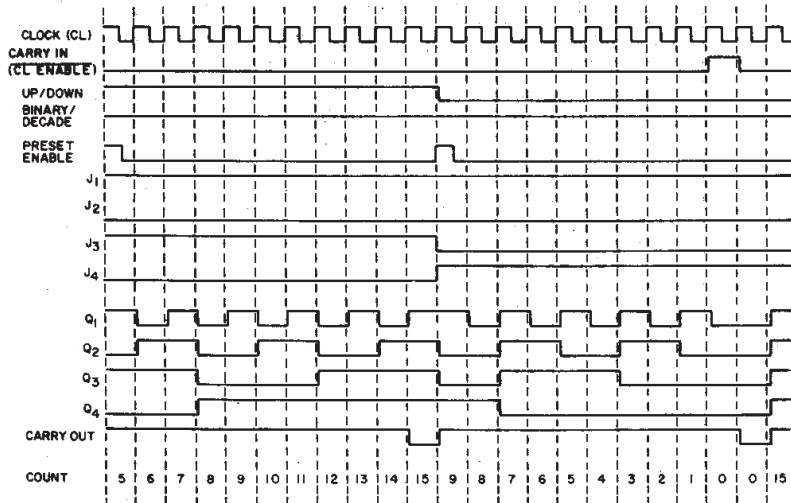
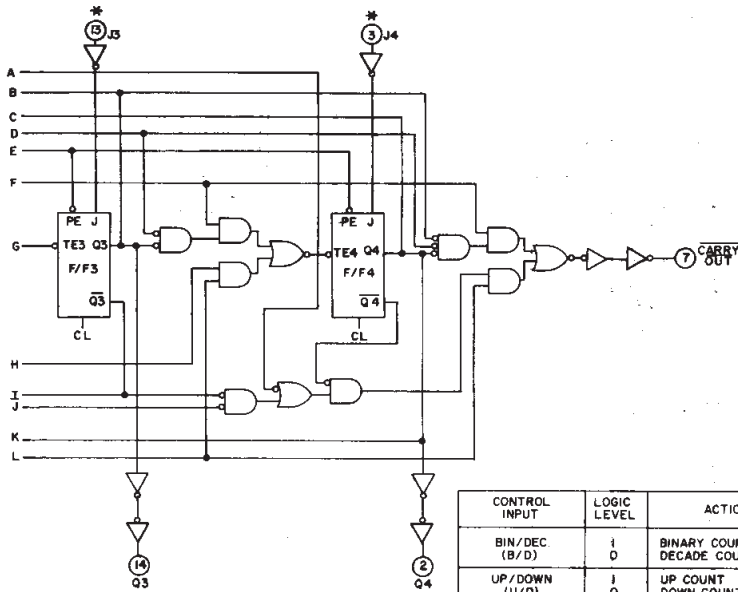


Fig. 10 - Timing diagram-binary mode.

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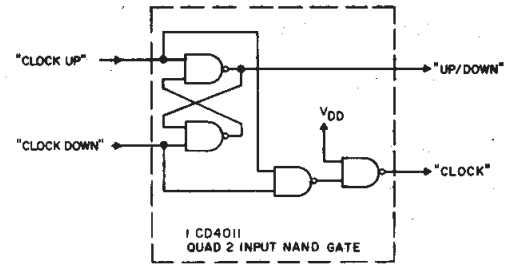
# CD4029B Types



CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1 0	BINARY COUNT DECADE COUNT
UP/DOWN (U/D)	1 0	UP COUNT DOWN COUNT
PRESET ENABLE (PE)	1 0	JAM IN NO JAM
CARRY IN (C <sub>I</sub> ) (CLOCK ENABLE)	1 0	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION ADVANCE COUNTER AT POS. CLOCK TRANSITION

92CL-28675 #1

Fig. 9 - Logic diagram (cont'd).

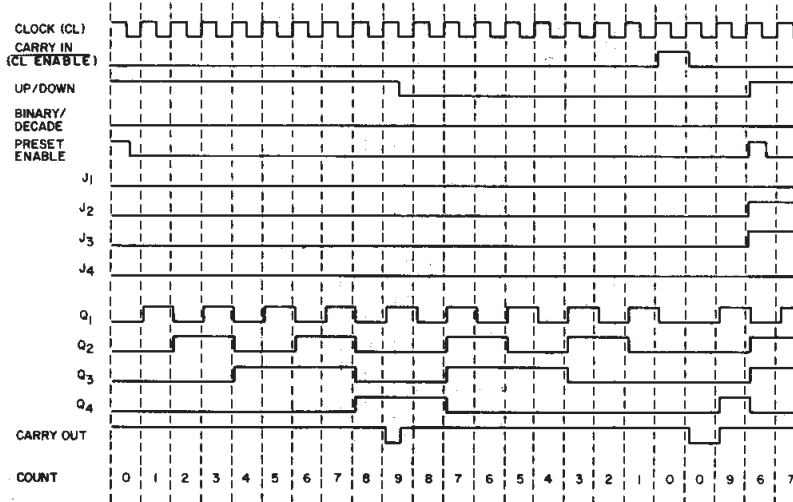


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Fig. 11 - Conversion of clock up, clock down input signals to clock and up/down input signals.

The CD4029B CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029B CLOCK and UP/DOWN inputs can easily be realized by use of the circuit in Fig. 11.

CD4029B changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.



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Fig. 12 - Timing diagram-decade mode.

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# CD4029B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS	
	$V_{DD}$ (V)		Min.	Typ.	Max.		
<b>Clocked Operation</b>							
Propagation Delay Time: $t_{PHL}, t_{PLH}$ Q Output	5	—	250	500		ns	
	10	—	120	240			
	15	—	90	180			
Carry Output	5	—	280	560			
	10	—	130	260			
	15	—	95	190			
Transition Time: $t_{THL}, t_{TLH}$ Q Outputs, Carry Output	5	—	100	200			
	10	—	50	100			
	15	—	40	80			
Minimum Clock Pulse Width, $t_W$	5	—	90	180			
	10	—	45	90			
	15	—	30	60			
Clock Rise & Fall Time, $t_{rCL}, t_{fCL}^{**}$	5	—	—	15			$\mu\text{s}$
	10	—	—	15			
	15	—	—	15			
Minimum Setup Times, $t_S^*$ B/D or U/D	5	—	170	340		ns	
	10	—	70	140			
	15	—	50	100			
Maximum Clock Input Frequency, $f_{CL}$	5	2	4	—		MHz	
	10	4	8	—			
	15	5.5	11	—			
Input Capacitance, $C_{IN}$	Any Input		—	5	7.5	pF	
<b>Preset Enable</b>							
Propagation Delay Time: $t_{PHL}, t_{PLH}$ Q Outputs	5	—	235	470		ns	
	10	—	100	200			
	15	—	80	160			
Carry Output	5	—	320	640			
	10	—	145	290			
	15	—	105	210			
Minimum Preset Enable Pulse Width, $t_W$	5	—	65	130			
	10	—	35	70			
	15	—	25	50			
Minimum Preset Enable Removal Time, $t_{rem}^*$	5	—	100	200			
	10	—	55	110			
	15	—	40	80			
<b>Carry Input</b>							
Propagation Delay Time: $t_{PHL}, t_{PLH}$ Carry Output	5	—	170	340			ns
	10	—	70	140			
	15	—	50	100			
Min. HOLD Time $t_H^{***}$ Carry In	5	—	25	50		ns	
	10	—	15	30			
	15	—	12	25			
Min Set-Up Time $t_S^{***}$ Carry In	5	—	100	200		ns	
	10	—	35	70			
	15	—	30	60			

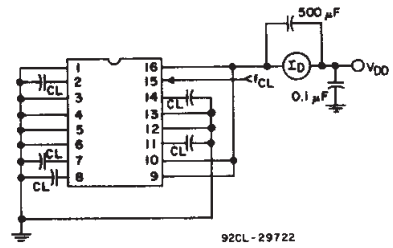


Fig. 13 – Power dissipation test circuit.

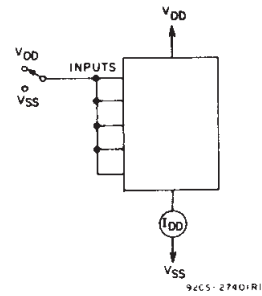


Fig. 14 – Quiescent device current test circuit.

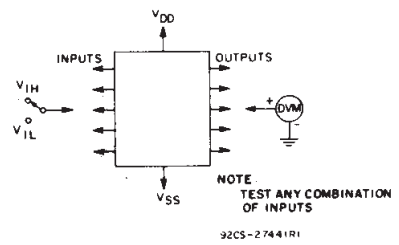


Fig. 15 – Input voltage test circuit.

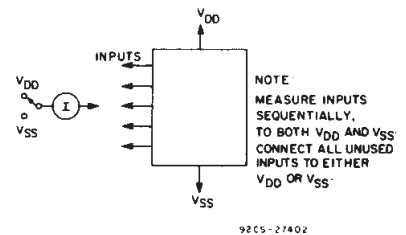
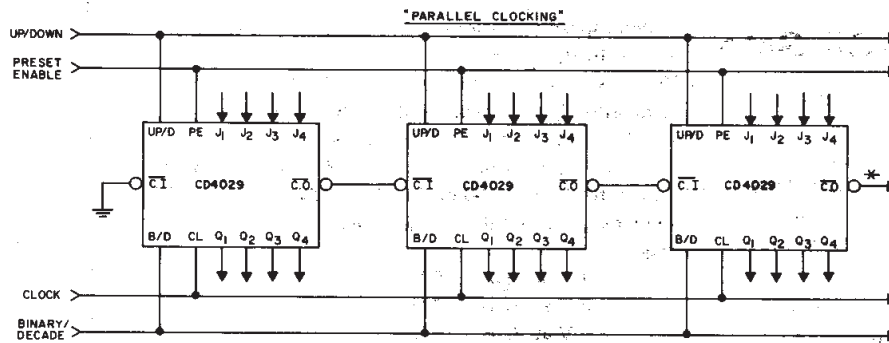


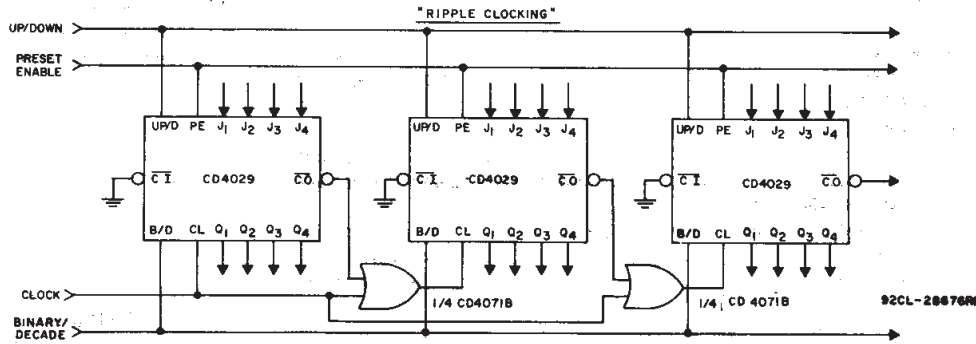
Fig. 16 – Input current test circuit.

\* From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.  
 \*\* If more than one unit is cascaded in the parallel clocked application,  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load. This measurement was made with a decoupling capacitor ( $>1\text{ }\mu\text{F}$ ) between  $V_{DD}$  and  $V_{SS}$ .  
 \*\*\* From Carry In to Clock Edge

# CD4029B Types

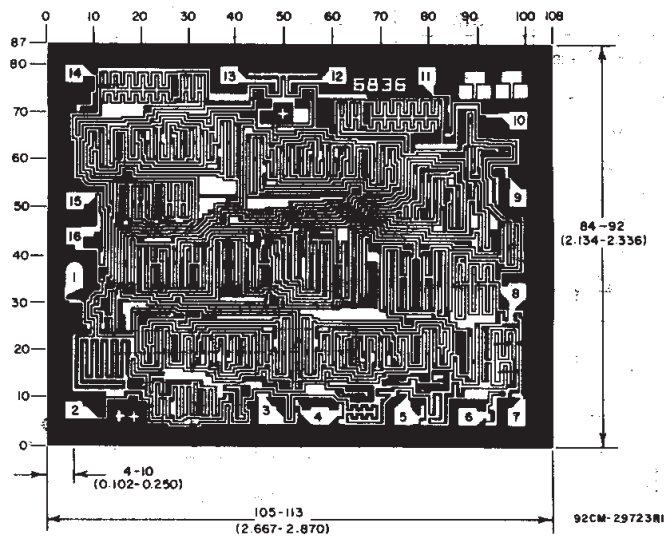


\* CARRY OUT lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4029B IC's. These negative-going glitches do not affect proper CD4029B operation. However, if the CARRY OUT signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the CARRY OUT signals should be gated with the clock signal using a 2-input OR gate such as CD4071B.



**Ripple Clocking Mode:**  
The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be high. For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages, and C.O. is connected directly to the CL input of the next stage with C.I. grounded.

Fig. 17 - Cascading counter packages.



Chip dimensions and pad layout for CD4029B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
8101602EA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4029BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4029BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4029BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4029BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4029BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4029BMT	ACTIVE	SOIC	D	16	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4029BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4029BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4029BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



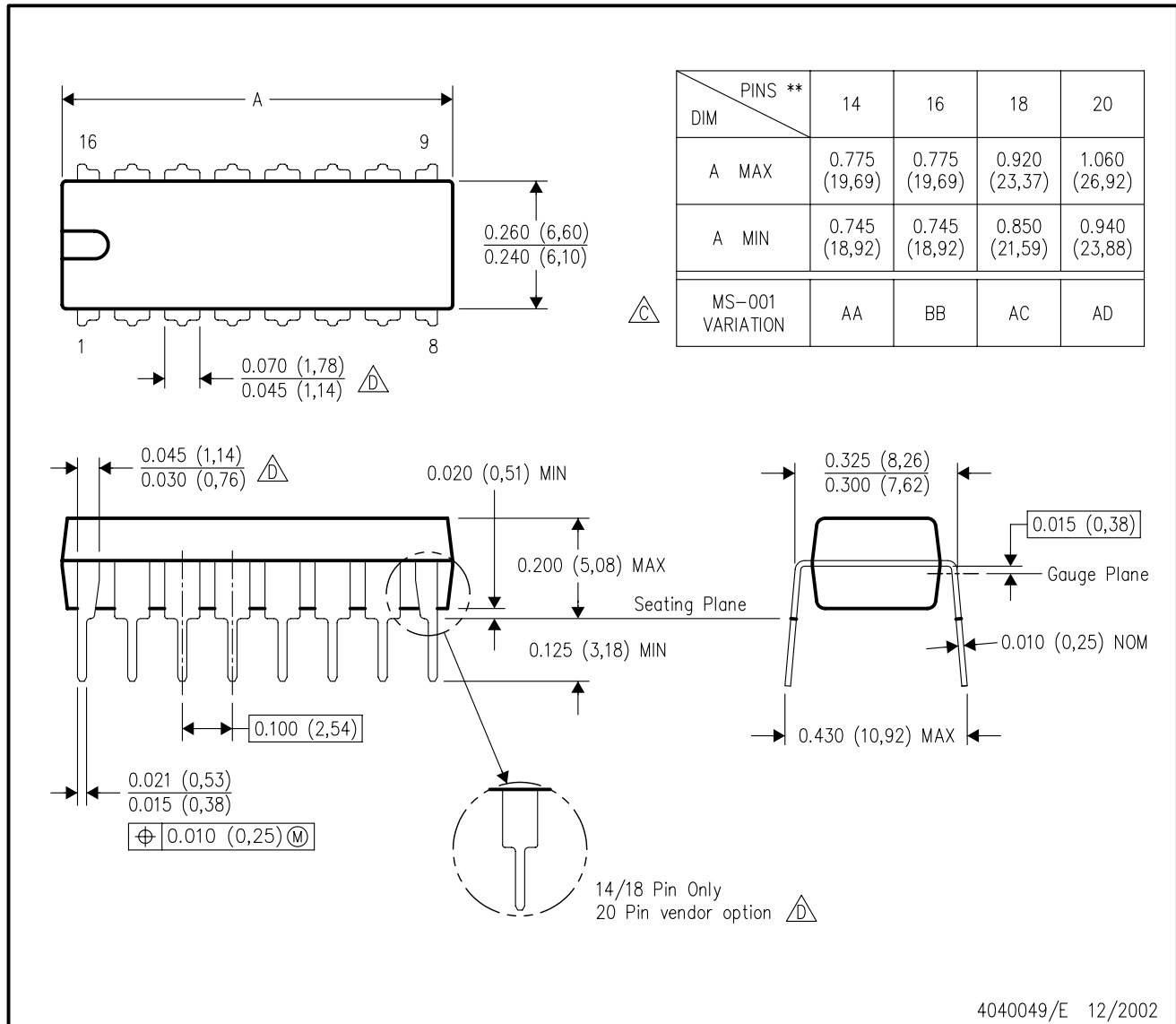
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- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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