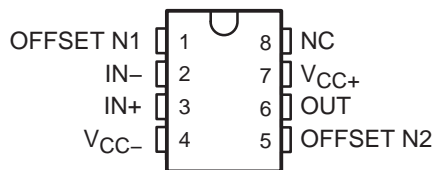


TL061, TL061A, TL061B, TL062, TL062A TL062B, TL064, TL064A, TL064B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

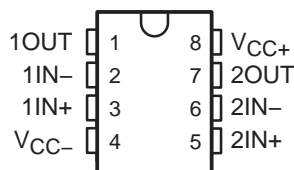
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- Very Low Power Consumption
- Typical Supply Current . . . 200 μ A (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes V_{CC+}
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/ μ s Typ

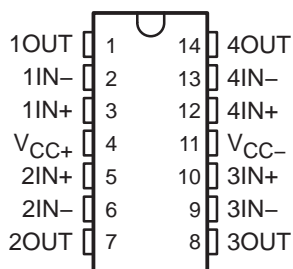
TL061, TL061A . . . D, P, OR PS PACKAGE
TL061B . . . P PACKAGE
(TOP VIEW)



TL062 . . . D, JG, P, PS, OR PW PACKAGE
TL062A . . . D, P, OR PS PACKAGE
TL062B . . . D OR P PACKAGE
(TOP VIEW)

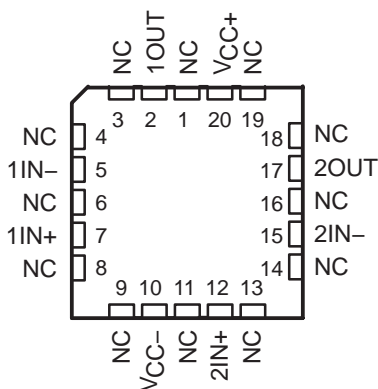


TL064 . . . D, J, N, NS, PW, OR W PACKAGE
TL064A, TL064B . . . D OR N PACKAGE
(TOP VIEW)

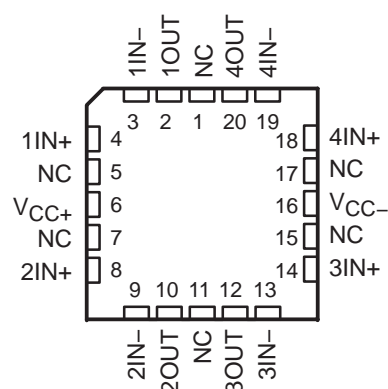


NC – No internal connection

TL062 . . . FK PACKAGE
(TOP VIEW)



TL064 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The JFET-input operational amplifiers of the TL06_ series are designed as low-power versions of the TL08_ series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and input bias currents. The TL06_ series features the same terminal assignments as the TL07_ and TL08_ series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in an integrated circuit.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C, and the M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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**TL061, TL061A, TL061B, TL062, TL062A
 TL062B, TL064, TL064A, TL064B
 LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

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description/ordering information (continued)

ORDERING INFORMATION

TA	V _{IO} MAX AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	15 mV	PDIP (P)	Tube of 50	TL061CP	TL061CP	
				TL062CP	TL062CP	
		PDIP (N)	Tube of 25	TL064CN	TL064CN	
		SOIC (D)	Tube of 75	TL061CD	TL061C	
				TL061CDR		
			Tube of 75	TL062CD	TL062C	
				TL062CDR		
			Tube of 50	TL064CD	TL064C	
				TL064CDR		
		SOP (PS)	Reel of 2000	TL061CPSR	T061	
				TL062CPSR	T062	
		SOP (NS)	Reel of 2000	TL064CNSR	TL064	
		TSSOP (PW)	Tube of 150	TL062CPW	T062	
				TL062CPWR		
			Tube of 90	TL064CPW	T064	
				TL064CPWR		
		6 mV	PDIP (P)	Tube of 50	TL061ACP	TL061ACP
					TL062ACP	TL062ACP
	PDIP (N)		Tube of 25	TL064ACN	TL064ACN	
				Tube of 75	TL061ACD	061AC
	TL061ACDR					
	SOIC (D)		Tube of 75	TL062ACD	062AC	
				TL062ACDR		
			Tube of 50	TL064ACD	TL064AC	
				TL064ACDR		
	SOP (PS)		Reel of 2000	TL061ACPSR	T061A	
				TL062ACPSR	T062A	
	3 mV		PDIP (P)	Tube of 50	TL061BCP	TL061BCP
		TL062BCP			TL062BCP	
		PDIP (N)	Tube of 25	TL064BCN	TL064BCN	
Tube of 75				TL062BCD	062BC	
		TL062BCDR				
SOIC (D)		Tube of 50	TL064BCD	TL064BC		
	TL064BCDR					

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

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description/ordering information (continued)

ORDERING INFORMATION (continued)

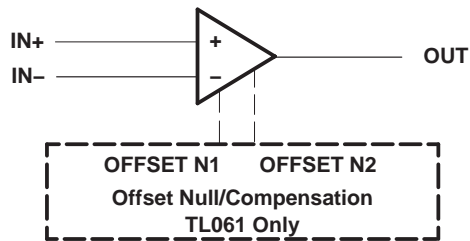
TA	V _{IO} MAX AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL061IP	TL061IP
				TL062IP	TL062IP
		PDIP (N)	Tube of 25	TL064IN	TL064IN
		SOIC (D)	Tube of 75	TL061ID	TL061I
				TL061IDR	
			Tube of 75	TL062ID	TL062I
				TL062IDR	
			Tube of 50	TL064ID	TL064I
				TL064IDR	
		TSSOP (PW)	Reel of 2000	TL062IPWR	TL062I
-55°C to 125°C	6 mV	CDIP (JG)	Tube of 50	TL062MJG	TL062MJG
		LCCC (FK)	Tube of 55	TL062MFK	TL062MFK
	9 mV	CDIP (J)	Tube of 25	TL064MJ	TL064MJ
		CFP (W)	Tube of 150	TL064MW	TL064MW
		LCCC (FK)	Tube of 55	TL064MFK	TL064MFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

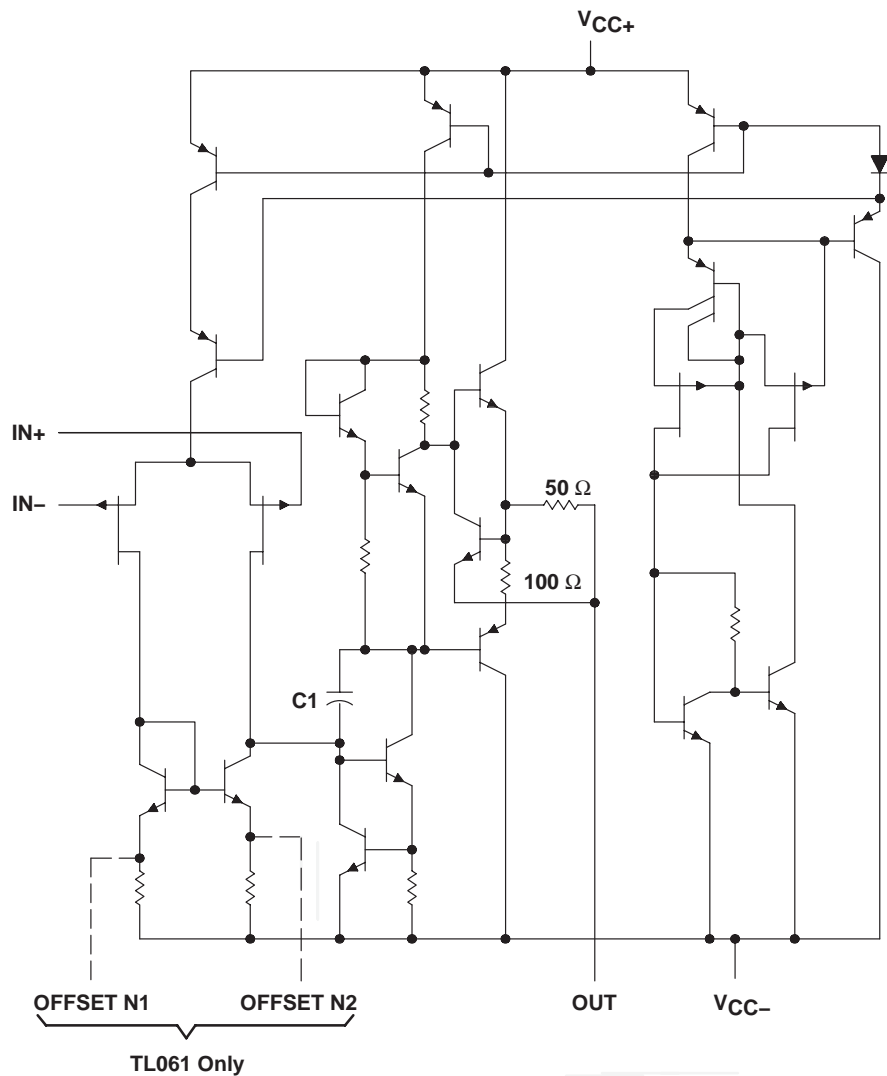
**TL061, TL061A, TL061B, TL062, TL062A
 TL062B, TL064, TL064A, TL064B
 LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

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symbol (each amplifier)



schematic (each amplifier)



$C1 = 10 \text{ pF}$ on TL061, TL062, and TL064
 Component values shown are nominal.

**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL06_C TL06_AC TL06_BC	TL06_I	TL06_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		-18	-18	-18	V
Differential input voltage, V_{ID} (see Note 2)		± 30	± 30	± 30	V
Input voltage, V_I (see Notes 1 and 3)		± 15	± 15	± 15	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Package thermal impedance, θ_{JA} (see Notes 5 and 6)	D (8-pin) package	97	97		°C/W
	D (14-pin) package	86	86		
	N package	80	80		
	NS package	76	76		
	P package	85	85		
	PS package	95	95		
	PW (8-pin) package	149	149		
Package thermal impedance, θ_{JC} (see Notes 7 and 8)	FK package			5.61	°C/W
	J package			15.05	
	JG package			14.5	
	W package			14.65	
Operating virtual junction temperature, T_J		150	150	150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package			300	°C
Lead temperature 1,6 mm (1/6 inch) from case for 10 seconds	D, N, NS, P, PS, or PW package	260	260		°C
Storage temperature range, T_{stg}		-65 to 150	-65 to 150	-65 to 150	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-} .
 - Differential voltages are at $IN+$ with respect to $IN-$.
 - The magnitude of the input voltage should never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 - The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
 - Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - The package thermal impedance is calculated in accordance with JESD 51-7.
 - Maximum power dissipation is a function of $T_J(\max)$, θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(\max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - The package thermal impedance is calculated in accordance with MIL-STD-883.



**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

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electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL061C TL062C TL064C			TL061AC TL062AC TL064AC			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO}	Input offset voltage	$V_O = 0,$ $R_S = 50\ \Omega$		$T_A = 25^\circ\text{C}$	3	15	3	6	mV
				$T_A = \text{Full range}$	20		7.5		
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega,$ $T_A = \text{Full range}$			10		10		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current	$V_O = 0$		$T_A = 25^\circ\text{C}$	5	200	5	100	pA
				$T_A = \text{Full range}$	5		3		nA
I_{IB}	Input bias current‡	$V_O = 0$		$T_A = 25^\circ\text{C}$	30	400	30	200	pA
				$T_A = \text{Full range}$	10		7		nA
V_{ICR}	Common-mode input voltage range	$T_A = 25^\circ\text{C}$			± 11	-12 to 15	± 11	-12 to 15	V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega,$		$T_A = 25^\circ\text{C}$	± 10	± 13.5	± 10	± 13.5	V
		$R_L \geq 10\ \text{k}\Omega,$		$T_A = \text{Full range}$	± 10		± 10		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V},$ $R_L \geq 10\ \text{k}\Omega$		$T_A = 25^\circ\text{C}$	3	6	4	6	V/mV
				$T_A = \text{Full range}$	3		4		
B_1	Unity-gain bandwidth	$R_L = 10\ \text{k}\Omega,$		$T_A = 25^\circ\text{C}$	1		1		MHz
r_i	Input resistance	$T_A = 25^\circ\text{C}$			10^{12}		10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0,$ $R_S = 50\ \Omega, T_A = 25^\circ\text{C}$			70	86	80	86	dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V},$ $V_O = 0, R_S = 50\ \Omega,$ $T_A = 25^\circ\text{C}$			70	95	80	95	dB
P_D	Total power dissipation (each amplifier)	$V_O = 0,$ No load		$T_A = 25^\circ\text{C},$	6	7.5	6	7.5	mW
I_{CC}	Supply current (each amplifier)	$V_O = 0,$ No load		$T_A = 25^\circ\text{C},$	200	250	200	250	μA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100,$		$T_A = 25^\circ\text{C}$	120		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC and -40°C to 85°C for TL06_I.

‡ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 15. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.



**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

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electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITION [†]	TL061BC TL062BC TL064BC			TL061I TL062I TL064I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0,$ $R_S = 50 \Omega$	$T_A = 25^\circ\text{C}$		3		6	mV
			$T_A = \text{Full range}$		5		9	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50 \Omega,$ $T_A = \text{Full range}$		10		10	$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25^\circ\text{C}$		5		100	pA
			$T_A = \text{Full range}$		3		10	nA
I_{IB}	Input bias current [‡]	$V_O = 0$	$T_A = 25^\circ\text{C}$		30		200	pA
			$T_A = \text{Full range}$		7		20	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25^\circ\text{C}$		± 11	-12 to 15	± 11	-12 to 15	V
V_{OM}	Maximum peak output voltage swing	$R_L = 10 \text{ k}\Omega, T_A = 25^\circ\text{C}$		± 10	± 13.5	± 10	± 13.5	V
		$R_L \geq 10 \text{ k}\Omega, T_A = \text{Full range}$		± 10		± 10		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10 \text{ V},$ $R_L \geq 10 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$		4		6	V/mV
			$T_A = \text{Full range}$		4		4	
B_1	Unity-gain bandwidth	$R_L = 10 \text{ k}\Omega, T_A = 25^\circ\text{C}$		1		1	MHz	
r_i	Input resistance	$T_A = 25^\circ\text{C}$		10^{12}		10^{12}	Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0,$ $R_S = 50 \Omega, T_A = 25^\circ\text{C}$		80		86	dB	
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9 \text{ V to } \pm 15 \text{ V},$ $V_O = 0, R_S = 50 \Omega,$ $T_A = 25^\circ\text{C}$		80		95	dB	
P_D	Total power dissipation (each amplifier)	$V_O = 0,$ No load	$T_A = 25^\circ\text{C},$		6		7.5	mW
I_{CC}	Supply current (each amplifier)	$V_O = 0,$ No load	$T_A = 25^\circ\text{C},$		200		250	μA
VO_1/VO_2	Crosstalk attenuation	$A_{VD} = 100, T_A = 25^\circ\text{C}$		120		120	dB	

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC and -40°C to 85°C for TL06_I.

[‡] Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 15. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

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electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL061M TL062M			TL064M			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0$, $R_S = 50 \Omega$	$T_A = 25^\circ\text{C}$		3	6	3	9	mV
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		9			15	
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50 \Omega$, $T_A = -55^\circ\text{C to } 125^\circ\text{C}$	10			10			$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current	$V_O = 0$	$T_A = 25^\circ\text{C}$		5	100	5	100	pA
		$T_A = -55^\circ\text{C}$		20*			20*	nA
		$T_A = 125^\circ\text{C}$		20			20	
I_{IB} Input bias current‡	$V_O = 0$	$T_A = 25^\circ\text{C}$		30	200	30	200	pA
		$T_A = -55^\circ\text{C}$		50*			50*	nA
		$T_A = 125^\circ\text{C}$		50			50	
V_{ICR} Common-mode input voltage range	$T_A = 25^\circ\text{C}$	± 11.5	-12 to 15	± 11.5	-12 to 15			V
V_{OM} Maximum peak output voltage swing	$R_L = 10 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$	± 10	± 13.5	± 10	± 13.5			V
	$R_L \geq 10 \text{ k}\Omega$, $T_A = -55^\circ\text{C to } 125^\circ\text{C}$	± 10		± 10				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10 \text{ V}$, $R_L \geq 10 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$		4	6	4	6	V/mV
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		4				
B_1 Unity-gain bandwidth	$R_L = 10 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$							MHz
r_i Input resistance	$T_A = 25^\circ\text{C}$	10^{12}			10^{12}			Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$, $V_O = 0$, $R_S = 50 \Omega$, $T_A = 25^\circ\text{C}$	80	86	80	86			dB
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9 \text{ V to } \pm 15 \text{ V}$, $V_O = 0$, $R_S = 50 \Omega$, $T_A = 25^\circ\text{C}$	80	95	80	95			dB
P_D Total power dissipation (each amplifier)	$V_O = 0$, No load	$T_A = 25^\circ\text{C}$		6	7.5	6	7.5	mW
I_{CC} Supply current (each amplifier)	$V_O = 0$, No load	$T_A = 25^\circ\text{C}$		200	250	200	250	μA
V_{O1}/V_{O2} Crosstalk attenuation	$A_{VD} = 100$, $T_A = 25^\circ\text{C}$	120			120			dB

* This parameter is not production tested.

† All characteristics are measured under open-loop conditions, with zero common-mode voltage, unless otherwise specified.

‡ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 15. Pulse techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unity gain (see Note 5)	$V_I = 10 \text{ V}$, $R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Figure 1	1.5	3.5		V/ μs
t_r Rise time	$V_I = 20 \text{ mV}$, $C_L = 100 \text{ pF}$, See Figure 1	0.2			μs
Overshoot factor		10%			
V_n Equivalent input noise voltage	$R_S = 20 \Omega$, $f = 1 \text{ kHz}$	42			nV/ $\sqrt{\text{Hz}}$

NOTE 5: Slew rate at $-55^\circ\text{C to } 125^\circ\text{C}$ is 0.7 V/ μs min.



PARAMETER MEASUREMENT INFORMATION

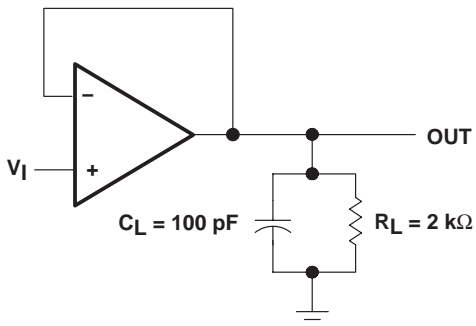


Figure 1. Unity-Gain Amplifier

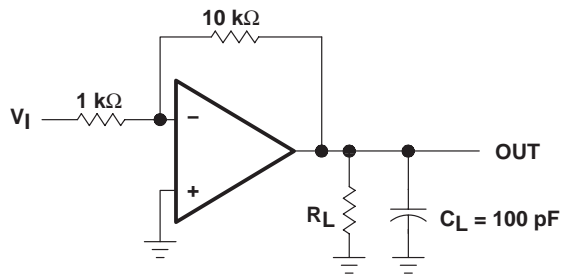


Figure 2. Gain-of-10 Inverting Amplifier

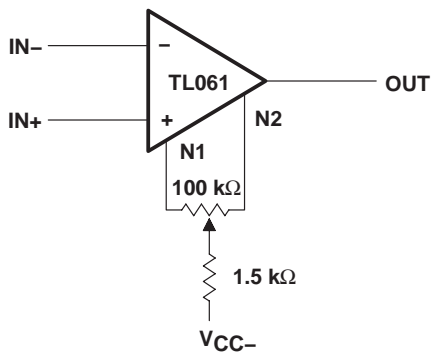


Figure 3. Input Offset-Voltage Null Circuit

TYPICAL CHARACTERISTICS

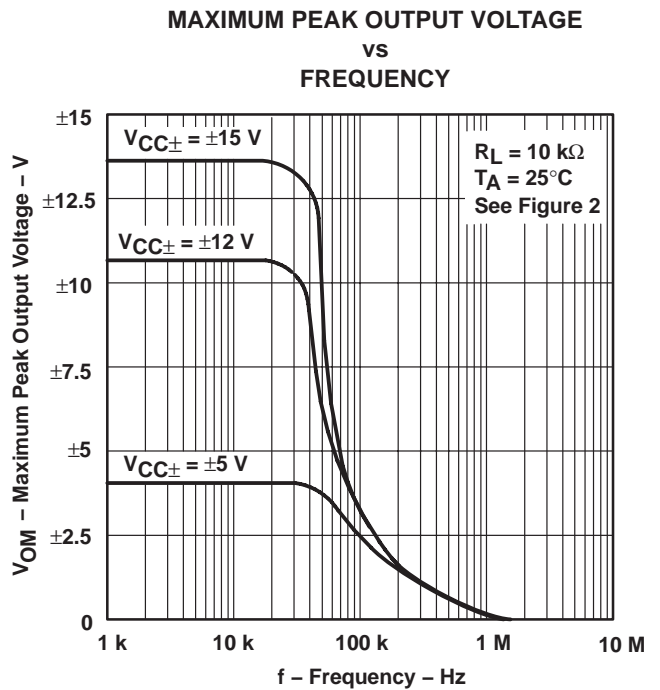
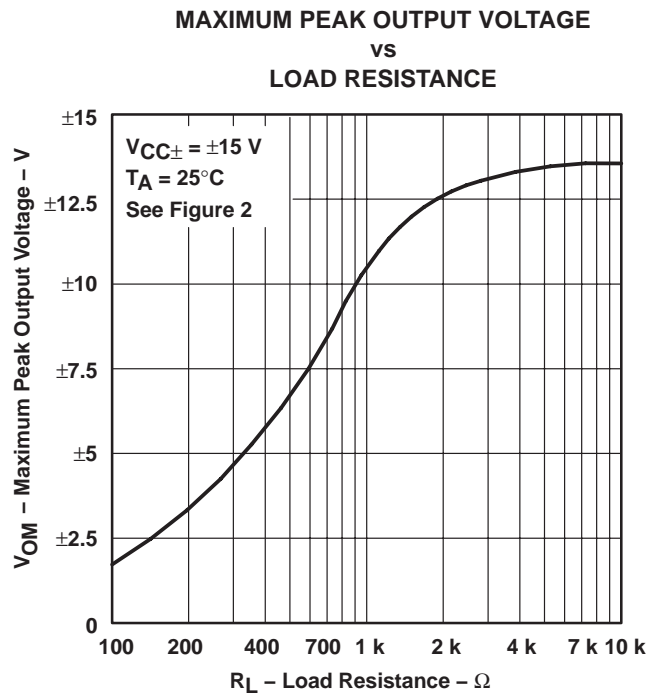
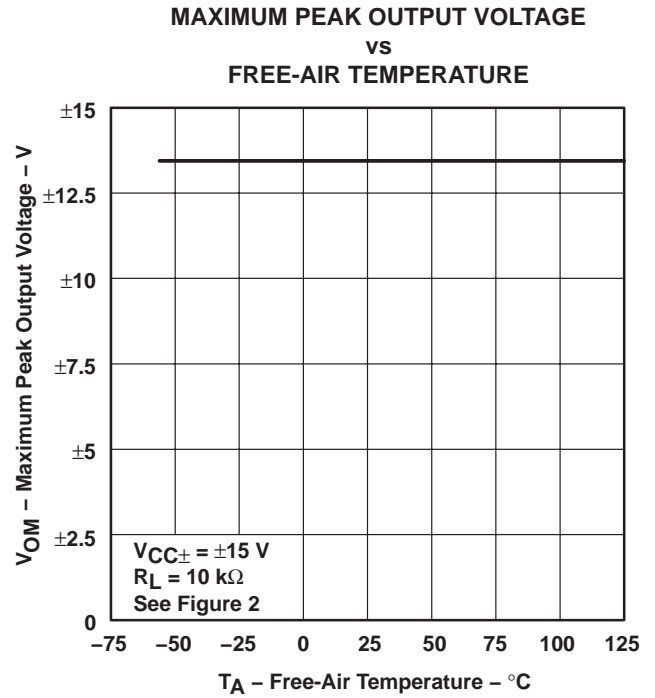
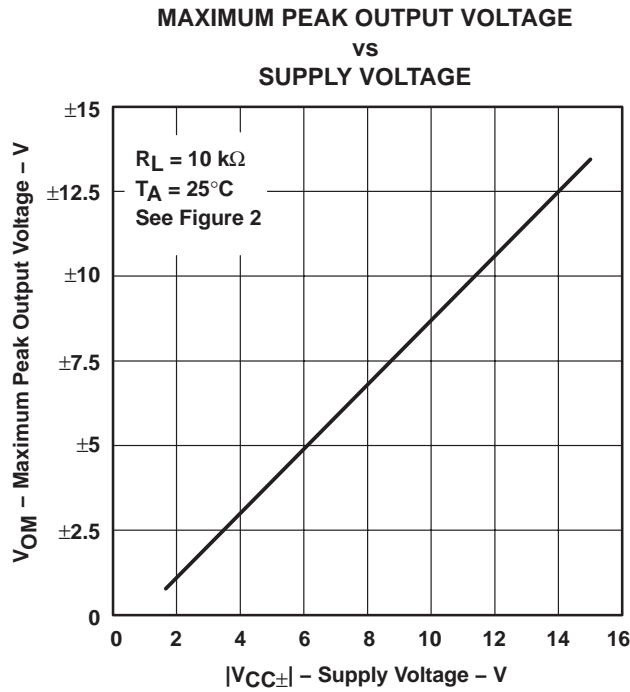
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Equivalent input noise voltage vs Frequency	18

**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS078J – NOVEMBER 1978 – REVISED SEPTEMBER 2004

TYPICAL CHARACTERISTICS†



† Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

**DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE**

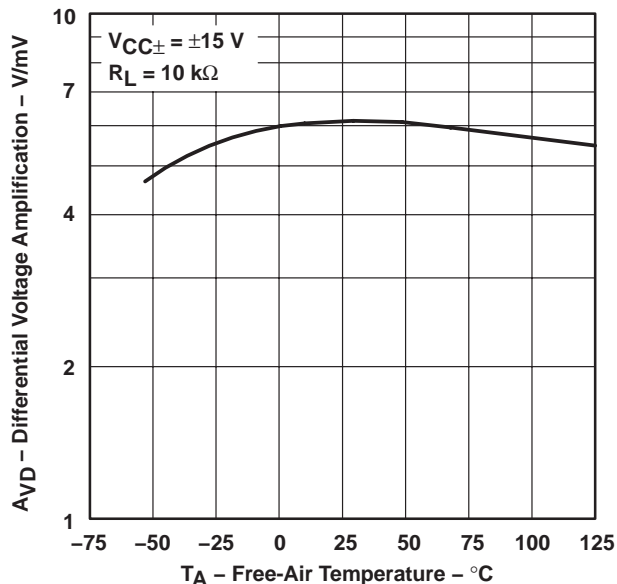


Figure 8

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE SHIFT
 vs
 FREQUENCY**

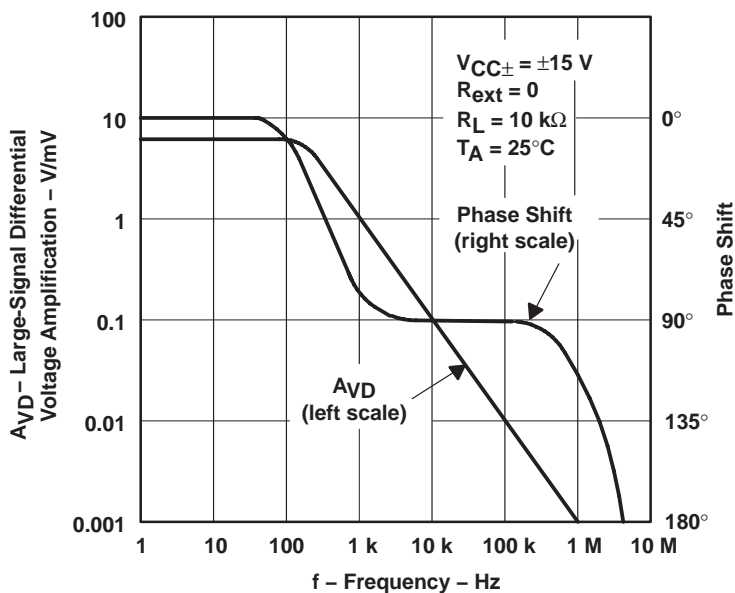


Figure 9

† Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B**
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS078J – NOVEMBER 1978 – REVISED SEPTEMBER 2004

TYPICAL CHARACTERISTICS†

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

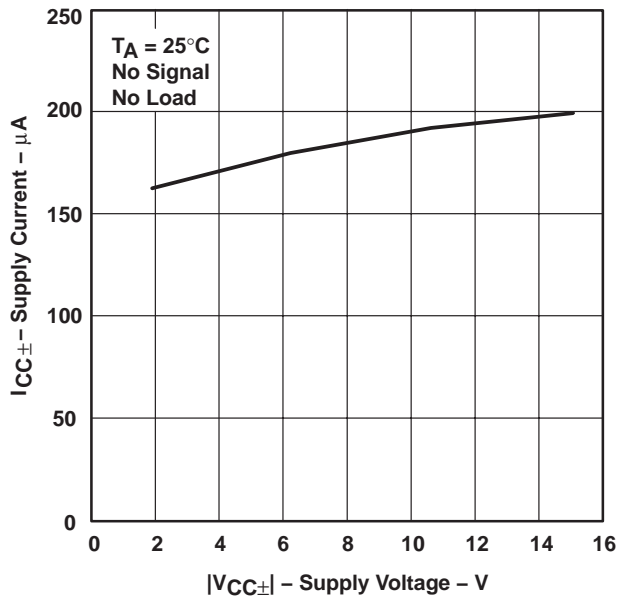


Figure 10

**SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

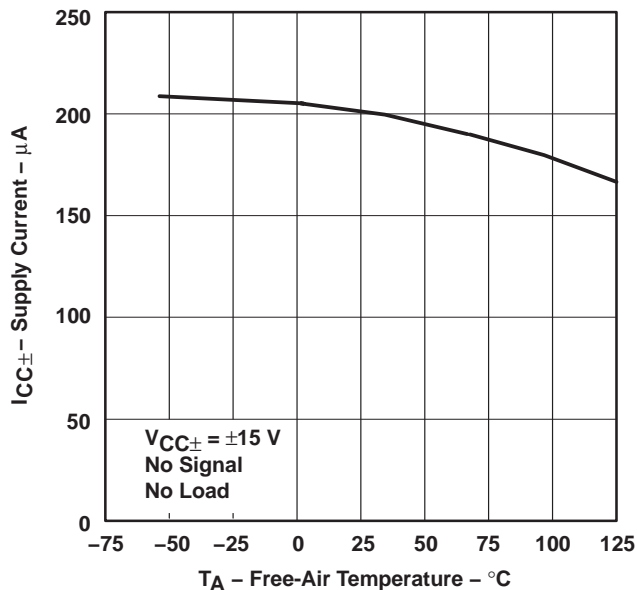


Figure 11

**TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE**

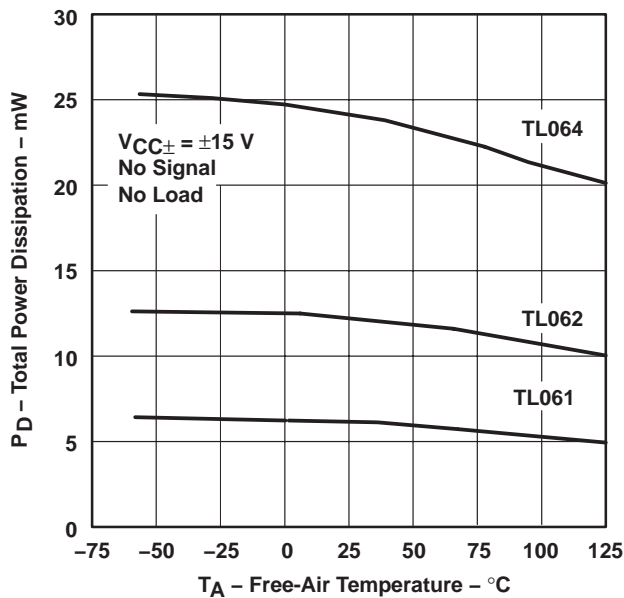


Figure 12

**ALL EXCEPT TL06_C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE**

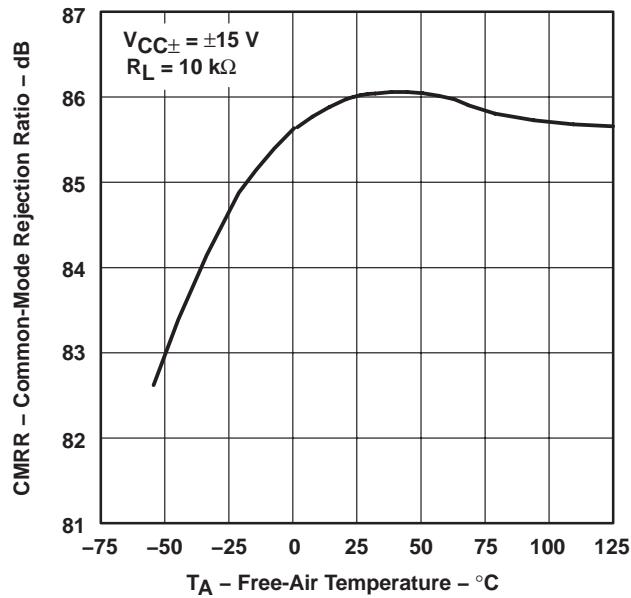


Figure 13

† Data at high and low temperatures are applicable only within the specified operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

NORMALIZED UNITY-GAIN BANDWIDTH,
 SLEW RATE, AND PHASE SHIFT

vs

FREE-AIR TEMPERATURE

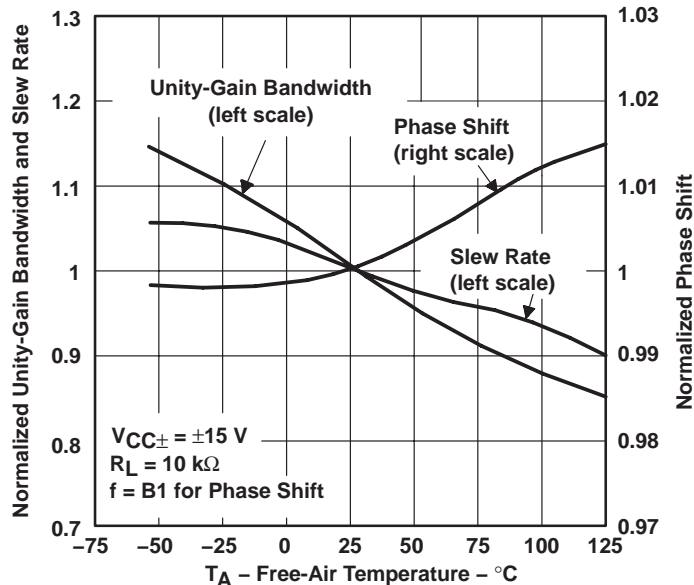


Figure 14

INPUT BIAS CURRENT
 vs
 FREE-AIR TEMPERATURE

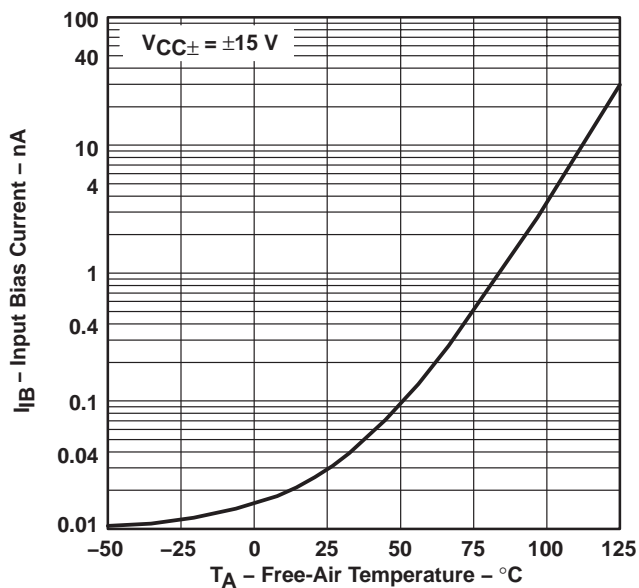


Figure 15

VOLTAGE-FOLLOWER
 LARGE-SIGNAL PULSE RESPONSE
 vs
 TIME

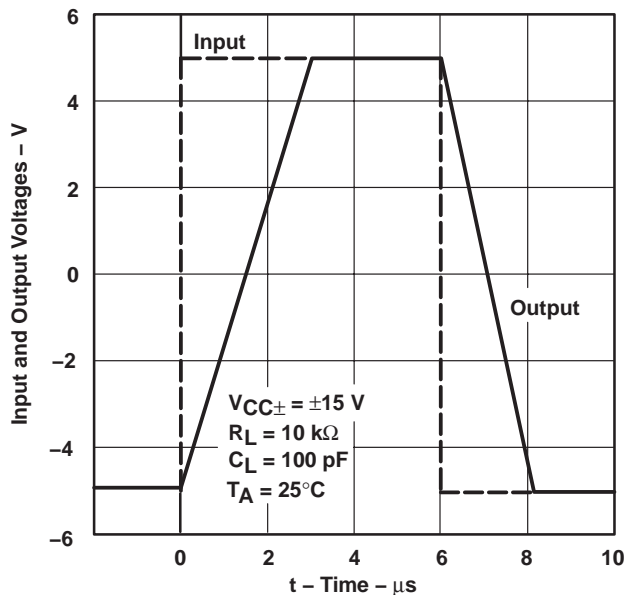
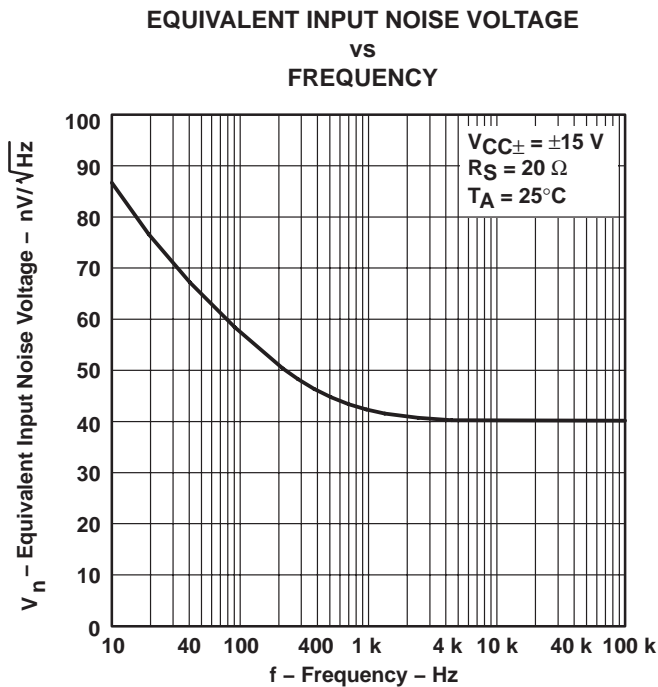
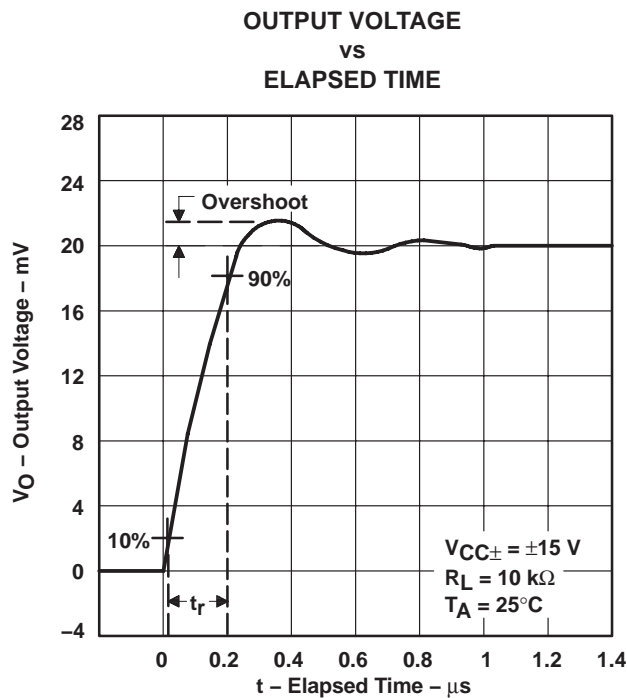


Figure 16

**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS078J – NOVEMBER 1978 – REVISED SEPTEMBER 2004

TYPICAL CHARACTERISTICS



**TL061, TL061A, TL061B, TL062, TL062A
TL062B, TL064, TL064A, TL064B
LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS**

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APPLICATION INFORMATION

Table of Application Diagrams

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Instrumentation amplifier	TL064	19
0.5-Hz square-wave oscillator	TL061	20
High-Q notch filter	TL061	21
Audio-distribution amplifier	TL064	22
Low-level light detector preamplifier	TL061	23
AC amplifier	TL061	24
Microphone preamplifier with tone control	TL061	25
Instrumentation amplifier	TL062	26
IC preamplifier	TL062	27

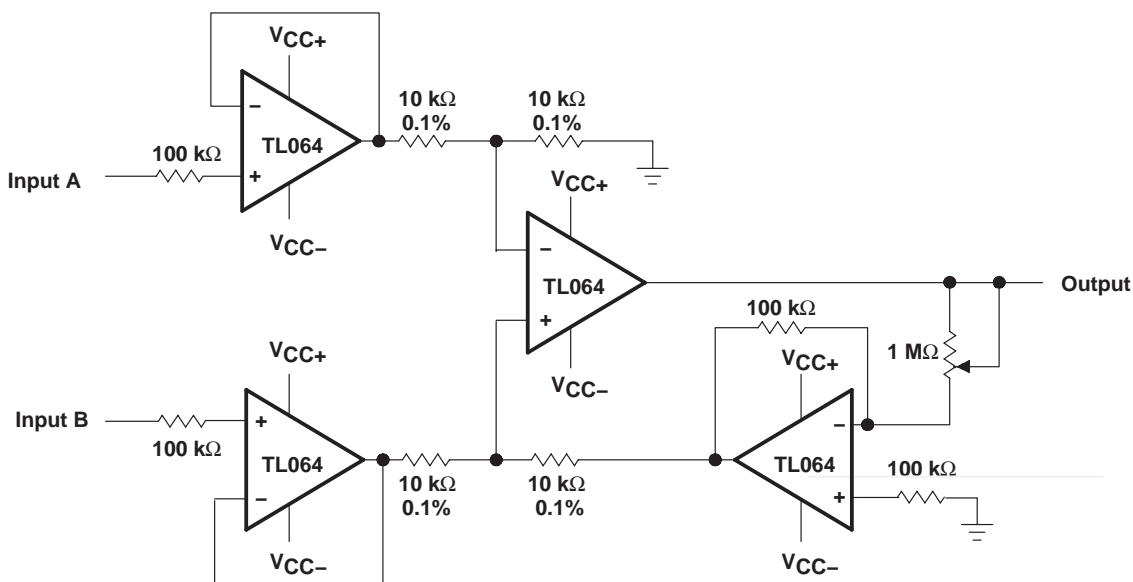


Figure 19. Instrumentation Amplifier

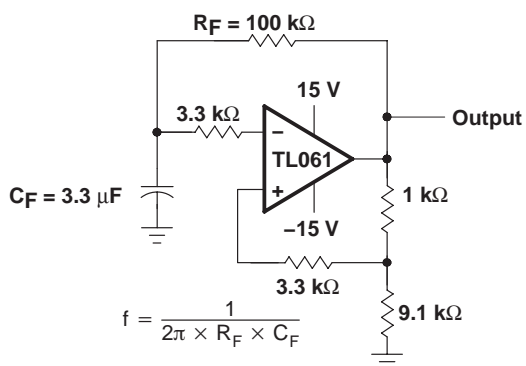


Figure 20. 0.5-Hz Square-Wave Oscillator

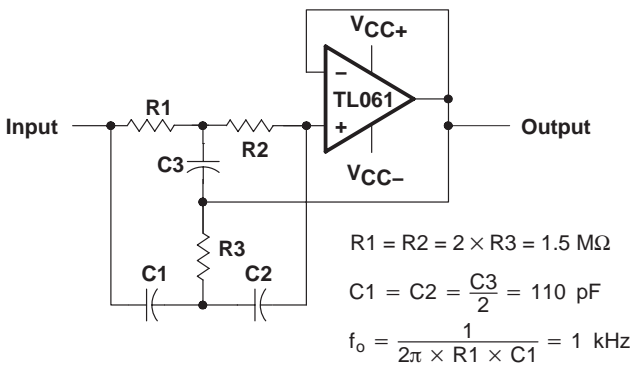


Figure 21. High-Q Notch Filter

APPLICATION INFORMATION

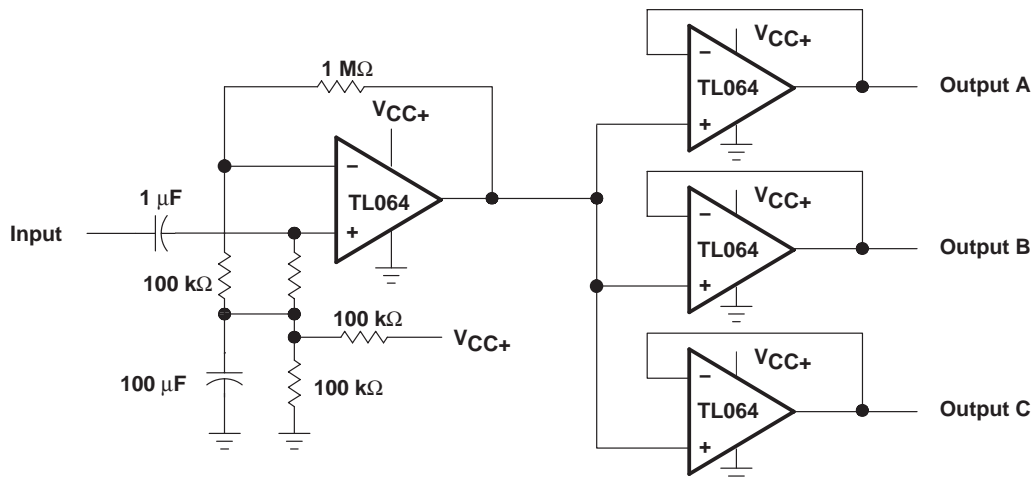


Figure 22. Audio-Distribution Amplifier

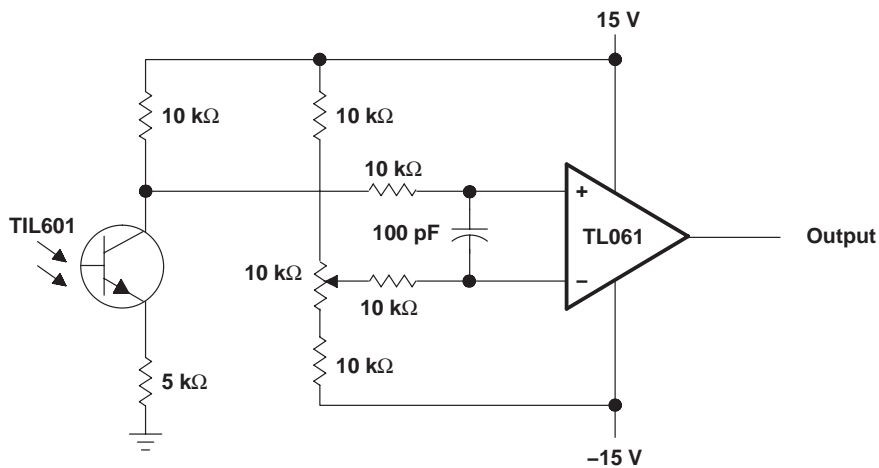


Figure 23. Low-Level Light Detector Preamplifier

APPLICATION INFORMATION

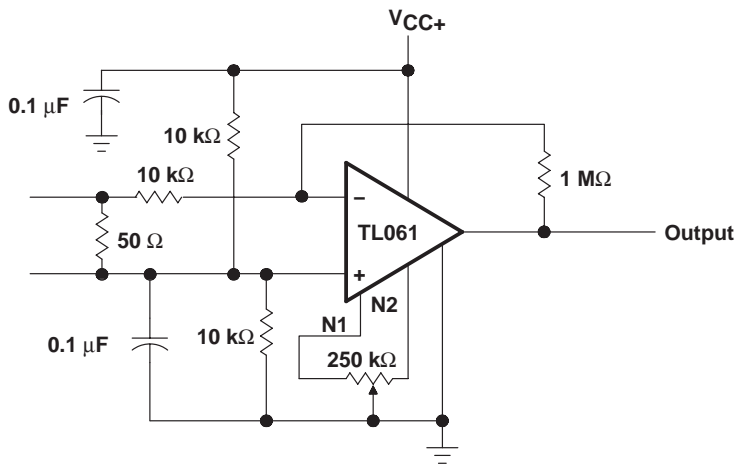


Figure 24. AC Amplifier

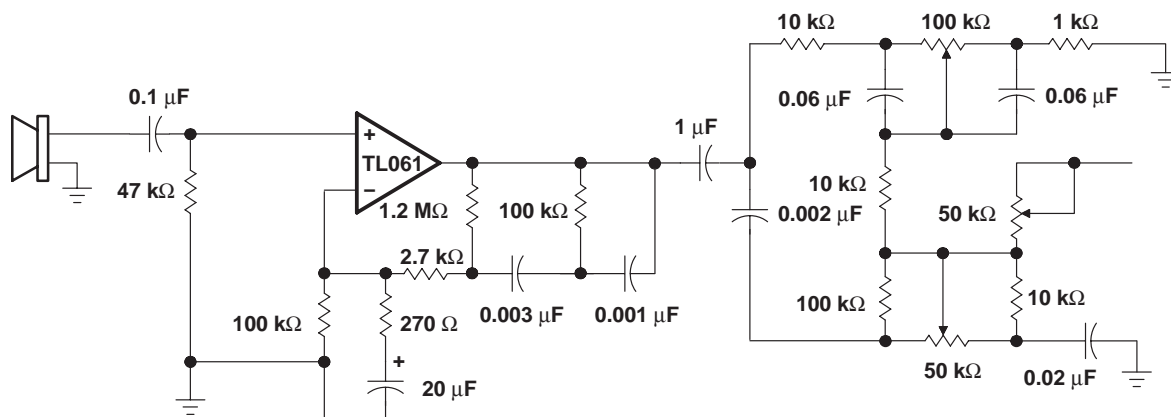


Figure 25. Microphone Preamp with Tone Control

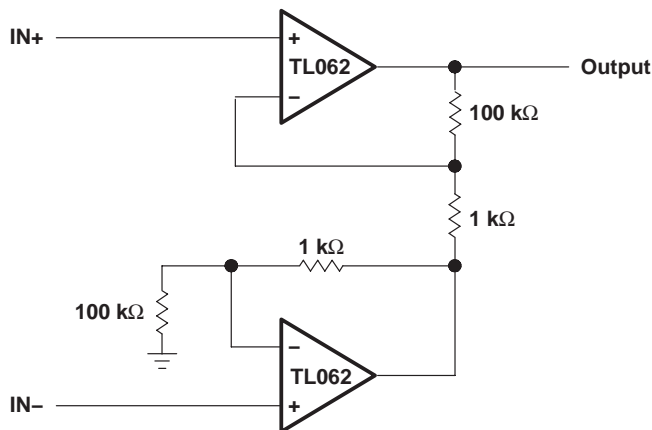


Figure 26. Instrumentation Amplifier

APPLICATION INFORMATION

IC PREAMPLIFIER RESPONSE CHARACTERISTICS

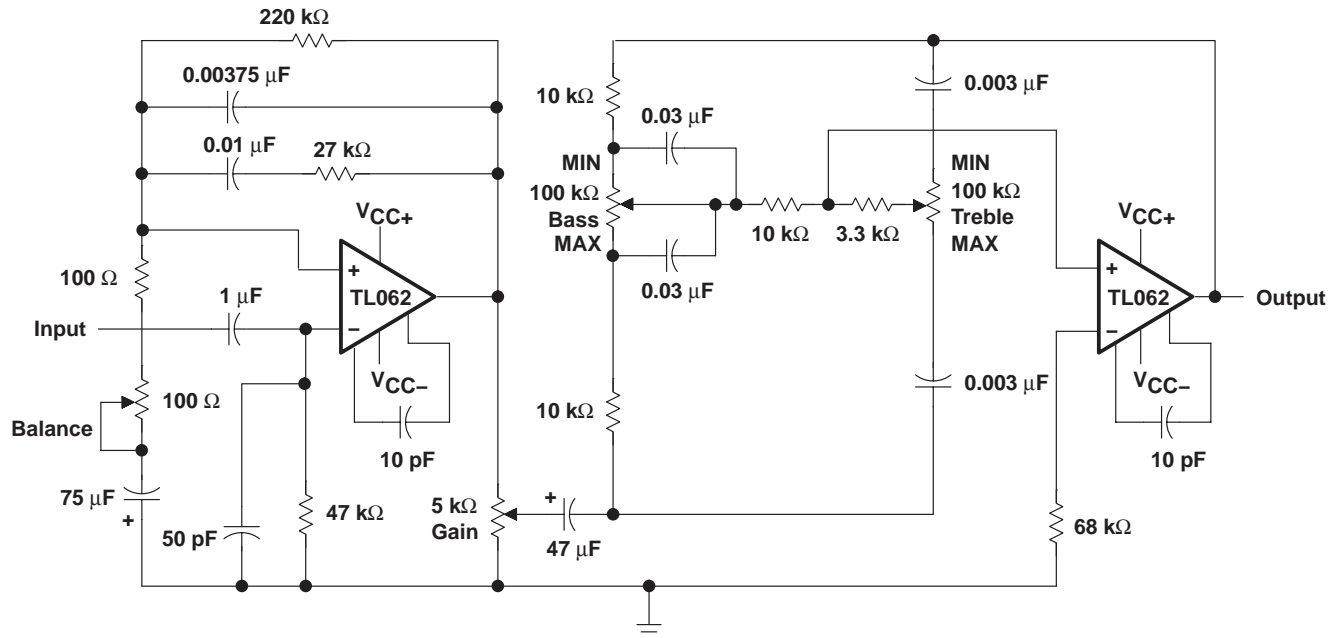
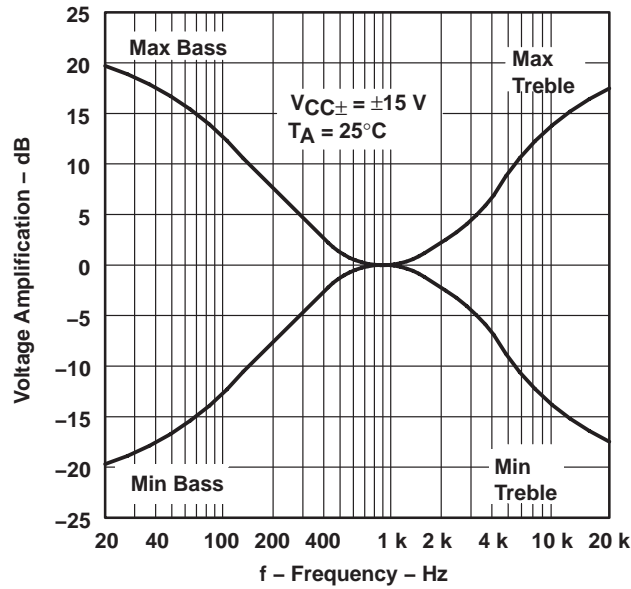


Figure 27. IC Preamplifier

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
81023012A	OBSOLETE	LCCC	FK	20		None	Call TI	Call TI
81023022A	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
8102302HA	ACTIVE	CFP	U	10	1	None	A42 SNPB	Level-NC-NC-NC
8102302PA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
81023032A	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
8102303CA	ACTIVE	CDIP	J	14	1	None	A42 SNPB	Level-NC-NC-NC
8102303DA	ACTIVE	CFP	W	14	1	None	A42 SNPB	Level-NC-NC-NC
TL061ACD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL061ACDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL061ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL061ACPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL061BCD	OBSOLETE	SOIC	D	8		None	Call TI	Call TI
TL061BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL061CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL061CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL061CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL061CPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL061CPWLE	OBSOLETE	TSSOP	PW	8		None	Call TI	Call TI
TL061ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL061IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL061IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL061MJG	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
TL061MJGB	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
TL062ACD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL062ACDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL062ACJG	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
TL062ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL062ACPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL062BCD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL062BCDR	ACTIVE	SOIC	D	8	2500	Pb-Free	CU NIPDAU	Level-2-250C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						(RoHS)		
TL062BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL062CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL062CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL062CJG	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
TL062CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL062CPSLE	OBSOLETE	SO	PS	8		None	Call TI	Call TI
TL062CPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL062CPW	ACTIVE	TSSOP	PW	8	150	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL062CPWLE	OBSOLETE	TSSOP	PW	8		None	Call TI	Call TI
TL062CPWR	ACTIVE	TSSOP	PW	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL062ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL062IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL062IJG	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
TL062IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL062IPWR	ACTIVE	TSSOP	PW	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL062MFKB	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
TL062MJG	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
TL062MJGB	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
TL064ACD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL064ACDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL064ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL064BCD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL064BCDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL064BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL064CD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL064CDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL064CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL064CNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL064CPW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL064CPWLE	OBSOLETE	TSSOP	PW	14		None	Call TI	Call TI
TL064CPWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL064ID	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL064IDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL064IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL064MFK	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
TL064MFKB	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
TL064MJ	ACTIVE	CDIP	J	14	1	None	A42 SNPB	Level-NC-NC-NC
TL064MJB	ACTIVE	CDIP	J	14	1	None	A42 SNPB	Level-NC-NC-NC
TL064MWB	ACTIVE	CFP	W	14	1	None	A42 SNPB	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

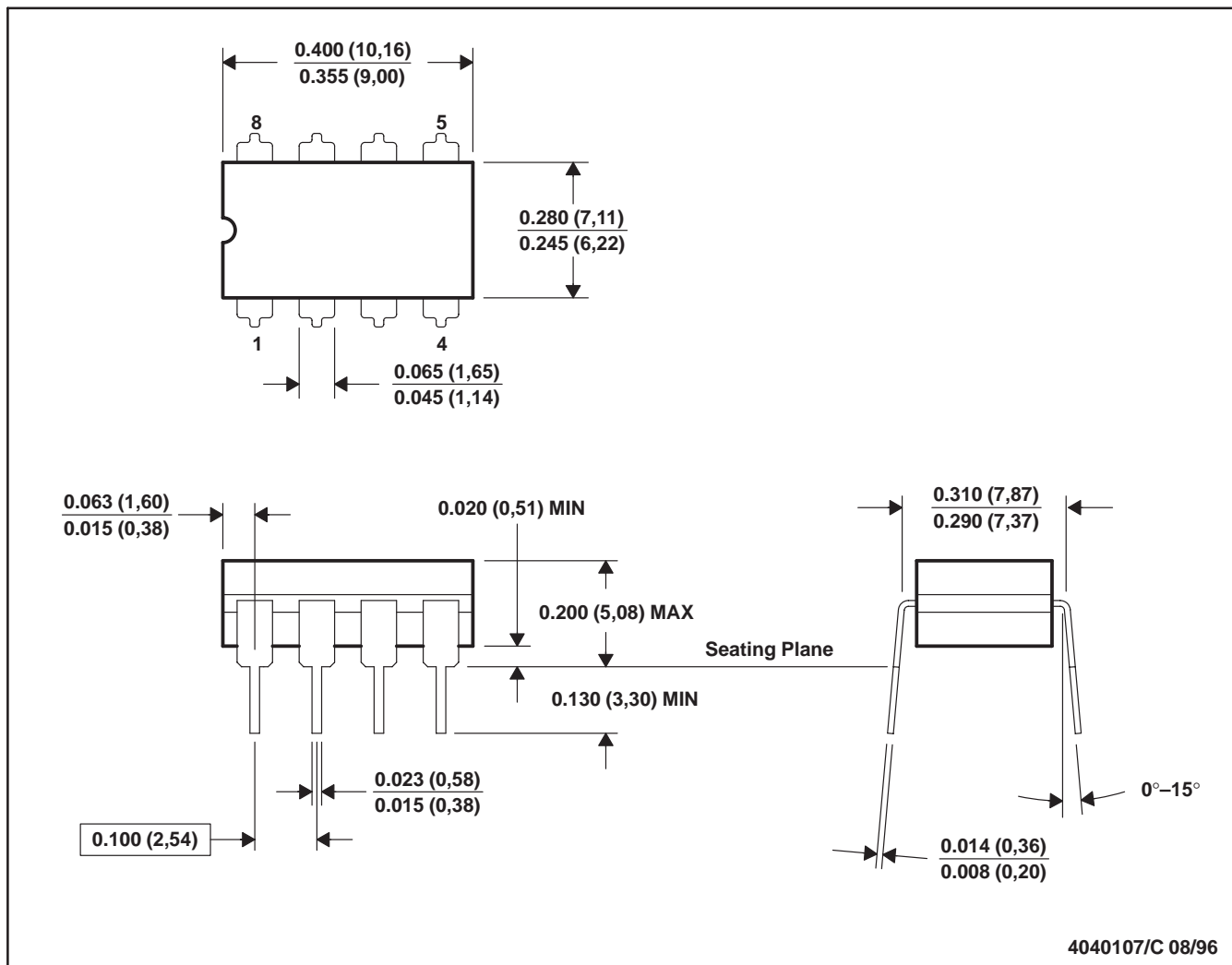
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

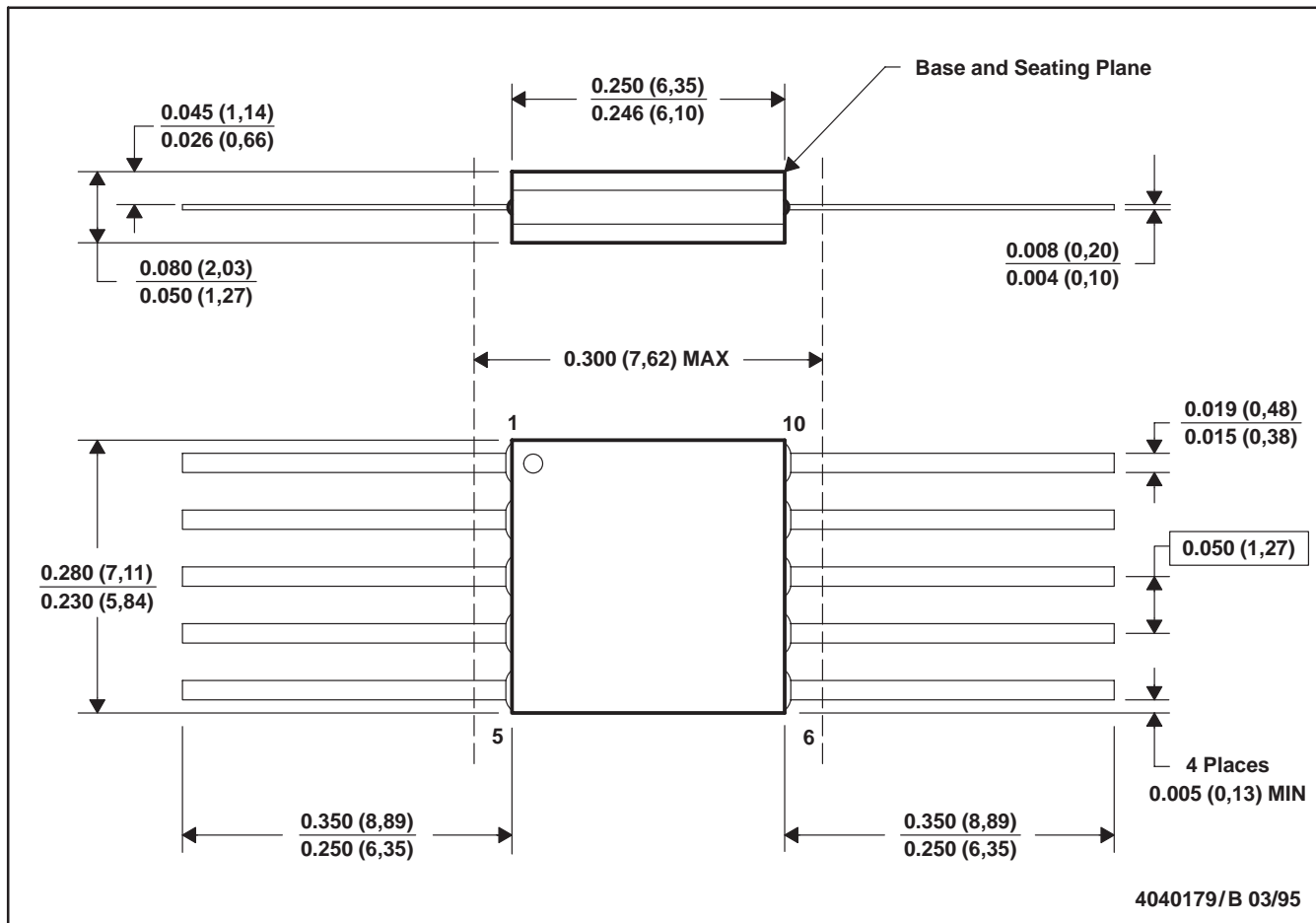


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

U (S-GDFP-F10)

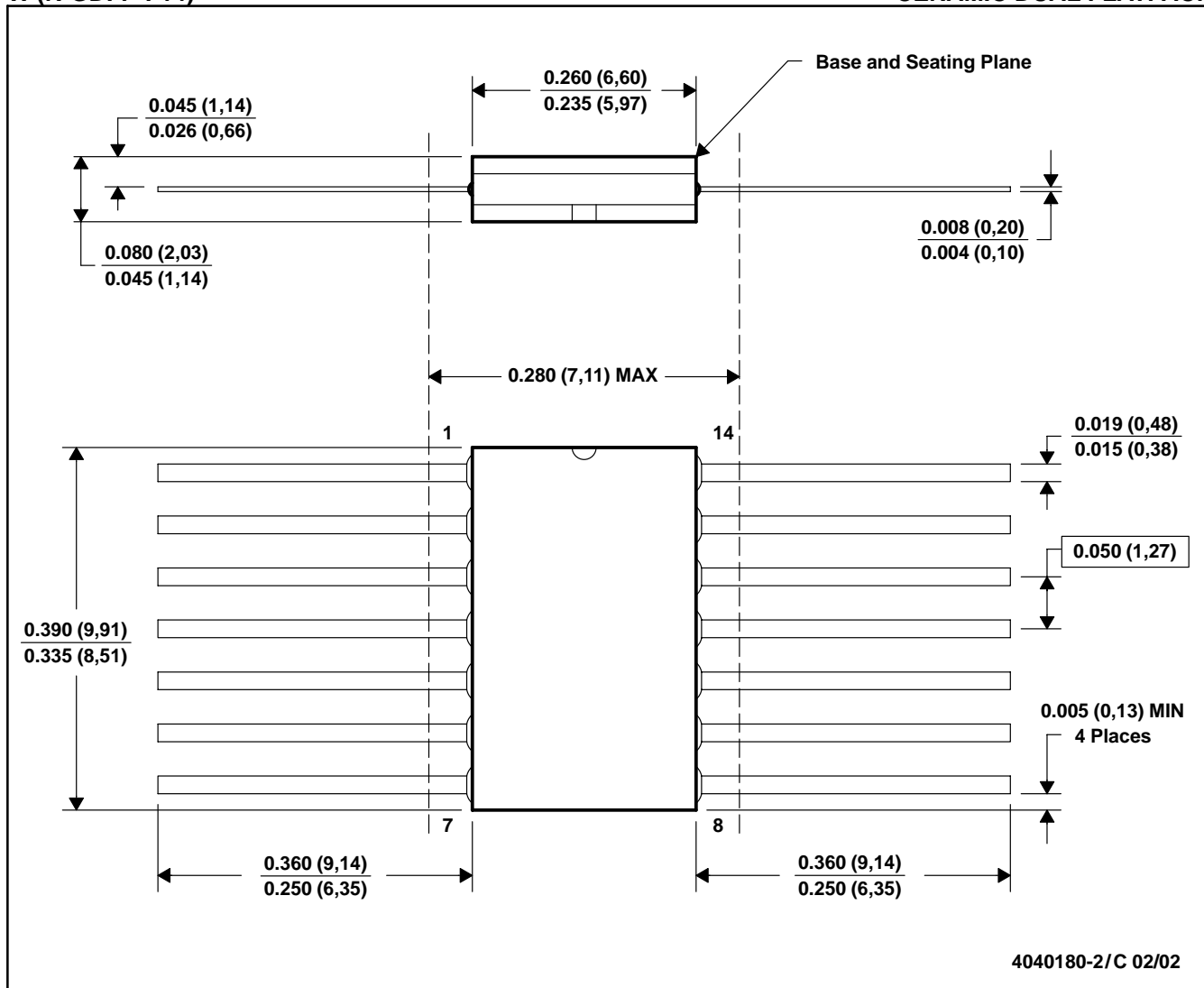
CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/C 02/02

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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