

# CD4017B, CD4022B Types

## CMOS Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4017B—Decade Counter with  
10 Decoded Outputs

CD4022B—Octal Counter with  
8 Decoded Outputs

■ CD4017B and CD4022B are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high-speed operation, 2-input decode-gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017B or every 8 clock input cycles in the CD4022B and is used to ripple-clock the succeeding device in a multi-device counting chain.

### Features:

- Fully static operation
- Medium-speed operation . . . 10 MHz (typ.) at  $V_{DD} = 10\text{ V}$
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Decade counter/decimal decode display (CD4017B)
- Binary counter/decoder
- Frequency division
- Counter control/timers
- Divide-by-N counting
- For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"

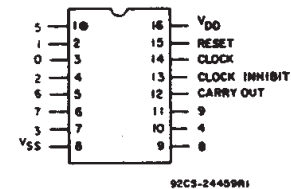
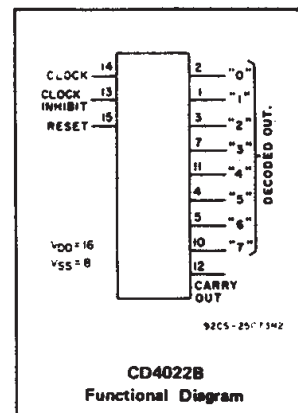
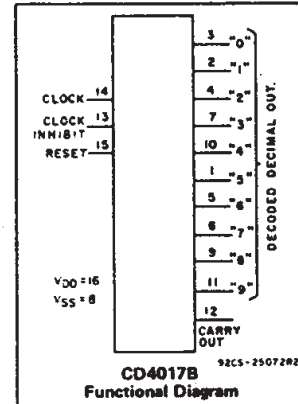
The CD4017B and CD4022B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic package (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4017B types also are supplied in 16-lead small-outline packages (M and M96 suffixes).

### RECOMMENDED OPERATING CONDITIONS

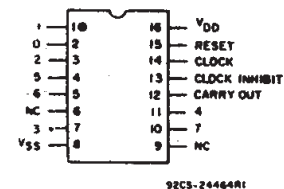
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	$V_{DD}$ (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)		3	18	V
Clock Input Frequency, $f_{CL}$	5	—	2.5	MHz
	10	—	5	
	15	—	5.5	
Clock Pulse Width, $t_W$	5	200	—	ns
	10	90	—	
	15	60	—	
Clock Rise & Fall Time, $t_{rCL}$ , $t_{fCL}$	5	UNLIMITED*		
	10			
	15			
Clock Inhibit Setup Time, $t_s$	5	230	—	ns
	10	100	—	
	15	70	—	
Reset Pulse Width, $t_{RW}$	5	260	—	ns
	10	110	—	
	15	60	—	
Reset Removal Time, $t_{rem}$	5	400	—	ns
	10	280	—	
	15	150	—	

\*Only if Pin 14 is used as the clock input. If Pin 13 is used as the clock input and Pin 14 is tied high (for advancing count on negative transition of the clock), rise and fall time should be  $\leq 15\ \mu\text{s}$ .



TOP VIEW  
CD4017B  
TERMINAL DIAGRAM



TOP VIEW  
NC - no connection  
CD4022B  
TERMINAL DIAGRAM

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# CD4017B, CD4022B Types

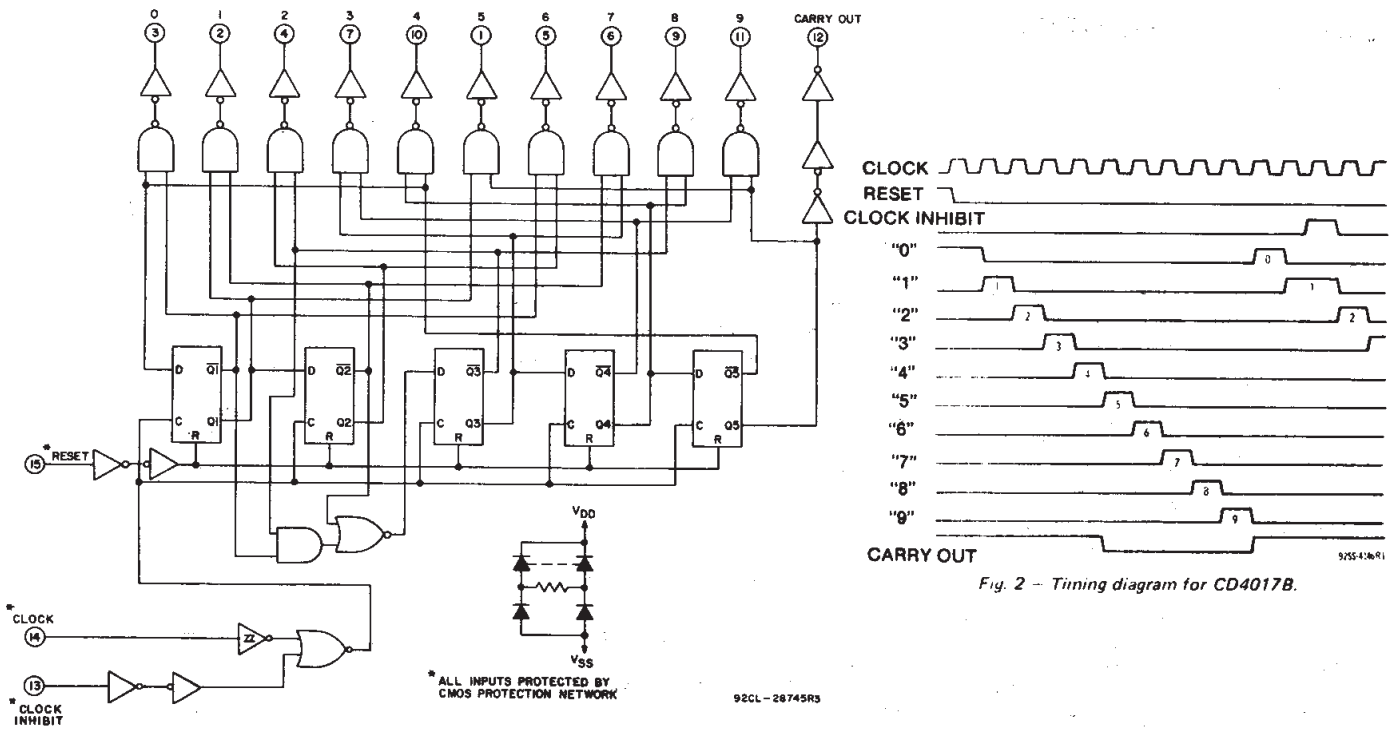


Fig. 2 - Timing diagram for CD4017B.

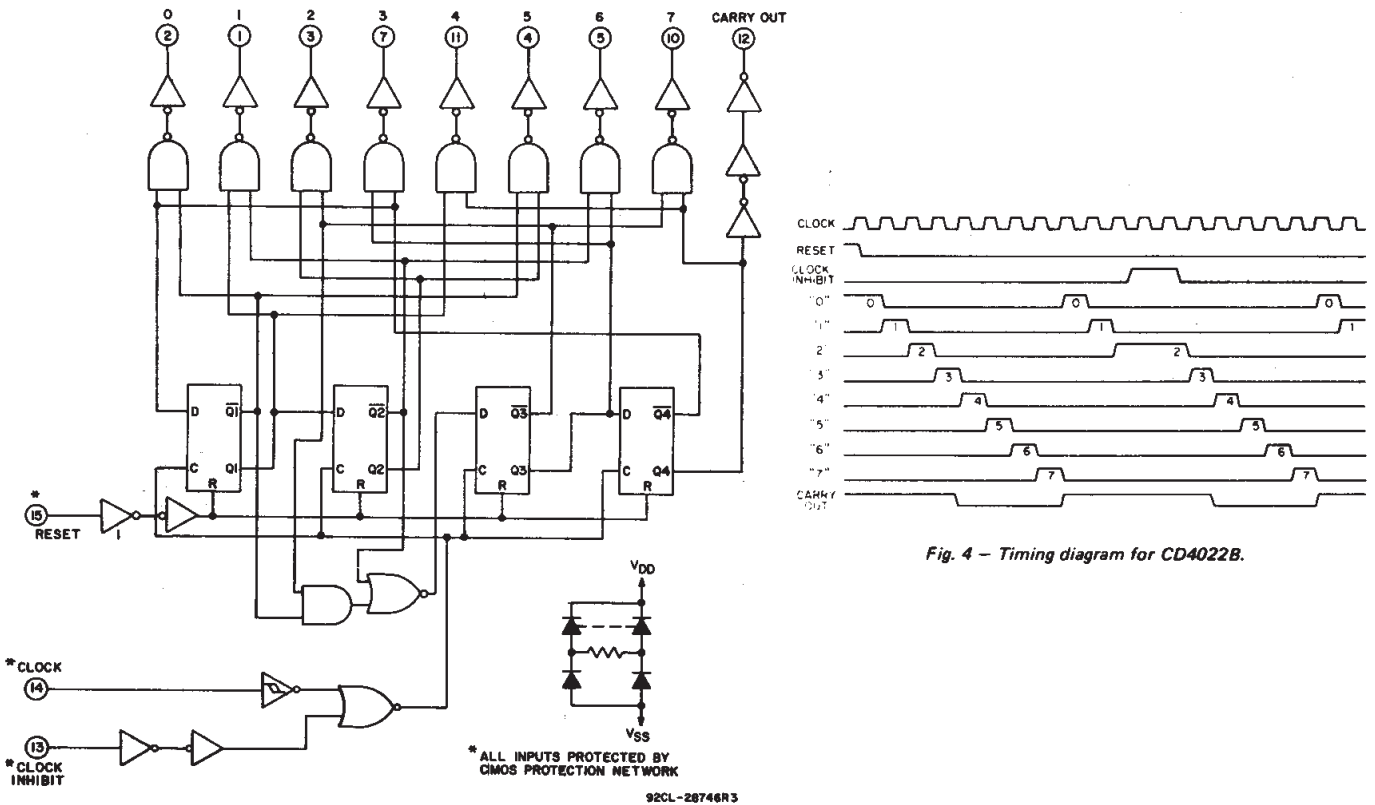


Fig. 4 - Timing diagram for CD4022B.

Fig. 3 - Logic diagram for CD4022B.

# CD4017B, CD4022B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10mA$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ C$ to $+100^\circ C$	500mW
For $T_A = +100^\circ C$ to $+125^\circ C$	Derate Linearity at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	$-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE ( $T_{sig}$ )	$-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max	$+265^\circ C$

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ( $^\circ C$ )							UNITS
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, $I_{DD}$ Max.	-	0.5	5	5	5	150	150	-	0.04	5	$\mu A$
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current $I_{OL}$ Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, $I_{OH}$ Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, $V_{OL}$ Max.	-	0.5	5	0.05				-	0	0.05	V
	-	0.10	10	0.05				-	0	0.05	
	-	0.15	15	0.05				-	0	0.05	
Output Voltage: High-Level, $V_{OH}$ Min.	-	0.5	5	4.95				4.95	5	-	V
	-	0.10	10	9.95				9.95	10	-	
	-	0.15	15	14.95				14.95	15	-	
Input Low Voltage $V_{IL}$ Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, $V_{IH}$ Min.	0.5, 4.5	-	5	3.5				3.5	-	-	V
	1.9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current $I_{IN}$ Max.	-	0.18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu A$

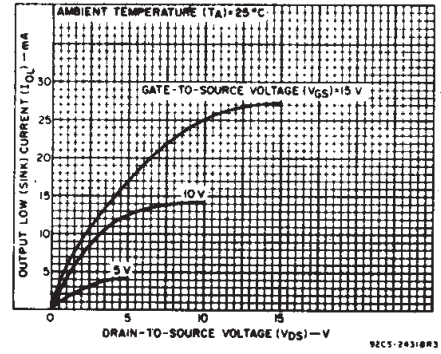


Fig. 5— Typical output low (sink) current characteristics.

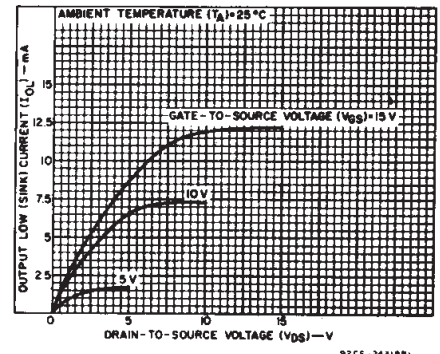


Fig. 6— Minimum output low (sink) current characteristics.

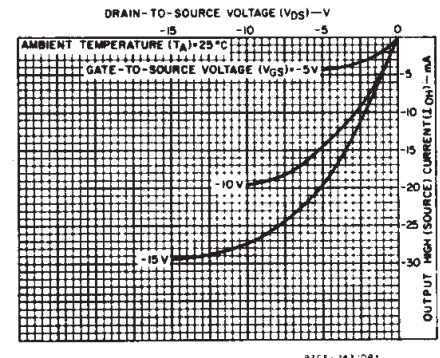


Fig. 7— Typical output high (source) current characteristics.

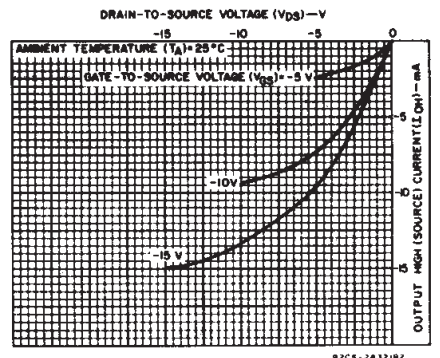


Fig. 8— Minimum output high (source) current characteristics.

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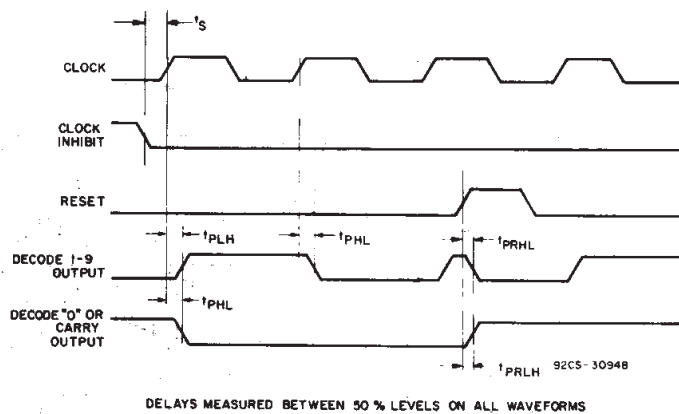
# CD4017B, CD4022B Types

## DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	CONDITIONS $V_{DD}$ (V)	LIMITS			UNITS
		Min.	Typ.	Max.	
<b>CLOCKED OPERATION</b>					
Propagation Delay Time, $t_{PHL}, t_{PLH}$ Decode Out	5	—	325	650	ns
	10	—	135	270	
	15	—	85	170	
Carry Out	5	—	300	600	ns
	10	—	125	250	
	15	—	80	160	
Transition Time, $t_{THL}, t_{TLH}$ Carry Out or Decode Out Line	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Maximum Clock Input Frequency, $f_{CL}^*$	5	2.5	5	—	MHz
	10	5	10	—	
	15	5.5	11	—	
Minimum Clock Pulse Width, $t_W$	5	—	100	200	ns
	10	—	45	90	
	15	—	30	60	
Clock Rise or Fall Time, $t_r, t_f$	5, 10, 15	UNLIMITED			
Minimum Clock Inhibit to Clock Setup Time, $t_s$	5	—	115	230	ns
	10	—	50	100	
	15	—	35	70	
Input Capacitance, $C_{IN}$	Any Input	—	5	—	pF
<b>RESET OPERATION</b>					
Propagation Delay Time, $t_{PHL}, t_{PLH}$ Carry Out or Decode Out Lines	5	—	265	530	ns
	10	—	115	230	
	15	—	85	170	
Minimum Reset Pulse Width, $t_W$	5	—	130	260	ns
	10	—	55	110	
	15	—	30	60	
Minimum Reset Removal Time	5	—	200	400	ns
	10	—	140	280	
	15	—	75	150	

\* Measured with respect to carry output line.



DELAYS MEASURED BETWEEN 50% LEVELS ON ALL WAVEFORMS

Fig. 9 - Propagation delay, setup, and reset removal time waveforms.

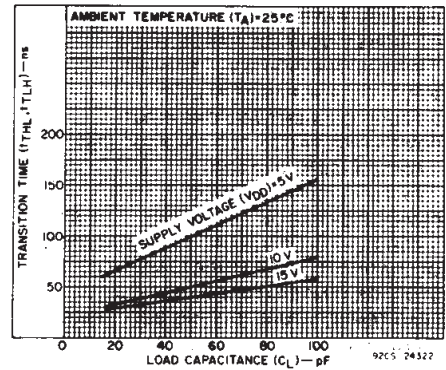


Fig. 10 - Typical transition time as a function of load capacitance.

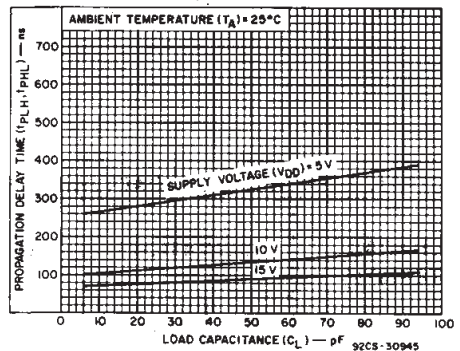


Fig. 11 - Typical propagation delay time as a function of load capacitance (clock to decode output).

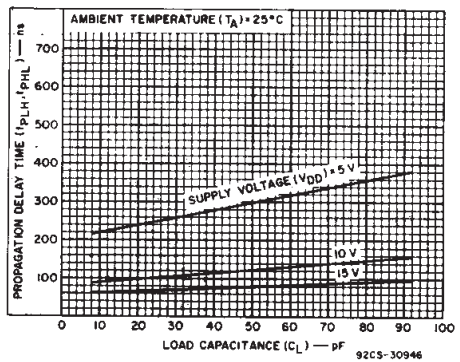


Fig. 12 - Typical propagation delay time as a function of load capacitance (clock to carry-out).

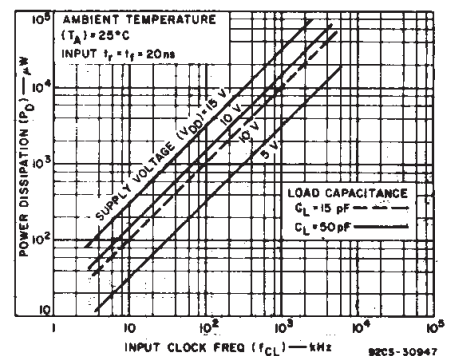


Fig. 13 - Typical dynamic power dissipation as a function of clock input frequency.

# CD4017B, CD4022B Types

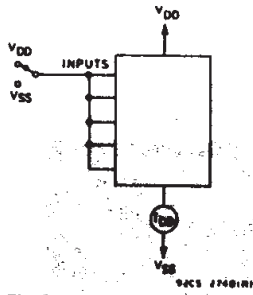


Fig. 14 - Quiescent device-current test circuit.

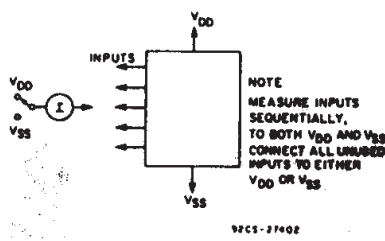


Fig. 15 - Input-leakage current.

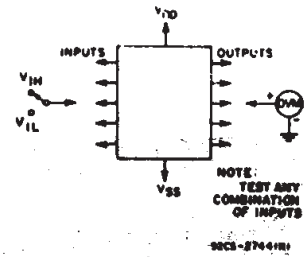


Fig. 16 - Input-voltage test circuit.

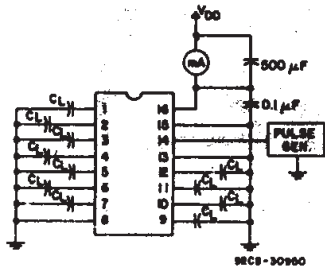


Fig. 17 - Dynamic power dissipation test circuit.

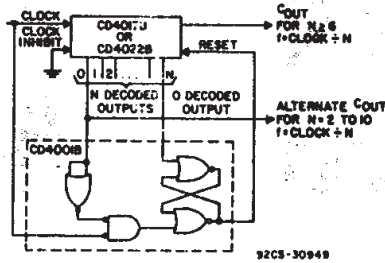


Fig. 18 - Divide by N counter ( $N \leq 10$ ) with N decoded outputs.

When the  $N^{\text{th}}$  decoded output is reached ( $N^{\text{th}}$  clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001B) generates a reset pulse which clears the CD4017B or CD4022B to its zero count. At this time, if the  $N^{\text{th}}$  decoded output is greater than or equal to 6 in the CD4017B or 5 in the CD4022B; the  $C_{OUT}$  line goes high to clock the next CD4017B or CD4022B counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip flop to enable the CD4017B or CD4022B. If the  $N^{\text{th}}$  decoded output is less than 6 (CD4017B) or 5 (CD4022B), the  $C_{OUT}$  line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

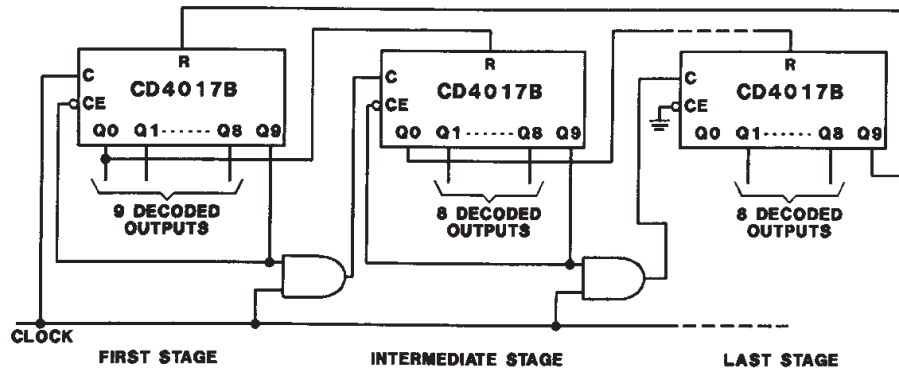
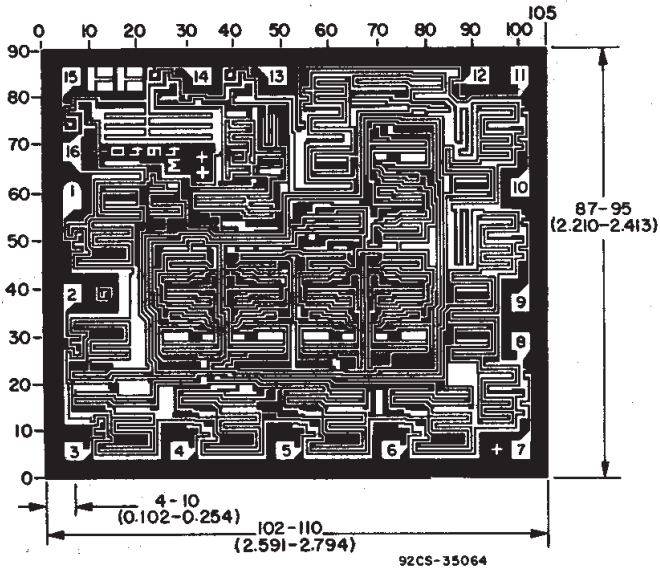


Fig. 19 - Cascading the CD4017B.

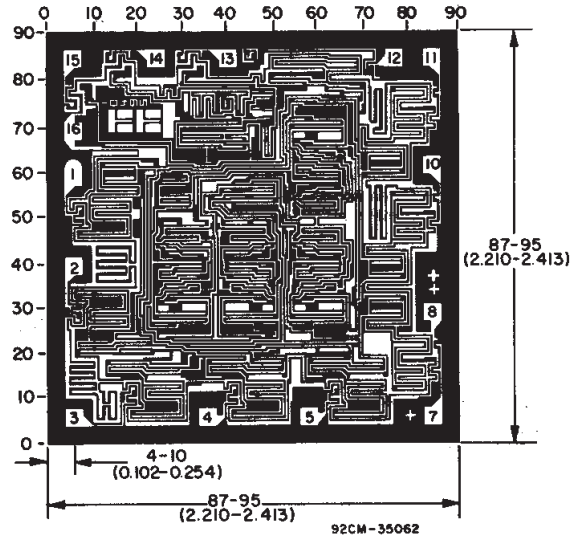
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# CD4017B, CD4022B Types

## CHIP DIMENSIONS AND PAD LAYOUTS



CD4017BH



CD4022BH

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).*

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
89270AKB3T	OBSOLETE			0		None	Call TI	Call TI
CD4017BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4017BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4017BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4017BM	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4017BM96	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4017BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4017BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4017BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4022BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4022BF	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4022BF3A	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC
CD4022BNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4022BPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4022BPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
JM38510/05651BEA	ACTIVE	CDIP	J	16	1	None	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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