



MULTI-CHANNEL LCD GAMMA CORRECTION BUFFER

FEATURES

- **Gamma Correction Channels: 10, 6**
- **Integrated V_{COM} Buffer**
- **Excellent Output Current Drive:**
 - **Gamma Channels: > 10mA**
 - **V_{COM} : > 100mA typ**
- **Large Capacitive Load Drive Capability**
- **Rail-to-Rail Output**
- **PowerPAD Package**
- **Low-Power/Channel: < 340uA**
- **Wide Supply Range: 4.5V to 16V**
- **Specified for 0°C to 85°C**
- **High ESD Rating: 4kV**

MODEL	GAMMA CHANNELS	VCOM CHANNELS
BUF11702	10	1
BUF07702	6	1

DESCRIPTION

The BUFxx702 are a series of multi-channel buffers targeted towards gamma correction in high-resolution LCD panels. The number of gamma correction channels required depends on a variety of factors and differs greatly from design to design. Therefore various channel options are offered. For additional space and cost savings, a V_{COM} channel with higher current drive capability is integrated in the BUF11702 and BUF07702.

The various buffers within the BUFxx702 are carefully matched to the voltage I/O requirements for the gamma correction application. Each buffer is capable of driving heavy capacitive loads and offers fast load current switching. The V_{COM} channel has increased output drive of > 100mA and can handle even larger capacitive loads.

The BUF07702 as well as the BUF11702 are available in the TSSOP-PowerPAD package for dramatically increased power dissipation capability. This way a large number of channels can be handled safely in one package.

A flow through pin out has been adopted to allow simple PCB routing and maintain the cost effectiveness of this solution. All inputs and outputs of the BUFxx702 incorporate internal ESD protection circuits that prevent functional failures at voltages up to 4kV (HBM) as tested under MIL-STD-883C Method 3015.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

PARAMETERS	BUFXX702	UNIT
Supply, V_{DD} ⁽²⁾	16.5	V
Input Voltage Range, V_I	V_{DD}	V
Continuous Total Power Dissipation	See Dissipation Rating Table	
Operating Free-Air Temperature Range, T_A	0 to 85	°C
Maximum Junction Temperature, T_J	150	°C
Storage Temperature Range, T_{STG}	-65 to 150	°C
Lead Temperature 1.6mm (1/16 inch) from Case for 10s	260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
BUF11702	TSSOP-28	PWP	0°C to +85°C	BUF11702PWP	Tube, 50
BUF11702	TSSOP-28	PWP	0°C to +85°C	BUF11702PWPR	Reels, 2000
BUF07702	TSSOP-20	PWP	0°C to +85°C	BUF07702PWP	Tube, 70
BUF07702	TSSOP-20	PWP	0°C to +85°C	BUF07702PWPR	Reels, 2000

(1) For the most current specification and package information, refer to our web site at www.ti.com.

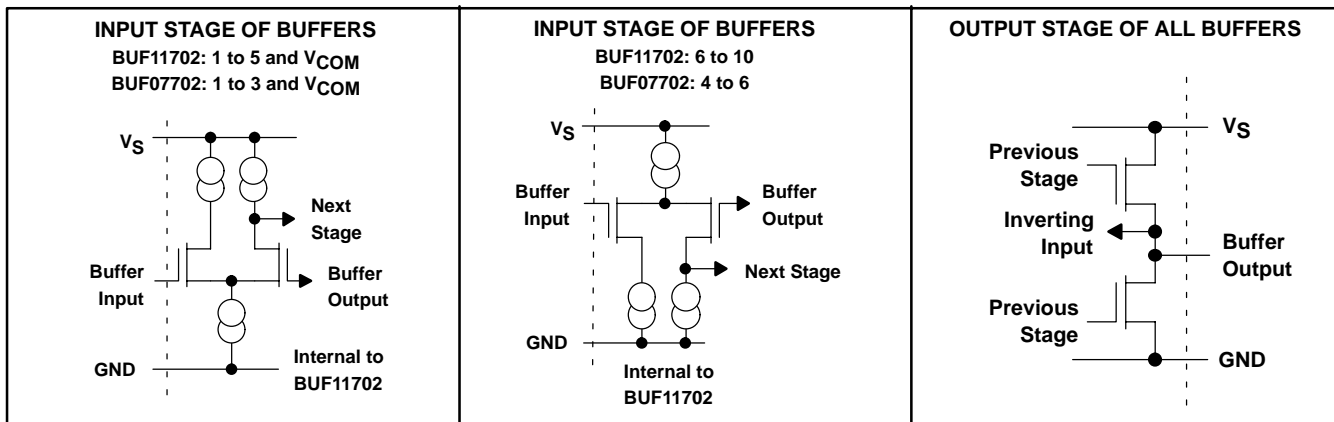
DISSIPATION RATING TABLE

PACKAGE TYPE	PACKAGE DESIGNATOR	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING
TSSOP-28	PWP (28)	0.72	27.9	4.3 W
TSSOP-20	PWP (20)	1.40	26.1	4.79 W

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	4.5		16	V
Operating Free-Air Temperature, T_A	0		85	°C

EQUIVALENT SCHEMATICS OF INPUTS AND OUTPUTS



ELECTRICAL CHARACTERISTICS

 over operating free-air temperature range, $V_{DD} = 4.5V$ to $16V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	$T_A \uparrow$	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		$V_I = V_{DD}/2$, $R_S = 50 \Omega$	25°C		1.5	12	mV
				Full Range(1)			15	
I_{IB}	Input bias current		$V_I = V_{DD}/2$	25°C		1		pA
				Full Range(1)		200		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 4.5 V$ to $16 V$	25°C	62	80		dB
				Full Range(1)	60			
Buffer gain			$V_I = 5 V$	25°C		0.9995		V/V
BW_3dB	3dB Bandwidth	Gamma Buffers VCOM Buffer	$C_L = 100pF$ $R_L = 2k\Omega$	25°C		1 0.6		MHz
SR	Slew Rate	Gamma Buffers VCOM Buffer	$C_L = 100pF$, $R_L = 2k\Omega$ $V_{IN} = 2V$ to $8V$	25°C		1 0.7		V/ μs
	Transient Load Regulation		$I_O = 0$ to $\pm 5mA$ $V_O = 5V$ $C_L = 100pF$ $t_T = 0.1\mu s$	25°C		900		mV
	Transient Load Response		See Figure 2	25°C		160		mV
t_S (I-sink)	Settling Time–Current		$I_O = 0$ to $-5mA$ $V_O = 5V$ $C_L = 100pF$ $R_L = 2k\Omega$	Full Range(1)		1		μs
t_S (I-src)	Settling Time–Current		$I_O = 0$ to $+5mA$ $V_O = 5V$ $C_L = 100pF$ $R_L = 2k\Omega$	Full Range(1)		2		μs
t_S	Settling Time–Voltage	Gamma Buffers	$V_I = 4.5V$ to $5.5V$ 0.1% $V_I = 5.5V$ to $4.5V$ 0.1%	25°C		6 4.6		μs
		VCOM Buffer	$V_I = 4.5V$ to $5.5V$ 0.1% $V_I = 5.5V$ to $4.5V$ 0.1%			5.8 5.6		μs
V_n	Noise Voltage	Gamma Buffers VCOM Buffer	$V_I = 5V$ $f = 1kHz$	25°C		45 40		nV/Hz
		Crosstalk		$V_{IP-P} = 6V$, $f = 1kHz$	25°C		85	

 (1) Full Range is $0^\circ C$ to $85^\circ C$.

ELECTRICAL CHARACTERISTICS: BUF07702

over operating free-air temperature range, $V_{DD} = 4.5V$ to $16V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT	
I_{DD}	Supply Current	ALL	$V_O = V_{DD}/2, V_I = V_{DD}/2$ $V_{DD} = 10V$	25°C	2.5	3.7	mA	
				Full Range		5.5	mA	
Common Mode Input Range	Buffers 1–3		25°C	1		V_{DD}	V	
	Buffers 4–6			0	$V_{DD}-1$			
	V_{COM} Buffer			1	V_{DD}			
Load regulation	V_{COM} buffer sinking	$V_{DD} = 10V,$ $I_O = 1mA$ to $30mA$	25°C	1	1.2	mV/mA		
			Full Range		2.5			
	V_{COM} buffer sourcing	$V_{DD} = 10V,$ $I_O = -1mA$ to $-30mA$	25°C	1	1.2			
			Full Range		2.5			
	Buffers 1–6 sinking	$V_{DD} = 10V,$ $I_O = 1mA$ to $30mA$	25°C	0.85	1			
			Full Range		1.5			
	Buffers 1–6 sourcing	$V_{DD} = 10V,$ $I_O = -1mA$ to $-30mA$	25°C	0.85	1			
			Full Range		1.5			
V_{OSH1}	High-level saturated output voltage	Buffer 1	$V_{DD} = 16V,$ $V_I = 16V$	$I_O = -5mA,$	25°C	15.85	15.9	V
					Full range	15.8		
V_{OSL6}	Low-level saturated output voltage	Buffer 6	$V_{DD} = 16V,$ $V_I = 16V$	$I_O = 5mA,$	25°C	0.1	0.15	V
					Full range	0.2		
V_{OH1}	High-level output voltage	Buffer 1	$V_{DD} = 10V,$ $V_I = 9.8V$	$I_O = -10mA,$	25°C	9.75	9.8	V
					Full range	9.7		
$V_{OH2/3}$		Buffer 2/3	$V_{DD} = 10V,$ $V_I = 9.5V$	$I_O = -10mA,$	25°C	9.45	9.5	V
					Full range	9.4		
$V_{OH4/5}$		Buffer 4/5	$V_{DD} = 10V,$ $V_I = 8V$	$I_O = -10mA,$	25°C	7.95	8	V
					Full range	7.9		
V_{OH6}		Buffer 6	$V_{DD} = 10V,$ $V_I = 8V$	$I_O = -10mA,$	25°C	7.95	8	V
					Full range	7.9		
V_{OHCOM}		V_{COM} Buffer	$V_{DD} = 10V,$ $V_I = 8V$	$I_O = -30mA,$	25°C	7.95	8	V
					Full range	7.9		
V_{OL1}	Low-level output voltage	Buffer 1	$V_{DD} = 10V,$ $V_I = 2V$	$I_O = 10mA,$	25°C	2	2.05	V
					Full range	2.1		
$V_{OL2/3}$		Buffer 2/3	$V_{DD} = 10V,$ $V_I = 2V$	$I_O = 10mA,$	25°C	2	2.05	V
					Full range	2.1		
$V_{OL4/5}$		Buffer 4/5	$V_{DD} = 10V,$ $V_I = 0.5V$	$I_O = 10mA,$	25°C	0.5	0.55	V
					Full range	0.6		
V_{OL6}		Buffer 6	$V_{DD} = 10V,$ $V_I = 0.2V$	$I_O = 10mA,$	25°C	0.2	0.25	V
					Full range	0.3		
V_{OLCOM}		V_{COM} Buffer	$V_{DD} = 10V,$ $V_I = 2V$	$I_O = 30mA,$	25°C	2	2.05	V
					Full range	2.1		

(1) Full Range is 0°C to 85°C.

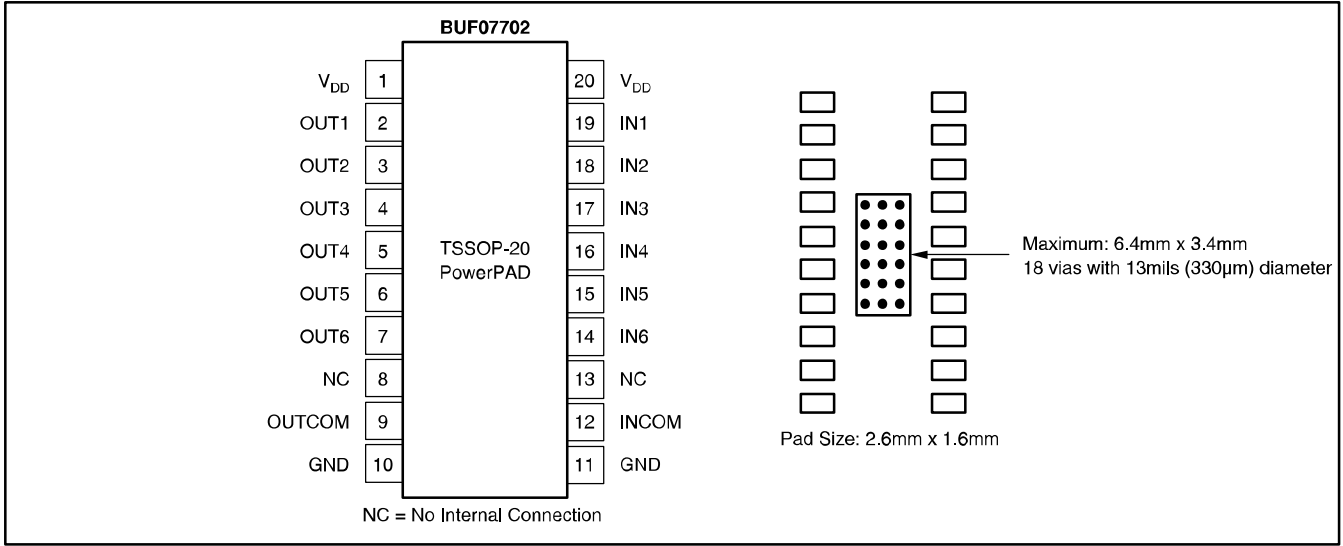
ELECTRICAL CHARACTERISTICS: BUF11702

 over operating free-air temperature range, $V_{DD} = 4.5V$ to $16V$, $T_A = 25^\circ C$, unless otherwise noted.

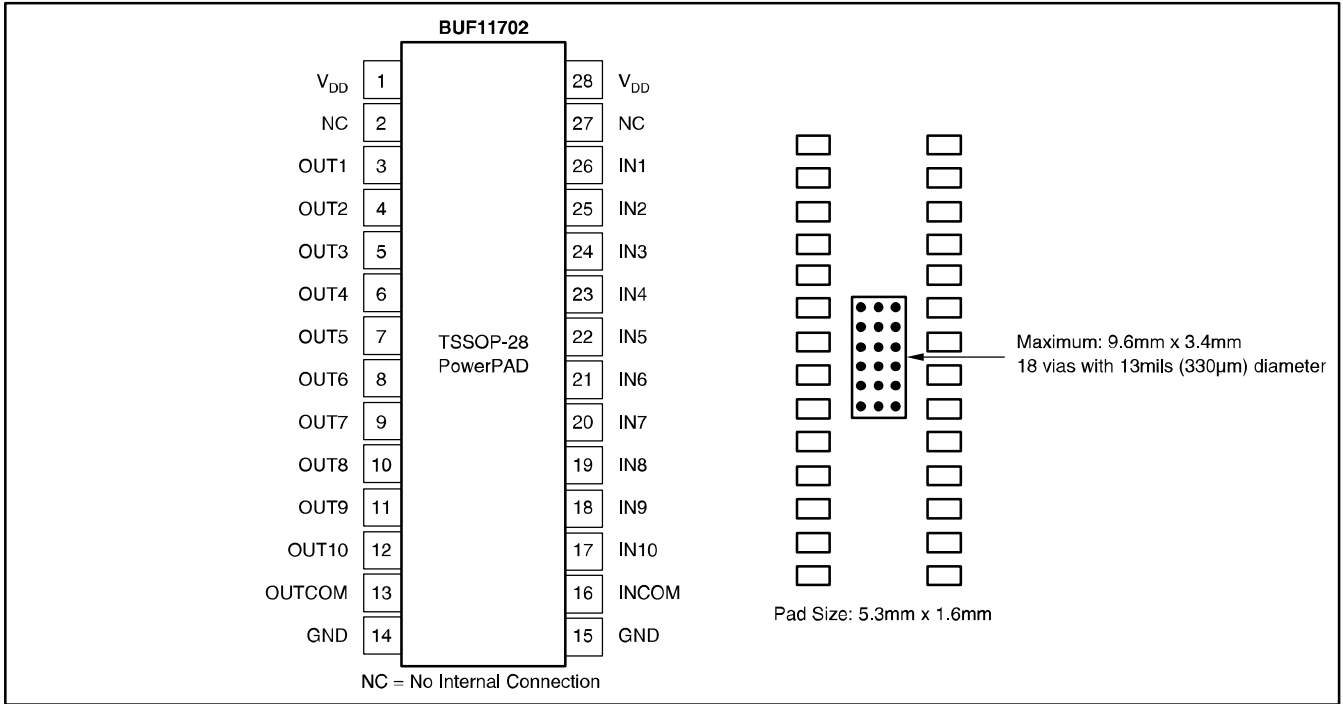
PARAMETER		TEST CONDITIONS	$T_A^{(1)}$	MIN	TYP	MAX	UNIT	
I_{DD}	Supply Current	ALL	$V_O = V_{DD}/2$, $V_I = V_{DD}/2$ $V_{DD} = 10V$	25°C	2.5	3.7	mA	
				Full Range		5.5		
Common Mode Input Range	Buffers 1–10		25°C	1		V_{DD}	V	
	Buffers 1–10			0		$V_{DD}-1$		
	V_{COM} Buffer			1		V_{DD}		
Load regulation	V_{COM} Buffer Sinking	$V_{DD} = 10V$, $I_O = 1mA$ to $30mA$	25°C	1		1.2	mV/mA	
			Full Range			2.5		
	V_{COM} Buffer Sourcing	$V_{DD} = 10V$, $I_O = -1mA$ to $-30mA$	25°C	1		1.2		
			Full Range			2.5		
	Buffers 1–10 sinking	$V_{DD} = 10V$, $I_O = 1mA$ to $30mA$	25°C	0.85		1		
			Full Range			1.5		
Buffers 1–10 sourcing	$V_{DD} = 10V$, $I_O = -1mA$ to $-30mA$	25°C	0.85		1			
		Full Range			1.5			
V_{OSH1}	High-level saturated output voltage	Buffer 1	$V_{DD} = 16V$, $V_I = 16V$	$I_O = -10mA$,	25°C	15.85	15.9	V
					Full range	15.8		
V_{OSL6}	Low-level saturated output voltage	Buffer 10	$V_{DD} = 16V$, $V_I = 16V$	$I_O = 10mA$,	25°C	0.1	0.15	V
					Full range		0.2	
V_{OH1}	High-level output voltage	Buffer 1	$V_{DD} = 10V$, $V_I = 9.8V$	$I_O = -10mA$,	25°C	9.75	9.8	V
					Full range	9.7		
$V_{OH2/3/4/5}$		Buffer 2/3/4/5	$V_{DD} = 10V$, $V_I = 9.5V$	$I_O = -10mA$,	25°C	9.45	9.5	V
					Full range	9.4		
$V_{OH6/7/8/9}$		Buffer 6/7/8/9	$V_{DD} = 10V$, $V_I = 8V$	$I_O = -10mA$,	25°C	7.95	8	V
					Full range	7.9		
V_{OH10}		Buffer 10	$V_{DD} = 10V$, $V_I = 8V$	$I_O = -10mA$,	25°C	7.95	8	V
					Full range	7.9		
V_{OHCOM}		V_{COM} Buffer	$V_{DD} = 10V$, $V_I = 8V$	$I_O = -30mA$,	25°C	7.95	8	V
					Full range	7.9		
V_{OL1}	Low-level output voltage	Buffer 1	$V_{DD} = 10V$, $V_I = 2V$	$I_O = 10mA$,	25°C	2	2.05	V
					Full range		2.1	
$V_{OL2/3/4/5}$		Buffer 2/3/4/5	$V_{DD} = 10V$, $V_I = 2V$	$I_O = 10mA$,	25°C	2	2.05	V
					Full range		2.1	
$V_{OL6/7/8/9}$		Buffer 6/7/8/9	$V_{DD} = 10V$, $V_I = 0.5V$	$I_O = 10mA$,	25°C	0.5	0.55	V
					Full range		0.6	
V_{OL10}		Buffer 10	$V_{DD} = 10V$, $V_I = 0.2V$	$I_O = 10mA$,	25°C	0.2	0.25	V
					Full range		0.3	
V_{OLCOM}		V_{COM} Buffer	$V_{DD} = 10V$, $V_I = 2V$	$I_O = 30mA$,	25°C	2	2.05	V
					Full range		2.1	

(1) Full Range is 0°C to 85°C.

BUF07702 Pin Configuration



BUF11702 Pin Configuration



PARAMETER MEASUREMENT INFORMATION

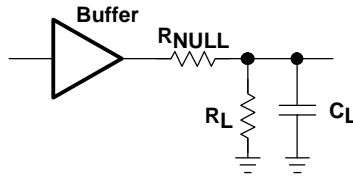
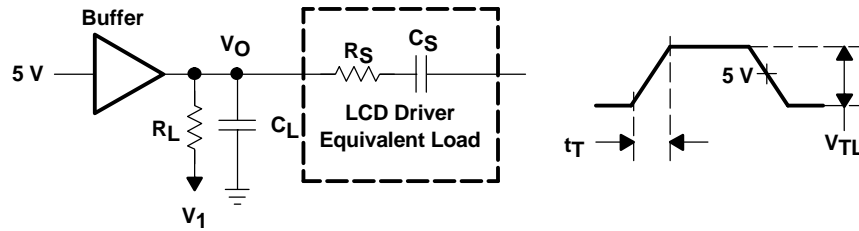


Figure 1. Bandwidth and Phase Shift Test Circuit



Test		V ₁	V _{TL}	t _T	C _S	R _S	C _L	R _L
Source	Ch1–Ch10	0 V	2 V	0.1 μs	100 pF	100 Ω	100 pF	1 kΩ
Sink	Ch1–Ch10	10 V	2 V	0.1 μs	100 pF	100 Ω	100 pF	1 kΩ

Figure 2. Transient Load Response Test Circuit

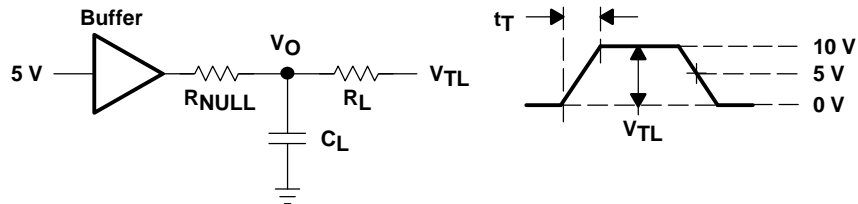


Figure 3. Transient Load Regulation Test Circuit

TYPICAL CHARACTERISTICS

DC CURVES

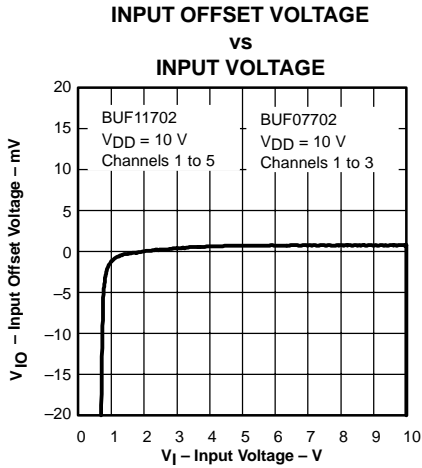


Figure 4

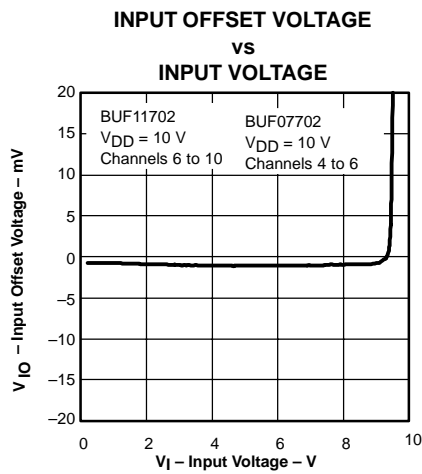


Figure 5

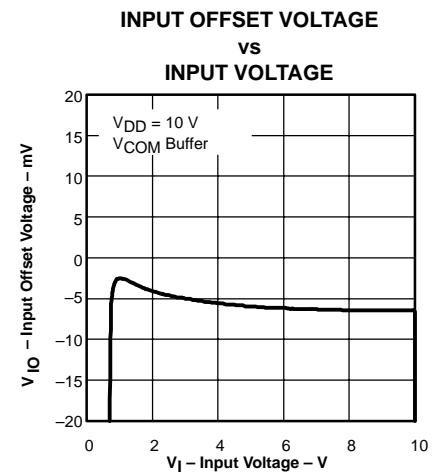


Figure 6

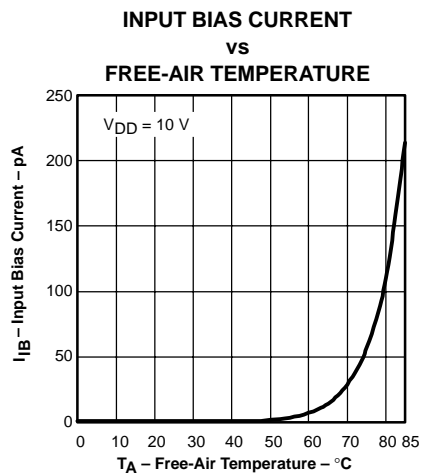


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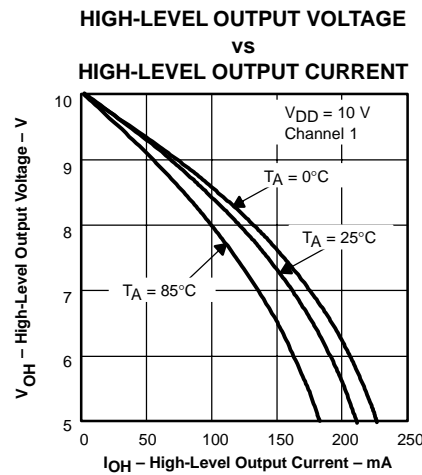


Figure 8

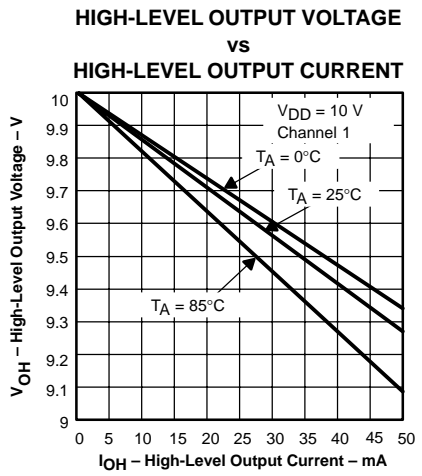


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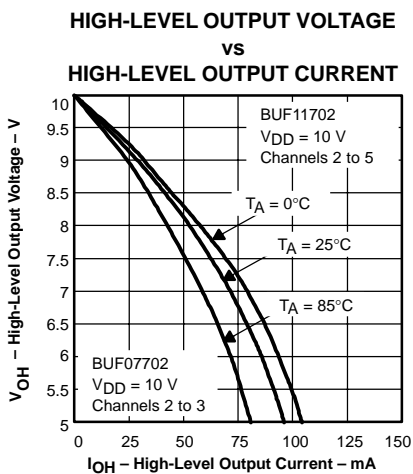


Figure 10

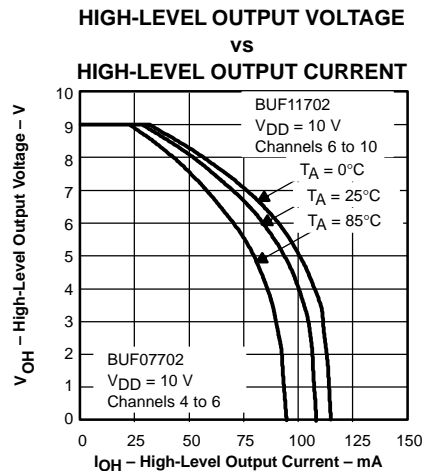


Figure 11

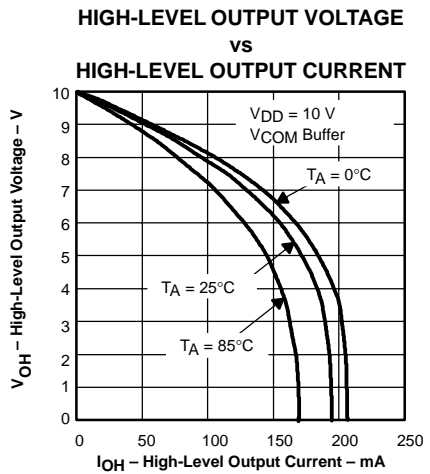


Figure 12

TYPICAL CHARACTERISTICS

DC CURVES (CONTINUED)

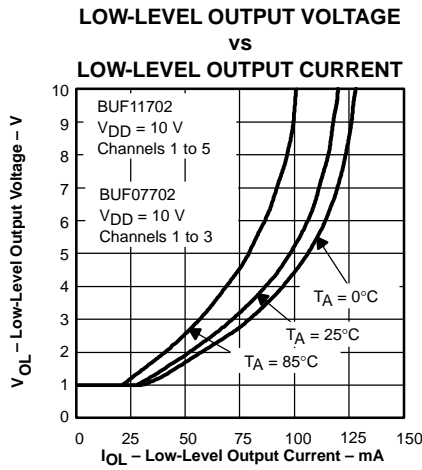


Figure 13

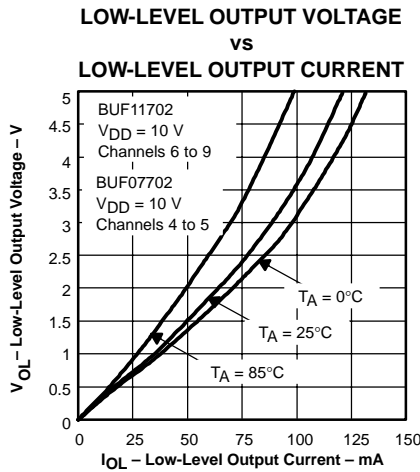


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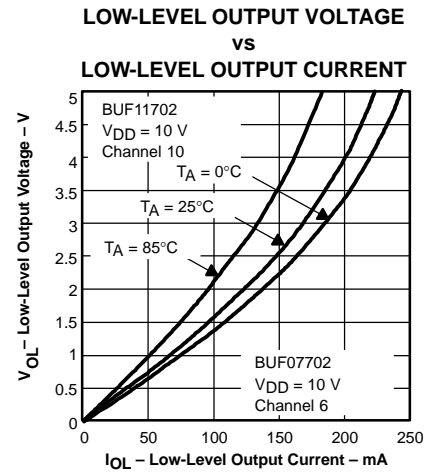


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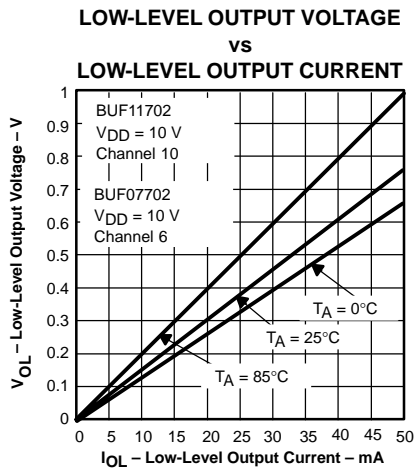


Figure 16

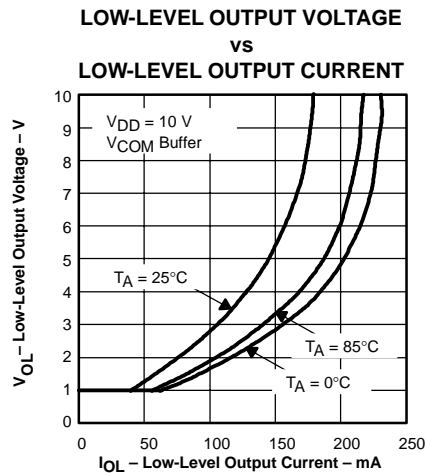


Figure 17

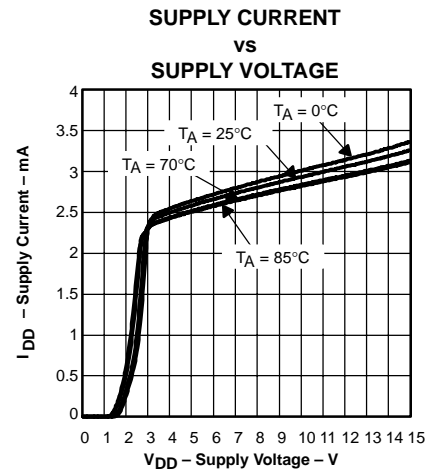


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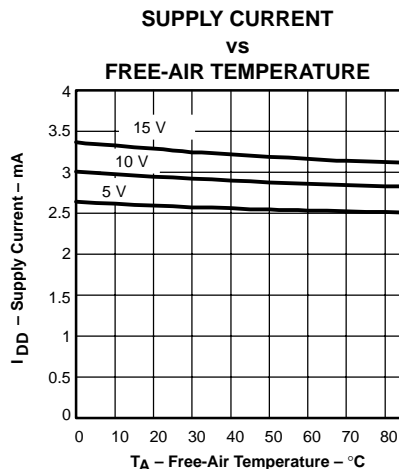


Figure 19

TYPICAL CHARACTERISTICS

AC CURVES

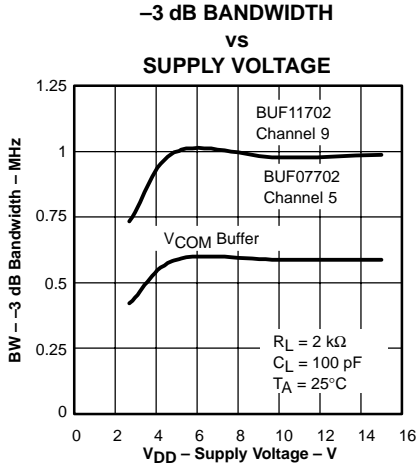


Figure 20

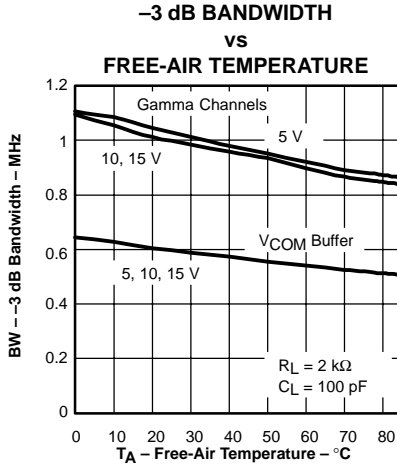


Figure 21

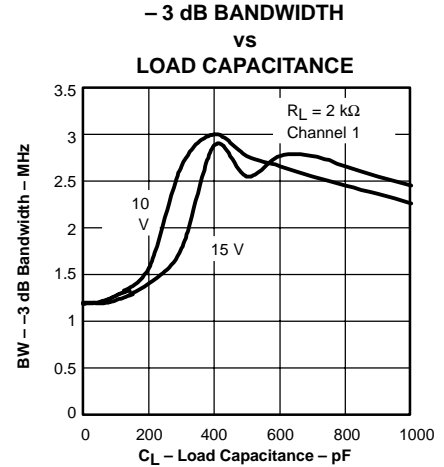


Figure 22

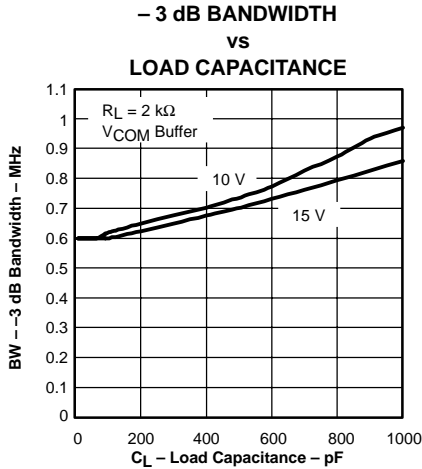


Figure 23

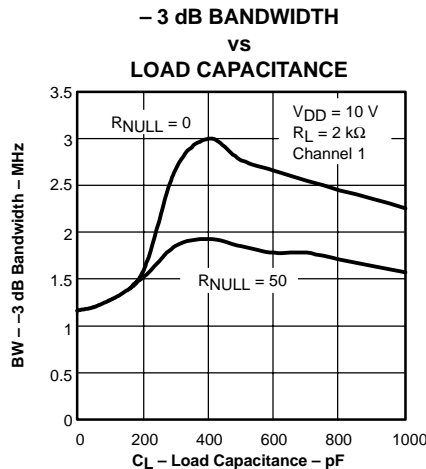


Figure 24

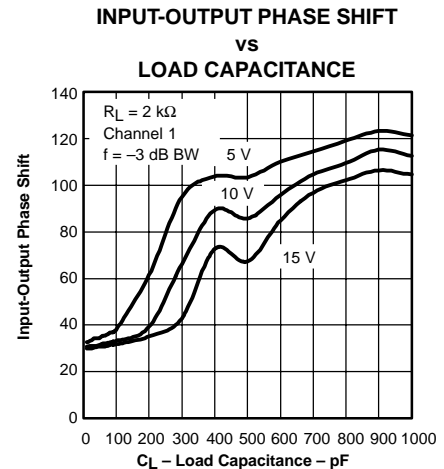


Figure 25

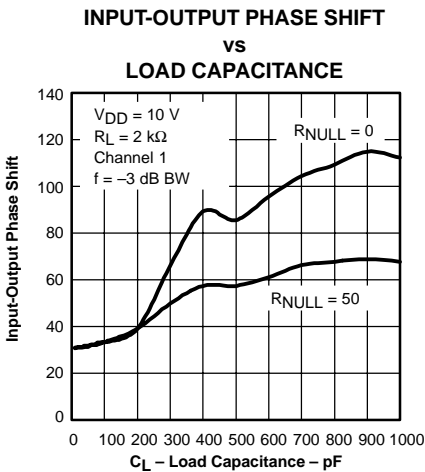


Figure 26

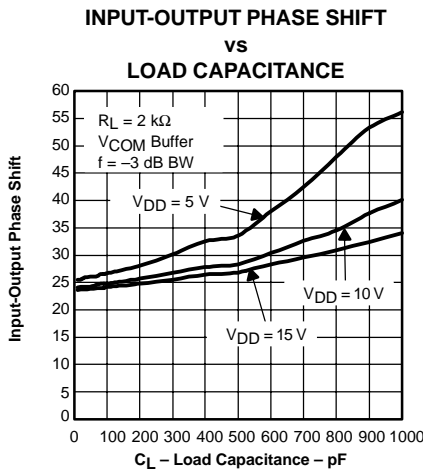


Figure 27

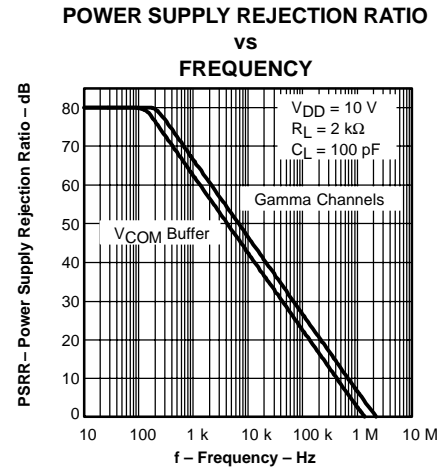


Figure 28

TYPICAL CHARACTERISTICS

AC CURVES (CONTINUED)

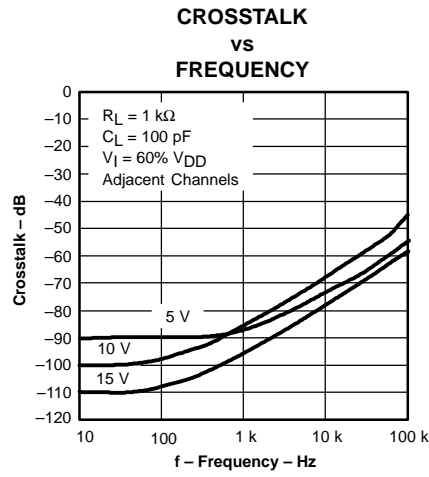


Figure 29

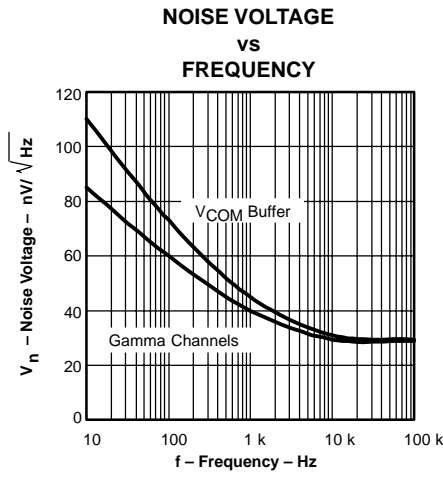


Figure 30

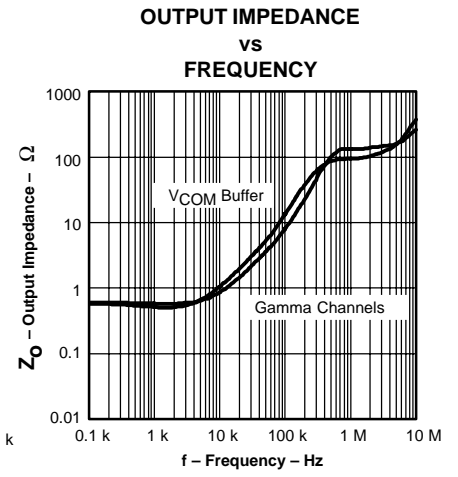


Figure 31

TYPICAL CHARACTERISTICS

TRANSIENT CURVES

SUPPLY VOLTAGE, OUTPUT VOLTAGE AND SUPPLY CURRENT

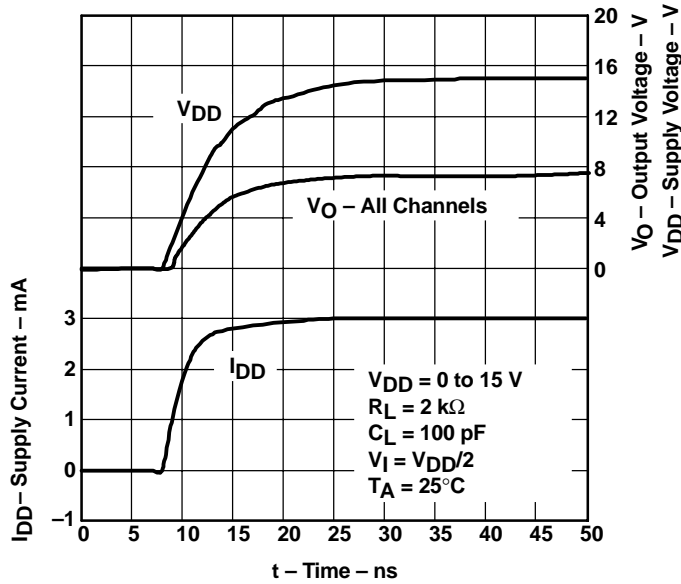


Figure 32

LARGE SIGNAL VOLTAGE FOLLOWER

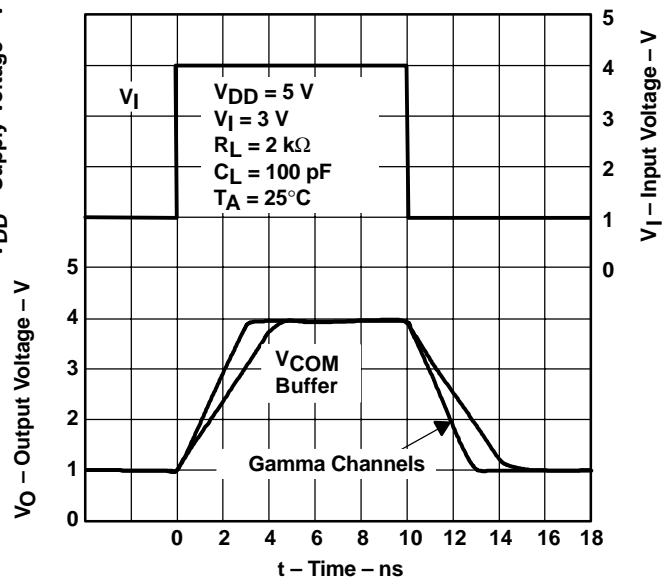


Figure 33

LARGE SIGNAL VOLTAGE FOLLOWER

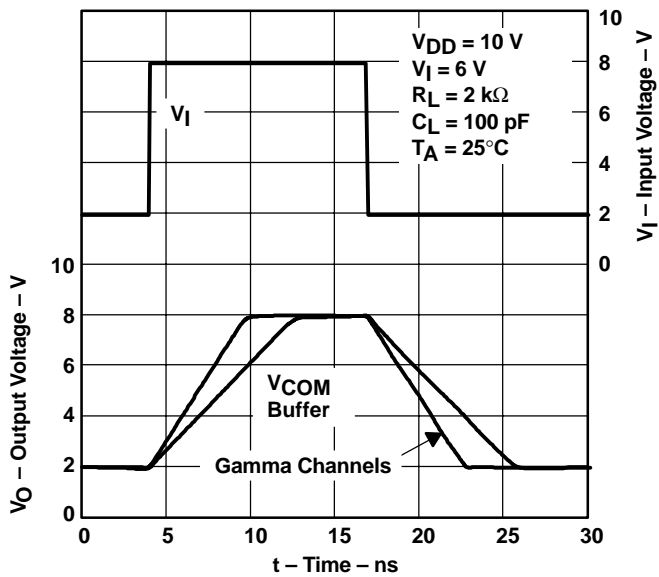


Figure 34

LARGE SIGNAL VOLTAGE FOLLOWER

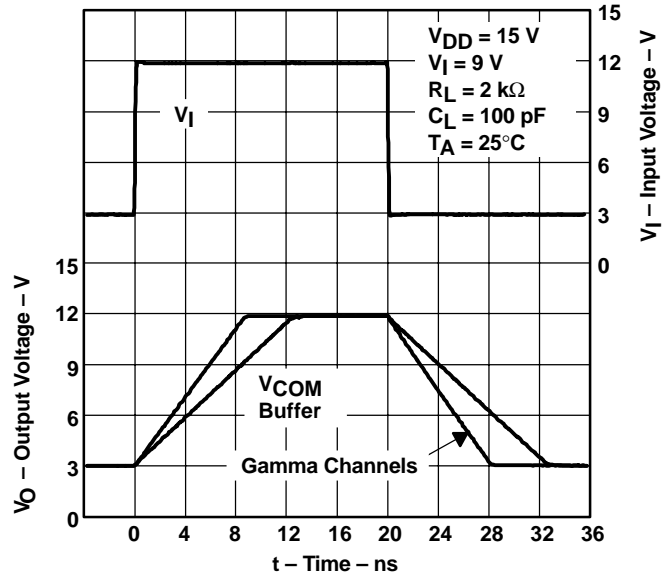


Figure 35

TYPICAL CHARACTERISTICS

TRANSIENT CURVES (CONTINUED)

SMALL SIGNAL VOLTAGE FOLLOWER

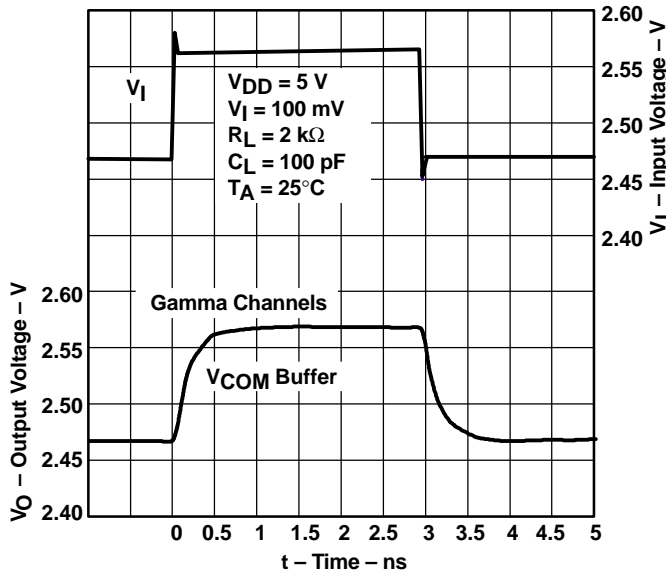


Figure 36

SMALL SIGNAL PULSE RESPONSE

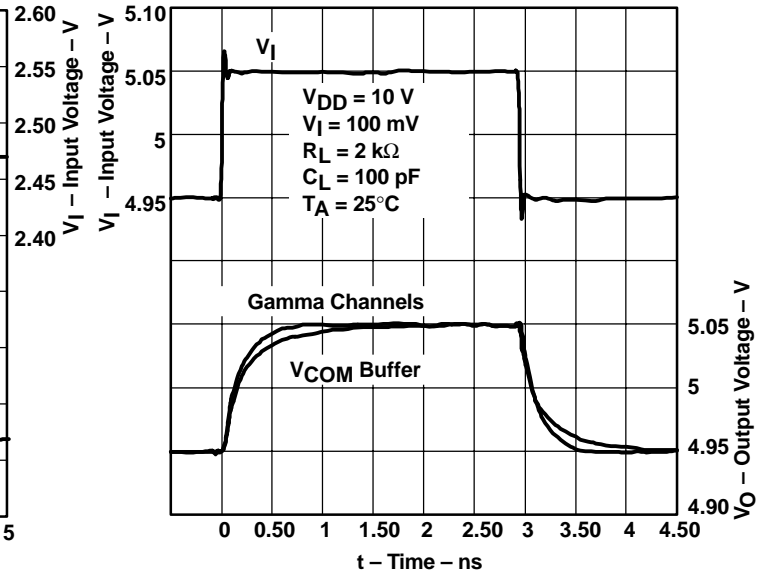


Figure 37

SMALL SIGNAL VOLTAGE FOLLOWER

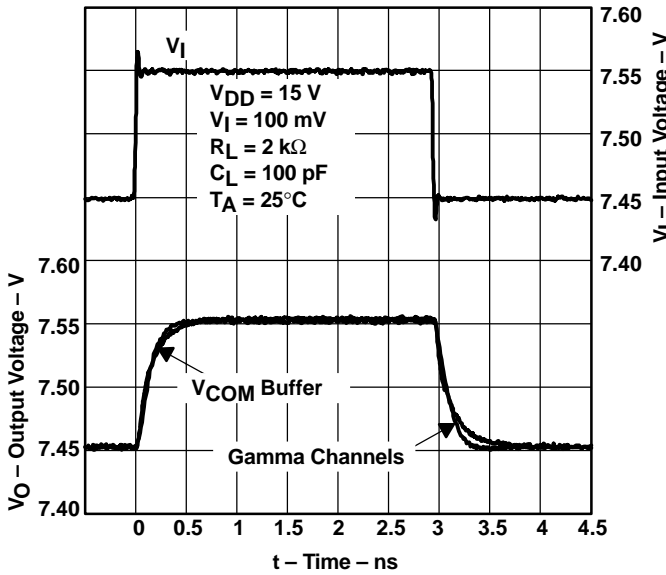


Figure 38

TRANSIENT LOAD RESPONSE – SOURCING

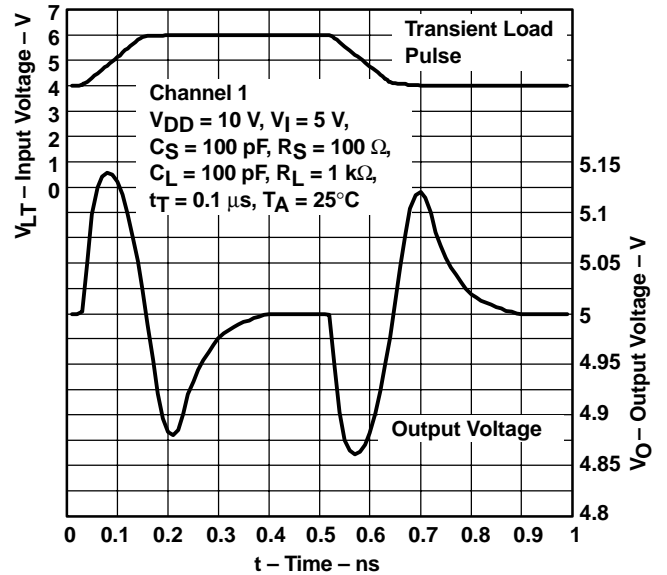


Figure 39

TYPICAL CHARACTERISTICS

TRANSIENT CURVES (CONTINUED)

TRANSIENT LOAD RESPONSE – SINKING

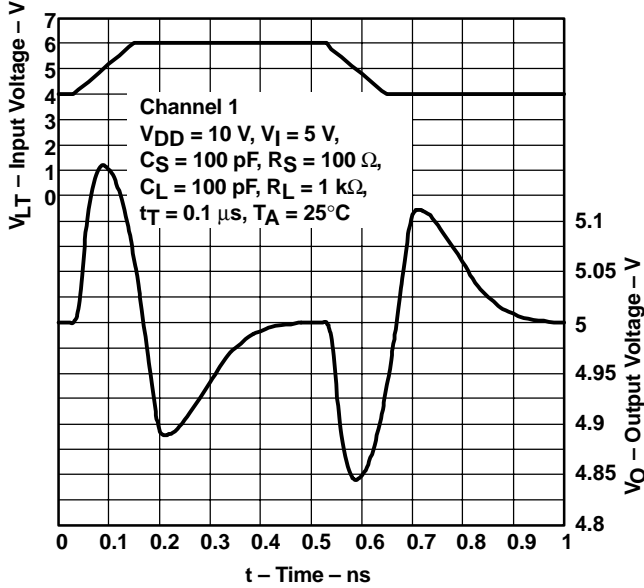


Figure 40

TRANSIENT LOAD REGULATION – SINKING

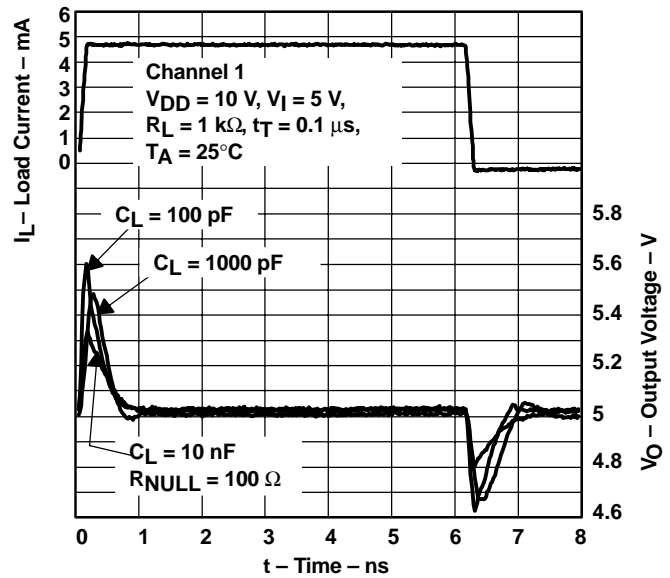


Figure 41

TRANSIENT LOAD REGULATION – SOURCING

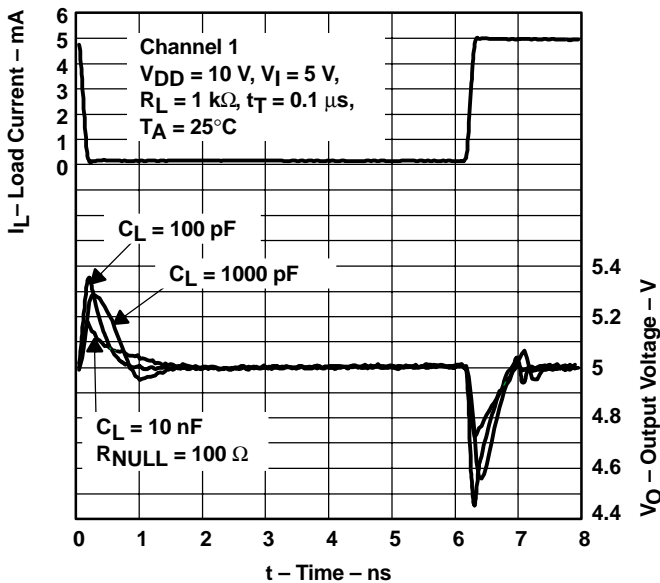


Figure 42

TRANSIENT LOAD REGULATION – V_{COM} BUFFER

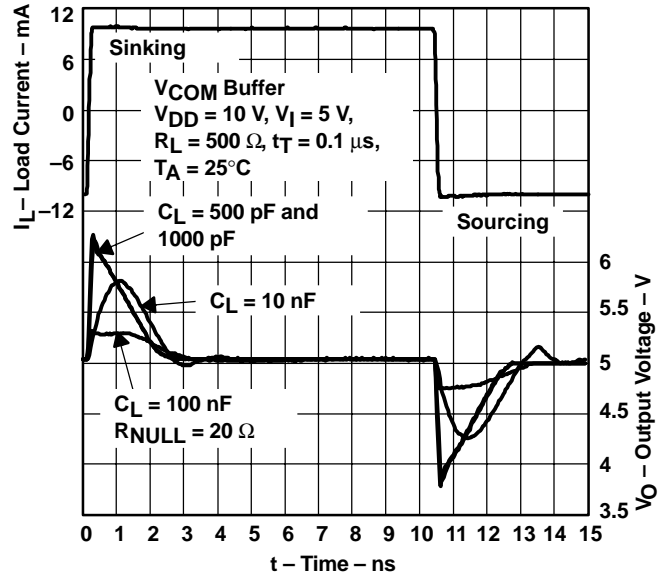


Figure 43

APPLICATION INFORMATION

The requirements on the number of gamma correction channels vary greatly from panel to panel. Therefore, the BUFxx702 series of gamma correction buffers offers different channel combinations. The BUF11702 offers 10 gamma channels plus one V_{COM} channel, whereas, the BUF07702 provides six gamma channels plus one V_{COM} . The V_{COM} channel can be used to drive the V_{COM} node on the LCD panel.

Gamma correction voltages are often generated using a simple resistor ladder, as shown in Figure 44. The BUFxx702 buffers the various nodes on the gamma correction resistor ladder. The low output impedance of the BUFxx702 forces the external gamma correction voltage on the respective reference node of the LCD source driver. Figure 44 shows an example of the BUFxx702 in a typical block diagram driving an LCD source driver with 10- or 6-channel gamma correction reference inputs.

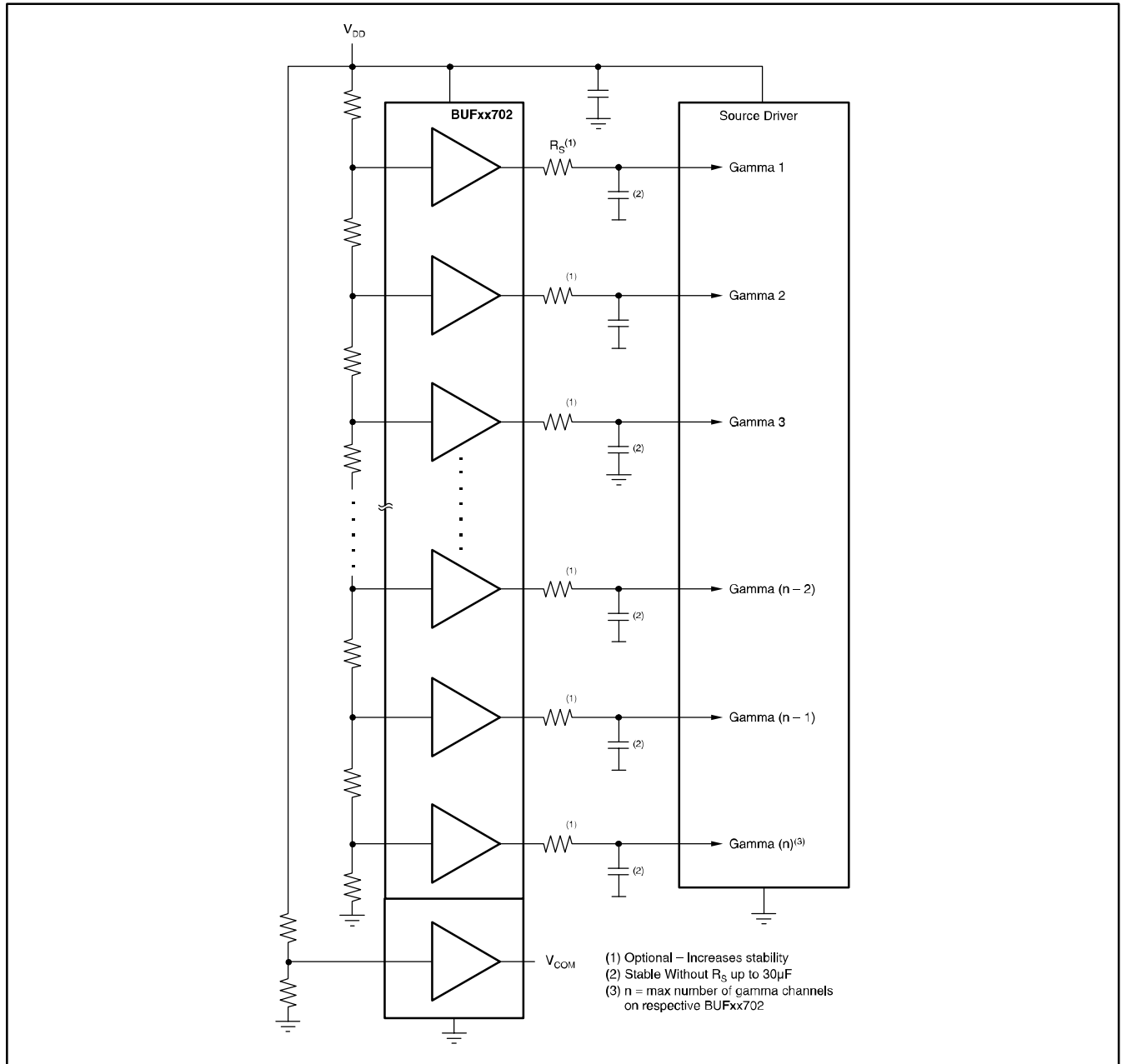


Figure 44. LCD Source Driver Typical Block Diagram.

INPUT VOLTAGE RANGE GAMMA BUFFERS

Figure 45 shows a typical gamma correction curve with 10 gamma correction reference points (GMA1 through GMA10). As can be seen from this curve, the voltage requirements for each buffer varies greatly. The swing capability of the input stages of the various buffers is carefully matched to the application. Using the example of the BUF11702 with 10 gamma correction channels, buffers 1 to 5 have input stages that include V_{DD} , but will only swing within 1V to GND. Buffers 1 through 5 have only a single NMOS input stage. Buffers 6 through 10 have only a single PMOS input stage. The input range of the PMOS input stage includes GND.

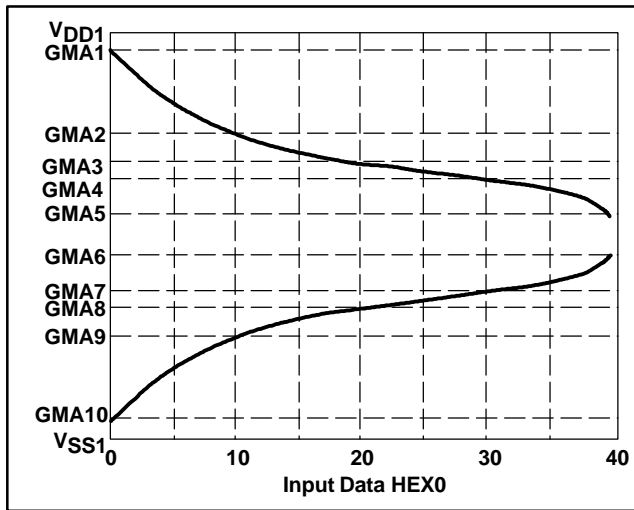


Figure 45. Gamma Correction Curve.

OUTPUT VOLTAGE SWING GAMMA BUFFERS

The output stages have been designed to match the characteristic of the input stage. Once again using the example of the BUF11702 means that the output stage of buffer 1 swings very close to V_{DD} , typically $V_{CC} - 100\text{mV}$ at 5mA; its ability to swing to GND is limited. Buffers 2 through 5 have smaller output stages with slightly larger output resistances, as they will not have to swing as close to the positive rail as buffer 1. Buffers 6 through 10 swing closer to GND than V_{DD} . Buffer 10 is designed to swing very close to GND, typically $\text{GND} + 100\text{mV}$ at a 5mA load current. See the typical characteristics for more details. This approach significantly reduces the silicon area and cost of the whole solution. However, due to this architecture, the correct buffer needs to be connected to the correct gamma correction voltage. Connect buffer 1 to the gamma voltage closest to V_{DD} , and buffers 2 through 5 to the following voltages. Buffer 10 should be connected to the gamma correction voltage closest to GND (or the negative rail), buffers 9 through 6 to the following higher voltages.

COMMON BUFFER (V_{COM})

The common buffer output of the BUF11702 has a greater output drive capability than buffers 1 through 10, to meet the heavier current demands of driving the common node of the LCD panel. It was also designed to drive heavier capacitive loads and still remain stable, as shown in Figure 46.

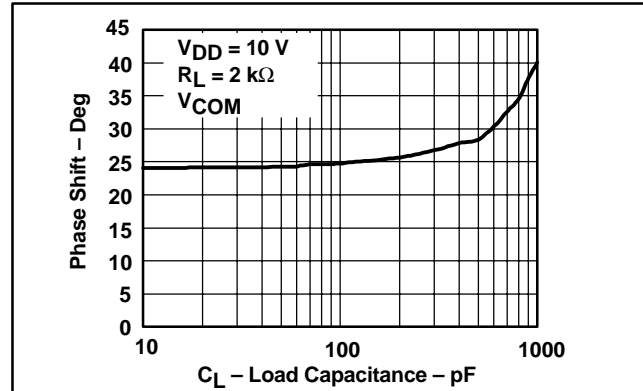


Figure 46. Phase Shift vs Load Capacitance.

CAPACITIVE LOAD DRIVE

The BUF11702 has been designed to be able to sink/source DC currents in excess of 10mA. Its output stage has been designed to deliver output current transients with little disturbance of the output voltage. However, there are times when very fast current pulses are required. Therefore, in LCD source driver buffer applications, it is quite normal for capacitors to be placed at the outputs of the reference buffers. These are to improve the transient load regulation. These will typically vary from 100pF and more. The BUF11702 gamma buffers were designed to drive capacitances in excess of 100pF and retain effective phase margins above 50° , as shown in Figure 47.

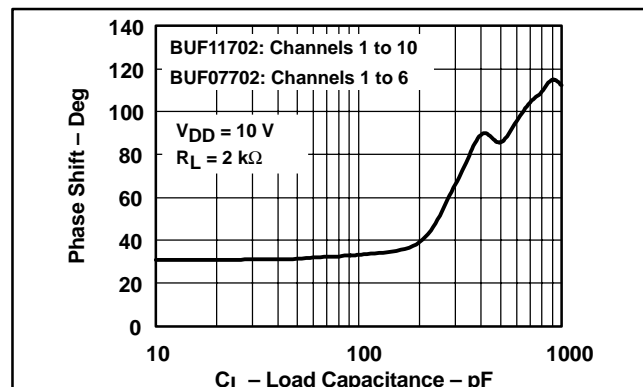


Figure 47. Phase Shift Between Output and Input vs Load Capacitance for the gamma buffers

APPLICATIONS WITH >10 GAMMA CHANNELS

When a greater number of gamma correction channels are required, two or more BUFxx702 devices can be used in parallel, as shown in Figure 48. This provides a cost-effective way of creating more reference voltages over the use of quad-channel op amps or buffers. The suggested configuration in Figure 48 simplifies layout. The various different channel versions provide a high degree of flexibility and also minimize total cost and space.

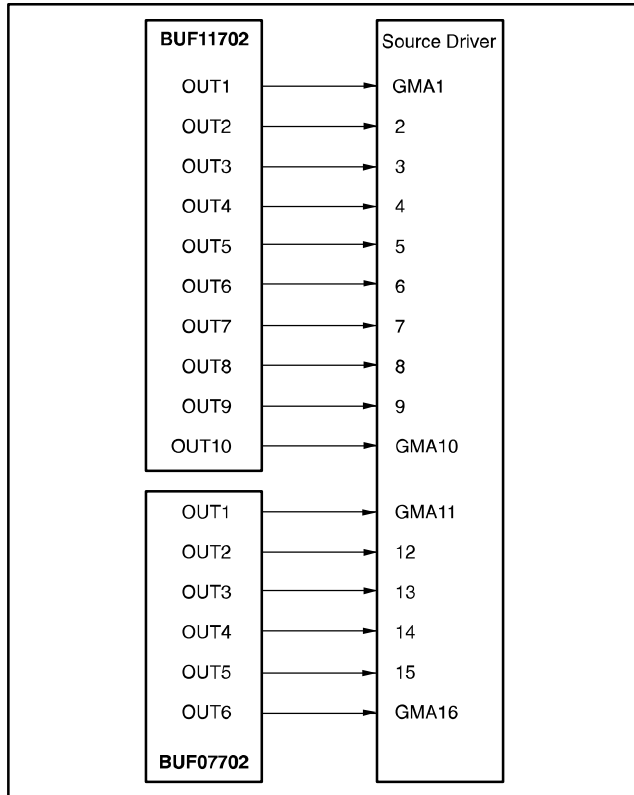


Figure 48. Creating > 10 Gamma Voltage Channels

MULTIPLE V_{COM} CHANNELS

In some LCD panels, more than one V_{COM} driver is required for best panel performance. Figure 49 uses 3 BUF07702s to create a total of 18 gamma-correction and 3 V_{COM} channels. This solution saves considerable space and cost over the more conventional approach of using 5 or 6 quad-channel buffers or op amps.

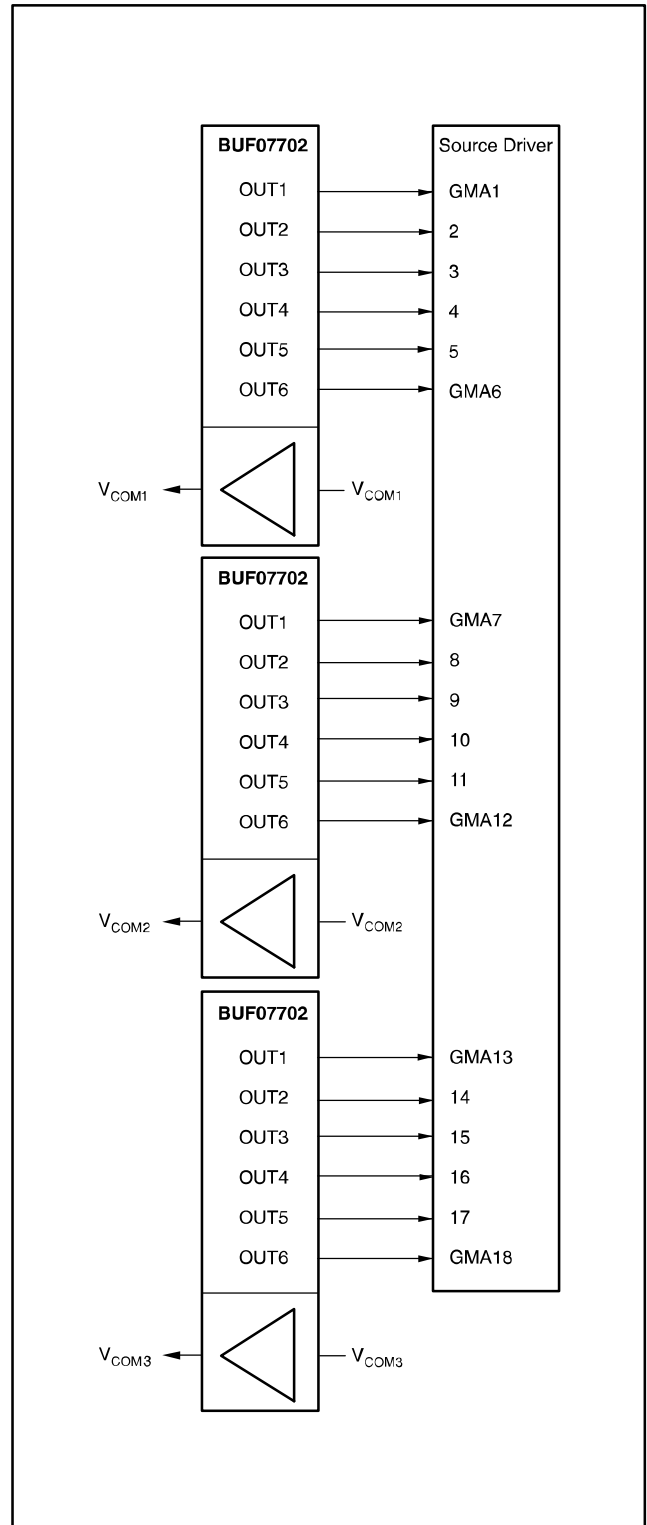


Figure 49. 18-Channel Application with Five Integrated V_{COM} Channels

COMPLETE LCD SOLUTION FROM TI

Besides the BUFxx702 line of gamma correction buffers, TI offers a complete set of ICs for the LCD panel market: source and gate drivers, various power-supply solutions, as well as audio power solutions. Figure 50 shows the Total IC solution from TI.

AUDIO POWER AMPLIFIER FOR TV SPEAKERS

The TPA3002D2 is a 7W (per channel) stereo audio amplifier specifically targeted towards LCD monitors and TVs. It offers highly efficient, filter-free Class-D operation for driving bridged tied stereo speakers. The TPA3002D2 is designed to drive stereo speakers as low as 8Ω without an output filter. The high efficiency of the TPA3002D2 eliminates the need for external heatsinks when playing music. Stereo speaker volume is controlled with a DC voltage applied to the volume control terminal offering a range of gain from -40dB to +36dB. Line outputs, for driving external headphone amplifier inputs, are also DC voltage controlled with a range of gain from -56dB to +20dB. An integrated +5V regulated supply is provided for powering an external headphone amplifier. The TPA3002D2 is scheduled to release to market in Q4, 2002. Texas Instruments offers

a full line of linear and switch-mode audio power amplifiers. For more information visit www.ti.com. For excellent audio performance TI recommends the OPA364 or OPA353 as headphone drivers.

GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF11702 is available in the thermally enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted; see Figures 51(a) and (b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 51(c). Due to this thermal pad having direct thermal contact with the die, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

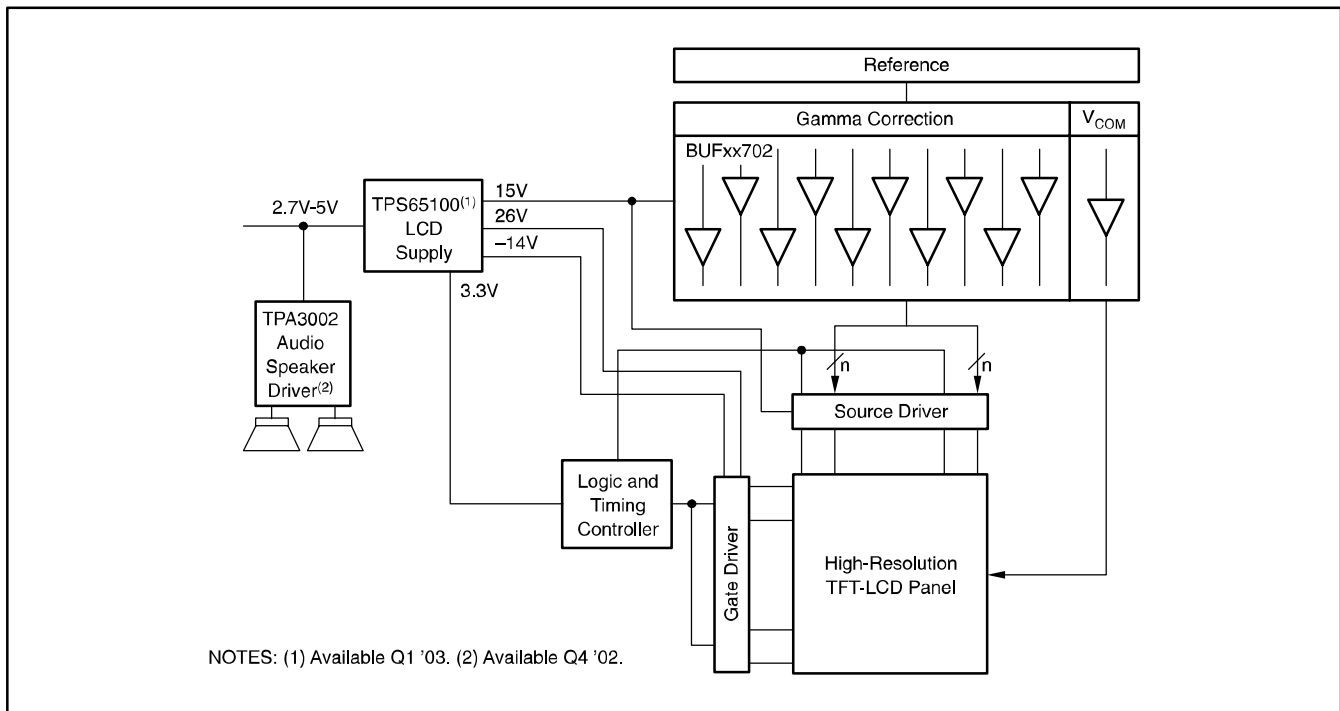


Figure 50. TI LCD Solution

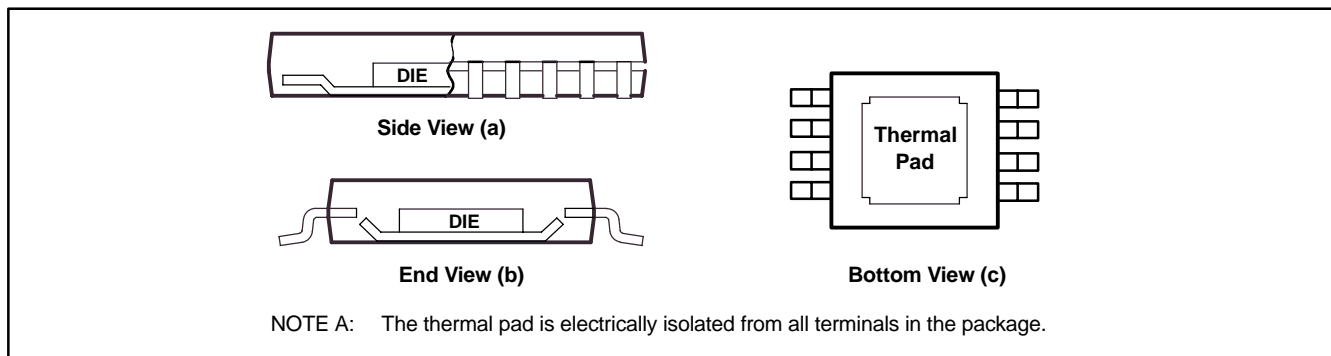


Figure 51. Views of Thermally Enhanced DGN Package

1. Prepare the PCB with a top-side etch pattern, (see Pin Configurations). There should be etching for the leads as well as etch for the thermal pad.
2. Place 18 holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUFxx702 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUFxx702 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUFxx702 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA} , the maximum power dissipation is shown in Figure 52, and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = maximum power dissipation (W)

T_{MAX} = absolute maximum junction temperature (150°C)

T_A = free-ambient air temperature (°C)

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = thermal coefficient from junction to case (°C/W)

θ_{CA} = thermal coefficient from case-to-ambient air (°C/W)

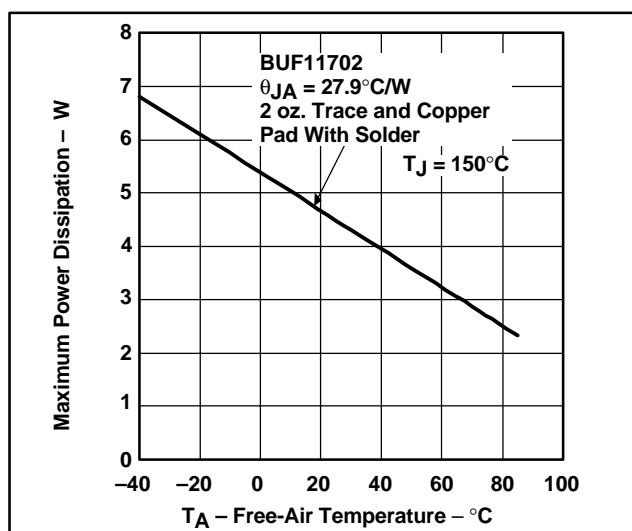


Figure 52. Maximum Power Dissipation vs Free-Air Temperature

This lower thermal resistance enables the BUFxx702 to deliver maximum output currents even at high ambient temperatures.

APPLICATION INFORMATION

BUF11702 Evaluation Module (SLOP356)

The BUF11702 has an evaluation module that can be mounted along with reference resistors and load capacitors. This enables the BUF11702 to be used in its own daughterboard in existing designs for easy evaluation. The schematic of the BUF11702 EVM is shown in Figure 53. Note that the EVM has been

configured for single supply use. As such, all decoupling capacitors are connected to the ground plane of the EVM, as are the ground terminals of the BUF11702.

In populated versions of the EVM, capacitors C₁ to C₄ have been included. Capacitors C₁ and C₂ are bulk decoupling capacitors of 6.8μF while capacitors C₃ and C₄ are 100nF ceramic high-frequency decoupling capacitors. Resistors R₁ to R₃₂ and capacitors C₅ to C₁₆ have not been included and are application specific.

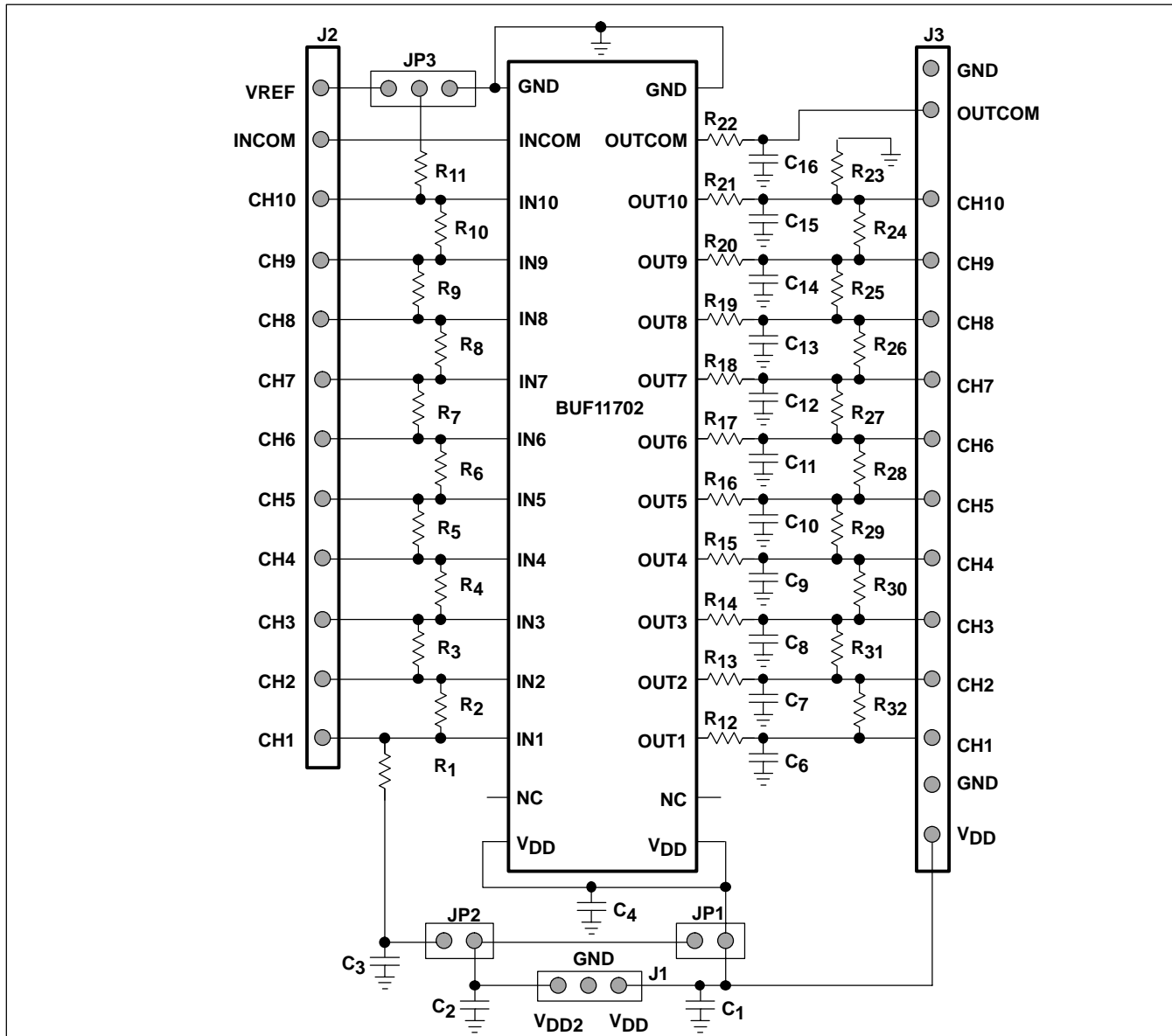


Figure 53. BUF11702 Evaluation Module Schematic

REFERENCE VOLTAGES

The reference voltages can be supplied externally via the connector J2 (not included) or generated onboard via resistors R₁ to R₁₁. Provision on the board for an external low side reference has been included so that the negative references can be referred to a voltage other than ground.

The reference ladder can be referred to either V_{DD} (master supply voltage) or a secondary voltage, V_{DD2}. This allows a low noise or absolute reference voltage to be used for the LCD source driver's DACs other than the system voltage. If the secondary voltage is used, then jumper JP1 should be left open and jumper JP2 shorted. If a ratiometric reference (proportional to the master supply voltage) is to be used, then jumper JP1 and JP2 should be shorted, feeding V_{DD} through to the reference ladder.

OUTPUT

The outputs of the BUF11702 are fed to connector J3 (not mounted). This enables the output voltages to be monitored directly on the EVM or fed off-board for evaluation in a real system.

Onboard load resistors, R₂₃ to R₃₂, connected to ground can also be mounted. These can be used to simulate resistive loading of the LCD source driver.

Transient improving capacitors are frequently used in LCD panel applications, and so pads to mount these transient improving capacitors, C₆ to C₁₆, have been included. Due to the possible magnitude of these capacitors, pads have been placed between the output of the BUF11702 and these capacitors to mount nulling resistors, R₁₂ to R₂₂. If the nulling resistors are not required, shorts could be placed instead of resistors.

The pads for R₁ to R₃₂ and capacitors C₃ to C₁₆ have been laid out to support 0805 or 1206 size components.

POWERPAD

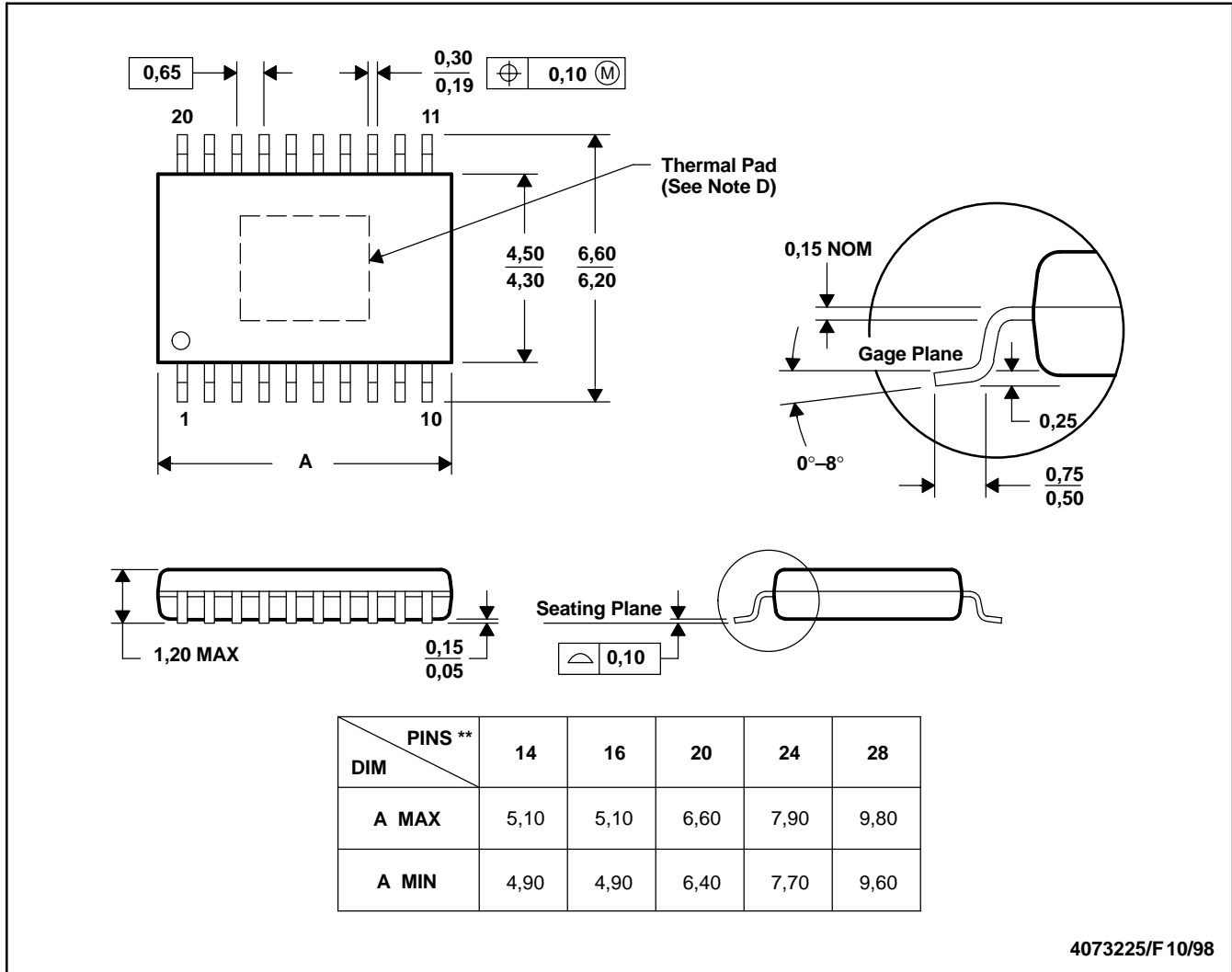
The EVM has been laid out to support the PowerPAD feature of the BUF11702. An area is provided on the EVM, under the BUF11702, for the exposed leadframe to be connected to. Eighteen vias are connected to the ground plane of the EVM to reduce the thermal case to ambient resistance, θ_{CA} , significantly. See applications section on general PowerPAD design considerations.

MECHANICAL DATA

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE

20 PINS SHOWN



4073225/F 10/98

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions.
 - D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 - E. Falls within JEDEC MO-153

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