

CD4007UB Types

CMOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

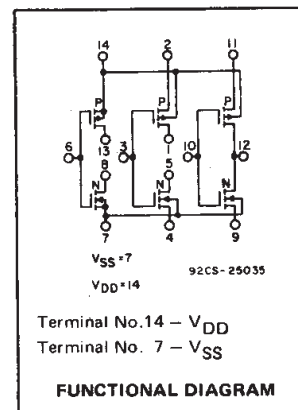
■ CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Standardized symmetrical output characteristics
- Medium Speed Operation – t_{PHL} , t_{PLH} = 30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C



RECOMMENDED OPERATING CONDITIONS

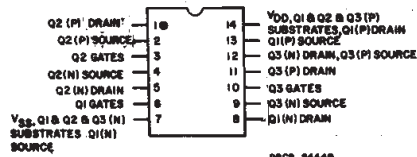
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

Applications:

- Extremely high-input impedance amplifiers
- Shapers
- Inverters
- Threshold detector
- Linear amplifiers
- Crystal oscillators

TERMINAL DIAGRAM
Top View



STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25								
				−55	−40	+85	+125	Min.	Typ.	Max.		
Quiescent Device Current, I _{DD} Max.	—	0,5	5	0.25	0.25	7.5	7.5	—	0.01	0.25	μA	
	—	0,10	10	0.5	0.5	15	15	—	0.01	0.5		
	—	0,15	15	1	1	30	30	—	0.01	1		
	—	0,20	20	5	5	150	150	—	0.02	5		
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—		
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	mA	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—		
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—		
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—		
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V	
	—	0,10	10	0.05				—	0	0.05		
	—	0,15	15	0.05				—	0	0.05		
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V	
	—	0,10	10	9.95				9.95	10	—		
	—	0,15	15	14.95				14.95	15	—		
Input Low Voltage, V _{IL} Max.	4.5	—	5	1				—	—	1	V	
	9	—	10	2				—	—	2		
	13.5	—	15	2.5				—	—	2.5		
Input High Voltage, V _{IH} Min.	0.5	—	5	4				4	—	—	V	
	1	—	10	8				8	—	—		
	1.5	—	15	12.5				12.5	—	—		
Input Current I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10 ^{−5}	±0.1	μA	

CD4007UB Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

..... -0.5V to $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT

..... $\pm 10mA$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ C$ to $+100^\circ C$ 500mW

For $T_A = +100^\circ C$ to $+125^\circ C$ Derate Linearly at 12mW/ $^\circ C$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A)

..... $-55^\circ C$ to $+125^\circ C$

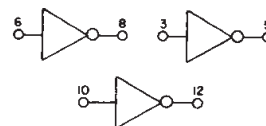
STORAGE TEMPERATURE RANGE (T_{stg})

..... $-65^\circ C$ to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max $+265^\circ C$

a) Triple Inverters



(14,2,11); (8,13);
(1,5); (7,4,9)

92CS-15350

b) 3-Input NOR Gate



(13,2); (1,11);
(12,5,8); (7,4,9)

92CS-15349

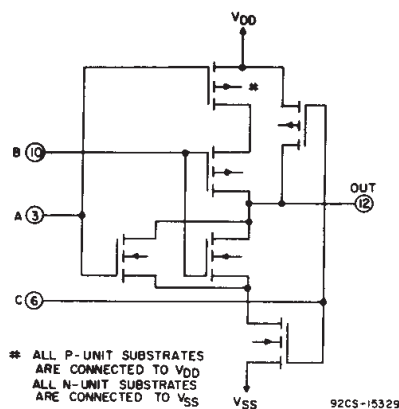
c) 3-Input NAND Gate



(1,12,13); (2,14,11);
(4,8); (5,9)

92CS-15348

d) Tree (Relay) Logic



92CS-15329

(13,12,5); (4,9,8);
(14,2); (1,11)

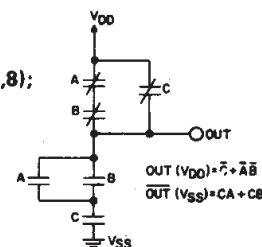


Fig. 2 — Sample CMOS logic circuit arrangements using type CD4007UB.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$; Input $t_r, t_f = 20$ ns,
 $C_L = 50$ pF, $R_L = 200$ K Ω

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS
		V_{DD} Volts	Typ.	Max.
Propagation Delay Time: t_{PHL} , t_{PLH}		5	55	110
		10	30	60
		15	25	50
Transition Time t_{THL} , t_{TLH}		5	100	200
		10	50	100
		15	40	80
Input Capacitance	C_{IN}	Any Input	10	15
				pF

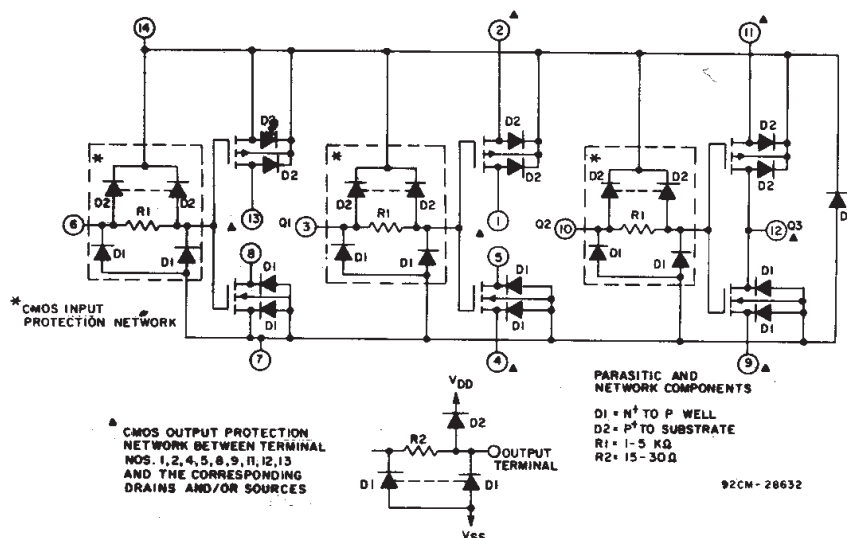
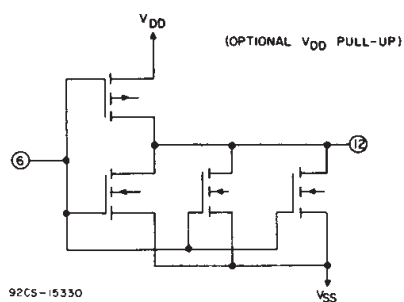


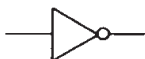
Fig. 1 — Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

CD4007UB Types

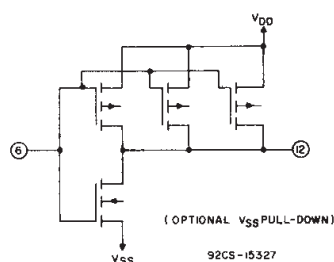
e) High Sink-Current Driver



(6,3,10); (8,5,12);
(11,14); (7,4,9)



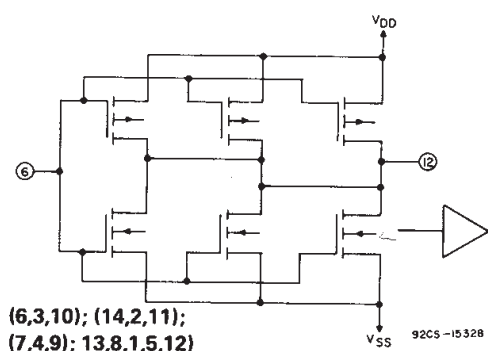
f) High Source-Current Driver



(6,3,10); (13,1,12);
(14,2,11); (7,9)

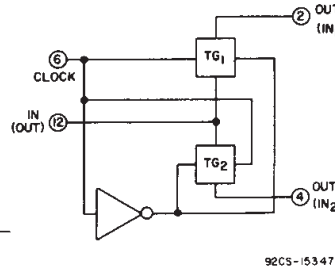


g) High Sink - and Source-Current Driver



(6,3,10); (14,2,11);
(7,4,9); (13,8,1,5,12)

h) Dual Bi-Directional Transmission Gating



(1,5,12); (2,9);
(11,4); (8,13,10);
(6,3)

Fig. 2 - Sample CMOS logic circuit arrangements using type CD4007UB (Cont'd).

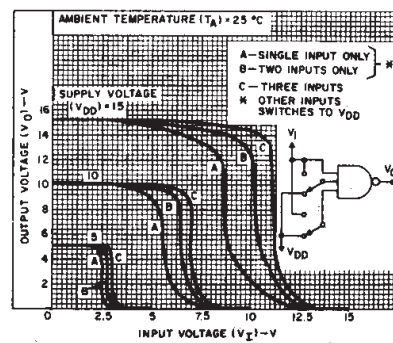


Fig. 3 - Typical voltage-transfer characteristics for NAND gate.

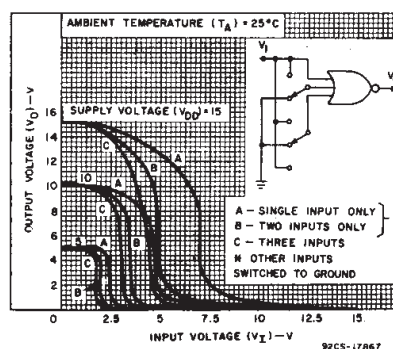


Fig. 4 - Typical voltage-transfer characteristics for NOR gate.

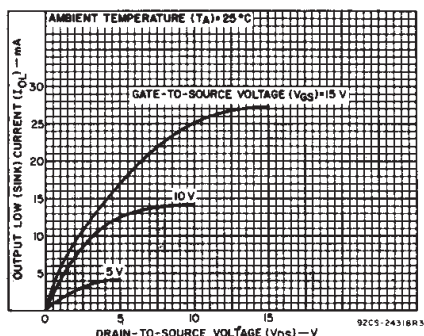


Fig. 5 - Typical output low (sink) current characteristics.

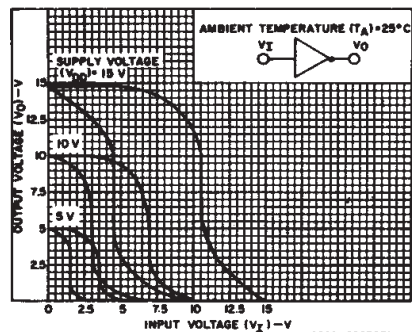


Fig. 6 - Minimum and maximum voltage-transfer characteristics for inverter.

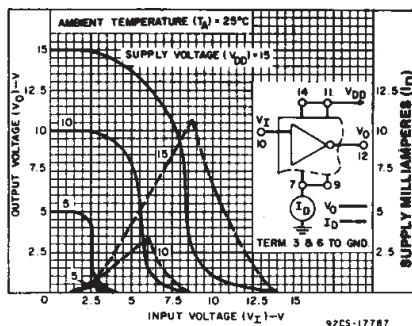


Fig. 7 - Typical current and voltage-transfer characteristics for inverter.

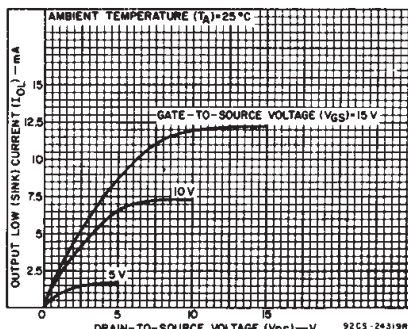


Fig. 8 - Minimum output low (sink) current characteristics.

CD4007UB Types

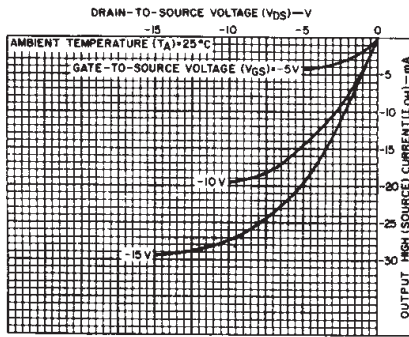


Fig. 9 - Typical output high (source) current characteristics.

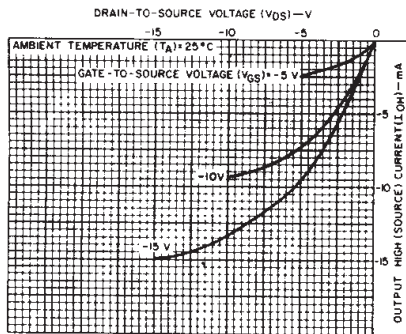


Fig. 10 - Minimum output high (source) current characteristics.

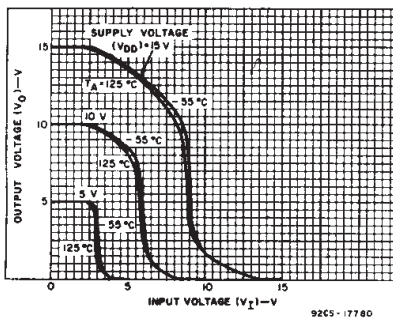


Fig. 11 - Typical voltage-transfer characteristics as a function of temperature.

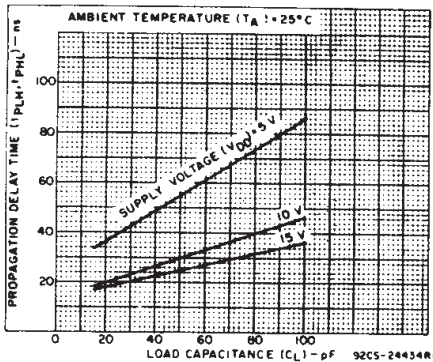


Fig. 12 - Typical propagation delay time vs. load capacitance.

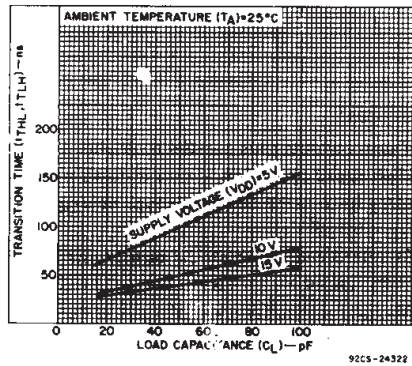


Fig. 13 - Typical transition time vs. load capacitance.

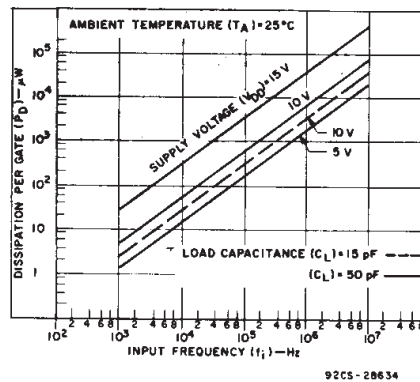


Fig. 14 - Typical dissipation vs. frequency characteristics.

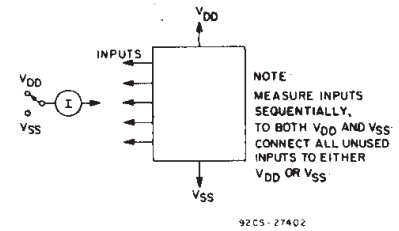


Fig. 15 - Input current test circuit.

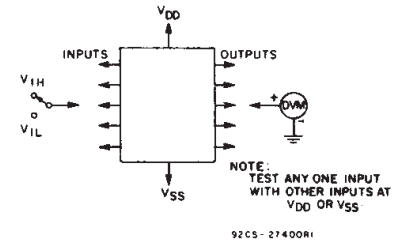


Fig. 16 - Input voltage test circuit.

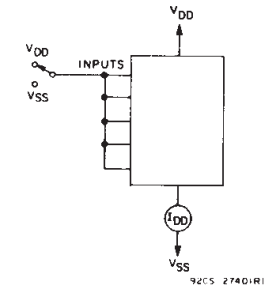
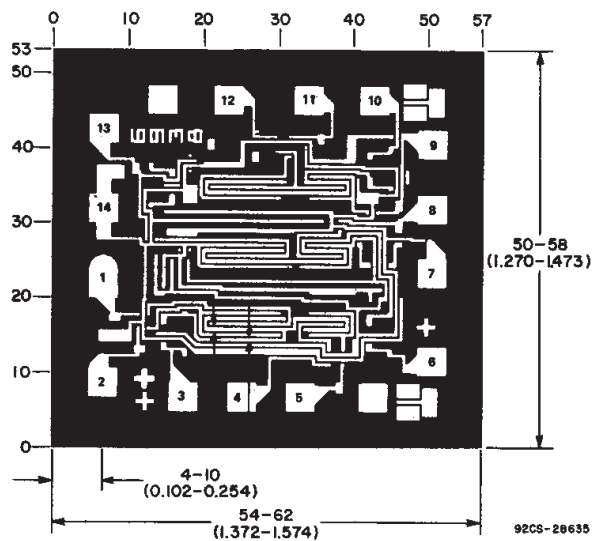


Fig. 17 - Quiescent device current test circuit.



DIMENSIONS AND PAD LAYOUT FOR CD4007UBH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4007UBE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD4007UBF	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4007UBF3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD4007UBF3A116	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
CD4007UBM	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4007UBM96	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4007UBMT	ACTIVE	SOIC	D	14	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4007UBNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD4007UBPW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD4007UBPWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

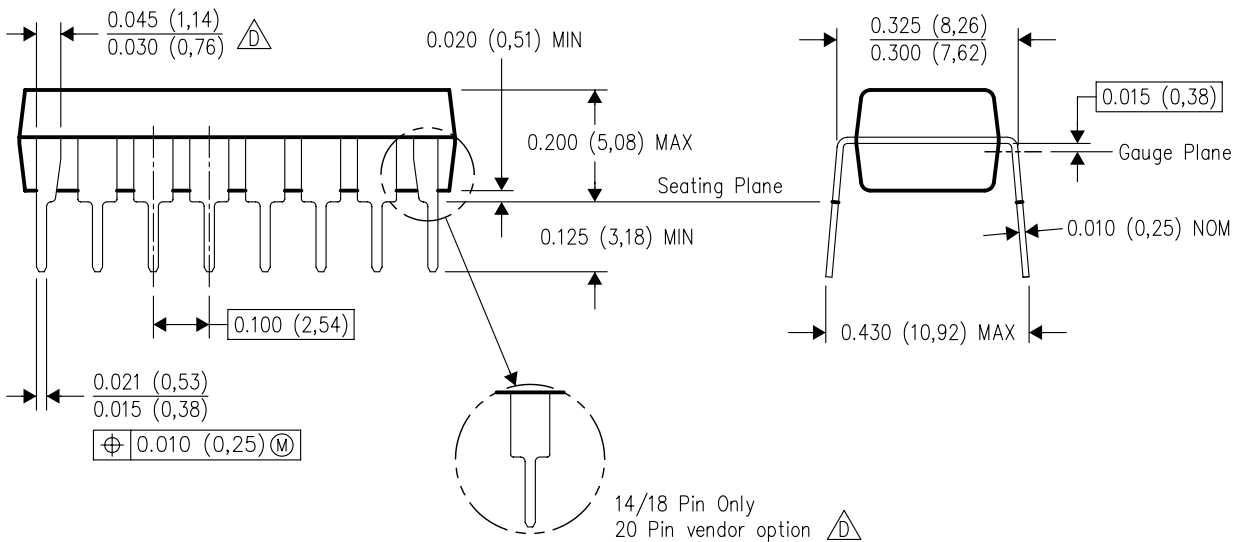
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

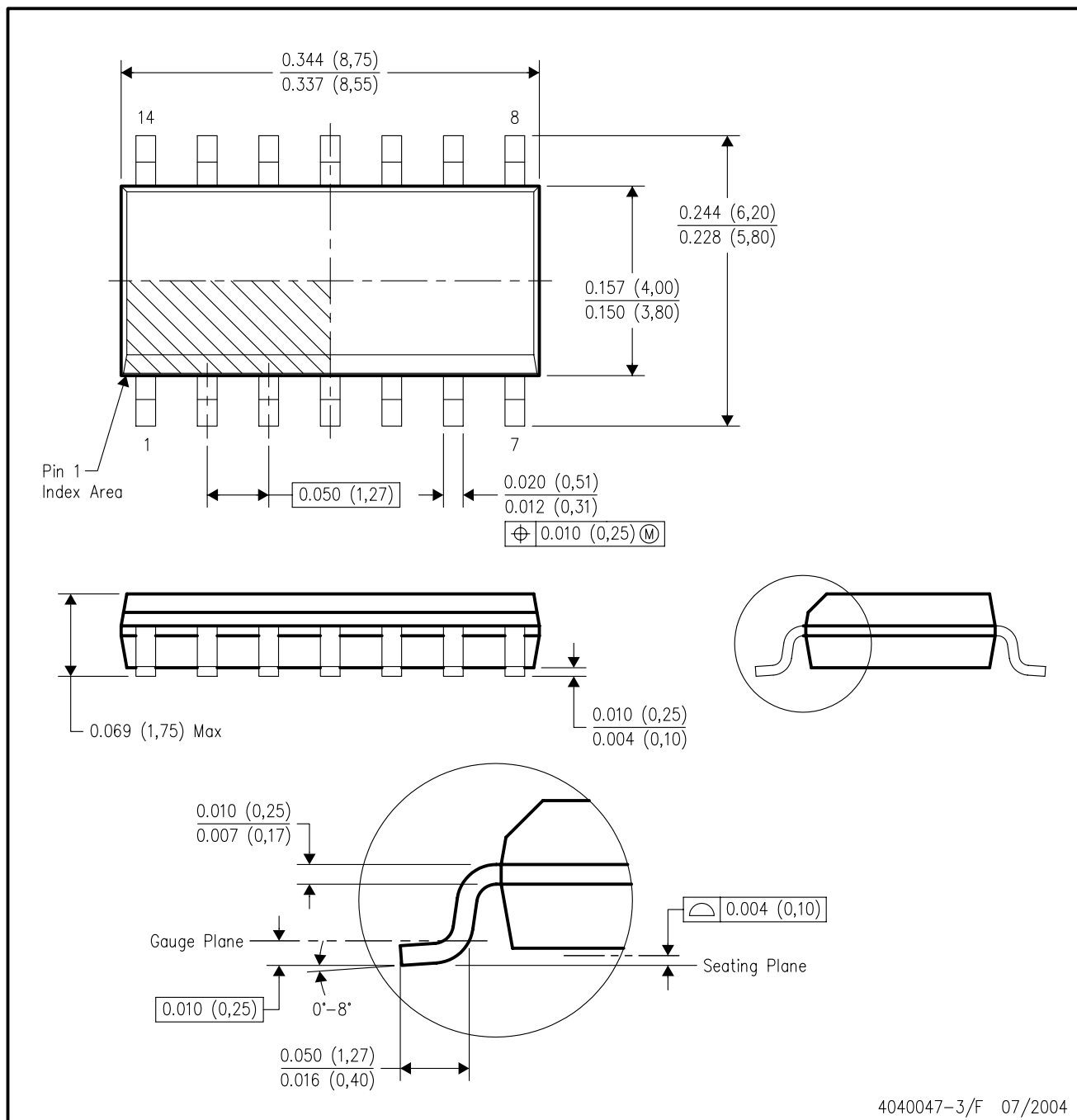


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



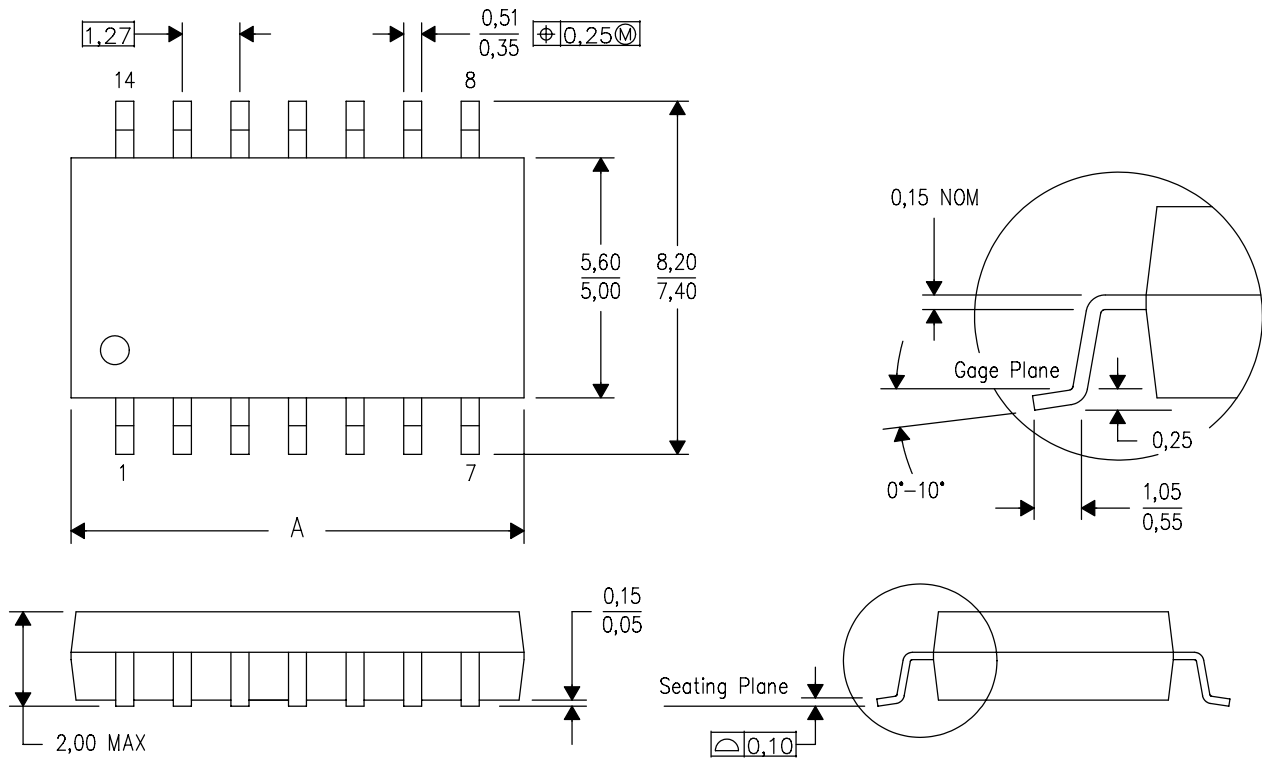
4040047-3/F 07/2004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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