

## CMOS Decade Up-Down Counter/Latch/Display Driver

High-Voltage Type (20-V Rating)



92CS-31380

**Features:**

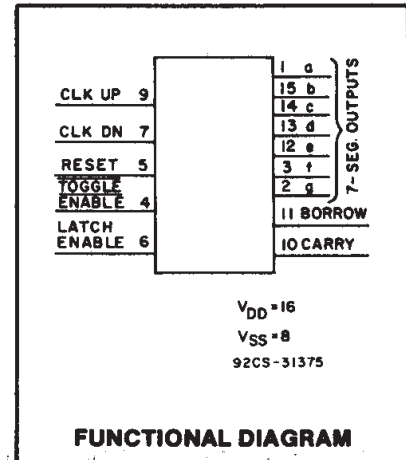
- Separate clock-up and clock-down lines-
- Capable of driving common cathode LEDs and other displays directly
- Allows cascading without any external circuitry
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25° C

■ CD40110B is a dual-clocked up/down counter with a special preconditioning circuit that allows the counter to be clocked, via positive going inputs, up or down regardless of the state or timing (within 100 ns typ.) of the other clock line.

The clock signal is fed into the control logic and Johnson counter after it is preconditioned. The outputs of the Johnson counter (which include anti-lock gating to avoid being locked at an illegal state) are fed into a latch. This data can be fed directly to the decoder through the latch or can be strobed to hold a particular count while the Johnson counter continues to be clocked. The decoder feeds a seven-segment bipolar output driver which can source up to 25 mA to drive LEDs and other displays such as low-voltage fluorescent and incandescent lamps.

A short duration negative-going pulse appears on the BORROW output when the count changes from 0 to 9 or the CARRY output when the count changes from 9 to 0. At the other times the BORROW and CARRY outputs are a logic 1.

The CARRY and BORROW outputs can be tied directly to the clock-up and clock-down lines respectively of another CD40110B for easy cascading of several counters.



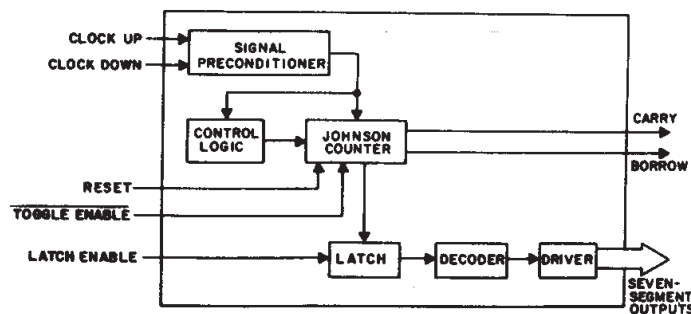
**FUNCTIONAL DIAGRAM**

- Noise margin (full package-temperature range) =
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- 5 V, 10 V and 15 V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices".

**Applications:**

- Rate comparators
- General counting applications where display is desired
- Up-down counting applications where input pulses are random in nature

The CD40110B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), and 16-lead dual-in-line plastic package (E suffix), and also available in chip form, (H suffix).



92CS-29200RI

Fig. 1 - Functional diagram.

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

## CD40110B Types

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )	-0.5V to +20V
Voltages referenced to V <sub>SS</sub> Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V <sub>DD</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ):	
For T <sub>A</sub> = -55°C to +100°C	500mW
For T <sub>A</sub> = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V <sub>DD</sub> V	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package Temperature Range)	—	3	18	V
Clock Input Frequency (Sum of CL <sub>UP</sub> & CL <sub>DN</sub> Freqs.)  f <sub>CL</sub>	5	—	1	MHz
	10	—	3	
	15	—	5	
Clock Pulse Width  t <sub>w</sub>	5	110	—	ns
	10	40	—	
	15	30	—	
Latch Enable Pulse Width	5	110	—	ns
	10	30	—	
	15	24	—	
Reset Removal-Time	5	550	—	ns
	10	200	—	
	15	130	—	
Reset Pulse Width	5	350	—	ns
	10	170	—	
	15	120	—	

## CD40110B Types

### STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				LIMITS AT INDICATED TEMPERATURES (°C)							Units
	I <sub>OH</sub> (mA)	V <sub>OH</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
									Min.	Typ.	Max.	
Quiescent Device Current Max. I <sub>DD</sub>	—	—	—	5	5	5	150	150	—	0.04	5	μA
	—	—	—	10	10	10	300	300	—	0.04	10	
	—	—	—	15	20	20	600	600	—	0.04	20	
	—	—	—	20	100	100	3000	3000	—	0.08	100	
Output Voltage Low-Level Max. V <sub>OL</sub>	—	—	0,5	5	0,05				—	0	0,05	V
	—	—	0,10	10	0,05				—	0	0,05	
	—	—	0,15	15	0,05				—	0	0,05	
High-Level Min. V <sub>OH</sub>	—	—	0,5	5	—	—	—	—	—	4,55	—	V
	—	—	0,10	10	—	—	—	—	—	9,55	—	
	—	—	0,15	15	—	—	—	—	—	14,55	—	
Input Low Voltage Max. V <sub>IL</sub>	—	0,5, 3,8	—	5	1,5				—	—	1,5	V
	—	1, 8,8	—	10	3				—	—	3	
	—	1,5, 13,8	—	15	4				—	—	4	
Input High Voltage Min. V <sub>IH</sub>	—	0,5, 3,8	—	5	3,8				3,5	—	—	V
	—	1, 8,8	—	10	7				7	—	—	
	—	1,5, 13,8	—	15	11				11	—	—	
7-Segment Outputs Output Drive Voltage, High Min. V <sub>OH</sub>	■	—	—	5	3,9		4		3,9	4,5	—	V
	-5	—	—		3,65		3,7		3,7	4,3	—	
	-10	—	—		3,55		3,65		3,65	4,25	—	
	-15	—	—		3,5		3,5		3,6	4,15	—	
	-20	—	—		3,45		3,35		3,45	4	—	
	■	—	—	10	8,75		8,85		8,75	9,5	—	
	-5	—	—		8,45		8,55		8,55	9,3	—	
	-10	—	—		8,42		8,5		8,5	9,25	—	
	-15	—	—		8,4		8,47		8,47	9,2	—	
	-20	—	—		8,4		8,40		8,45	9,1	—	
	■	—	—	15	13,8		13,9		13,8	14,5	—	
	-5	—	—		13,65		13,75		13,75	14,35	—	
	-10	—	—		13,6		13,72		13,72	14,3	—	
	-15	—	—		13,6		13,7		13,7	14,2	—	
	-20	—	—		13,6		13,6		13,65	14,1	—	
■	—	—	15	13,3		13,25		13,3	14,0	—		
-5	—	—		13,3		13,25		13,3	14,0	—		
-10	—	—		13,3		13,25		13,3	14,0	—		
-15	—	—		13,3		13,25		13,3	14,0	—		
-20	—	—		13,3		13,25		13,3	14,0	—		
7-Segment Outputs Output Low (Sink) Current Min. I <sub>OL</sub>	—	0,4	0,5	5	1,28	1,22	0,84	0,72	1	2	—	mA
	—	0,5	0,10	10	3,2	3	2,2	1,8	2,6	5,2	—	
	—	1,5	0,15	15	8,4	8	5,6	4,8	6,8	13,6	—	
Carry Outputs Output Low (Sink) Current Min. I <sub>OL</sub>	—	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	mA
	—	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—	
	—	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—	
Output High (Source) Current Min. I <sub>OH</sub>	—	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	mA
	—	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—	
	—	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—	
	—	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—	
Input Current Max. I <sub>IN</sub>	—	0,18	0,18	18	±0,1	±0,1	±1	±1	—	±10 <sup>-5</sup>	±0,1	μA

■ 0(10 μA)

**3**  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD40110B Types

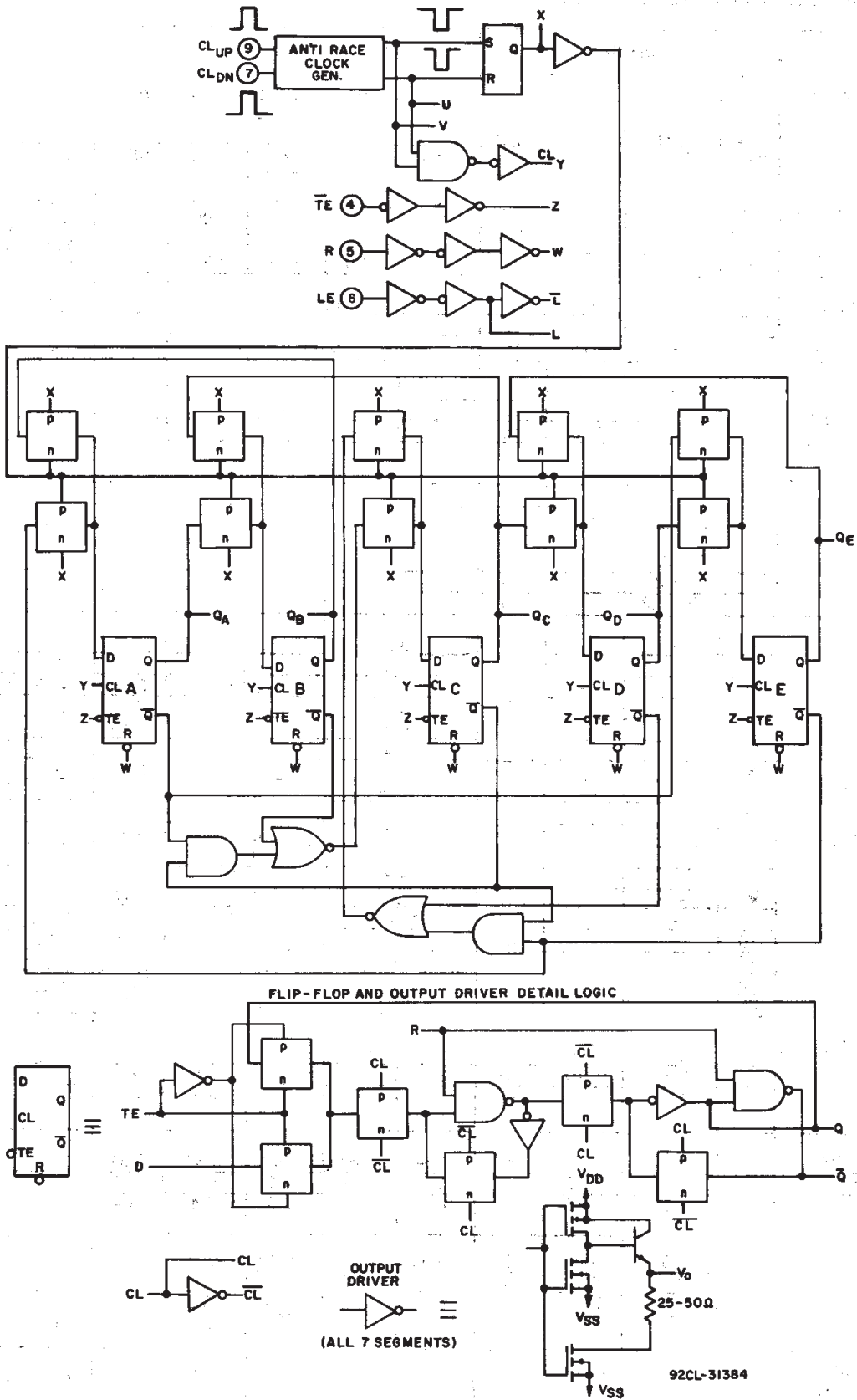
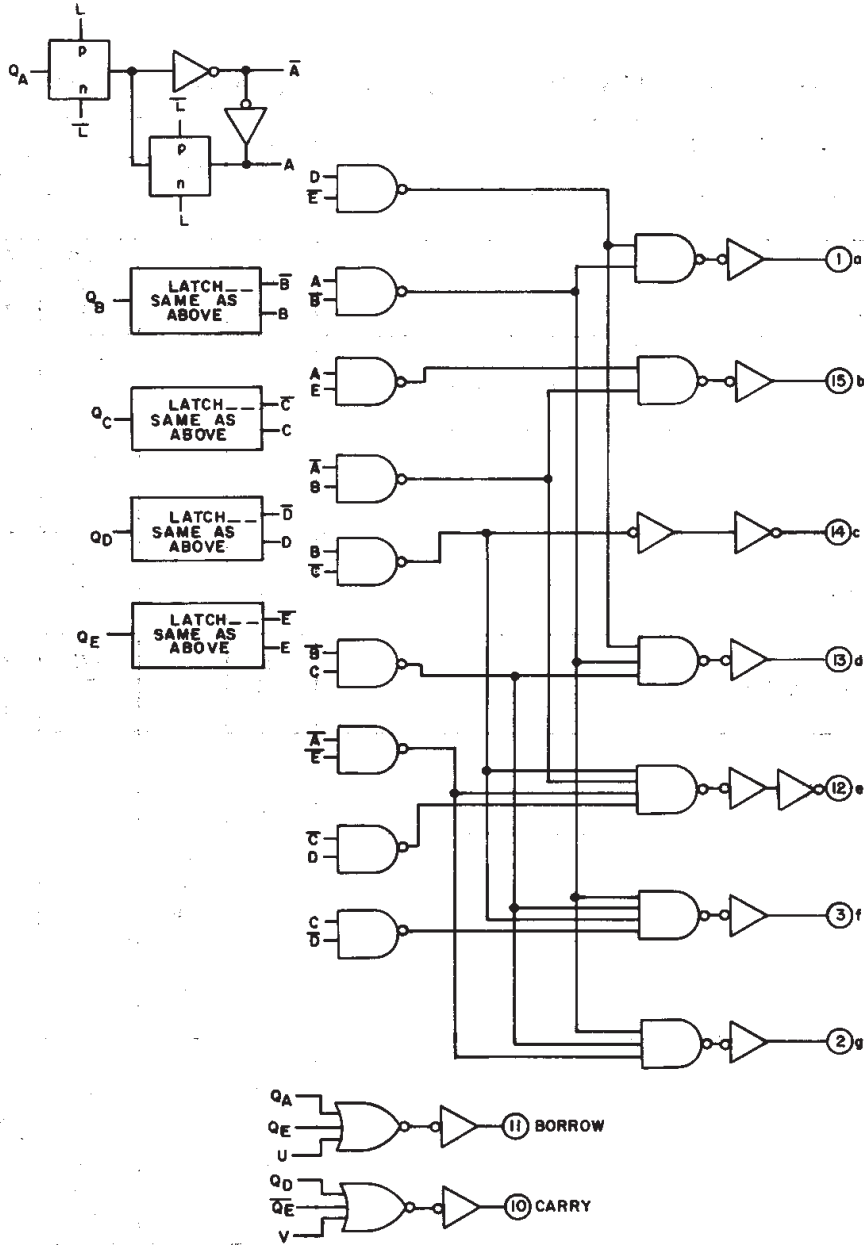


Fig. 2 - Logic diagram with flip-flop and output-driver details. (cont'd on page 5)

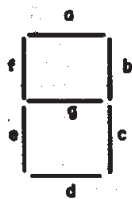
# CD40110B Types



92CL-31384

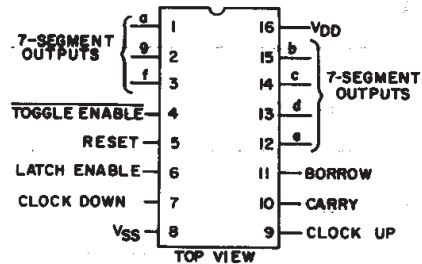
Fig. 2 - Logic diagram with flip-flop and output-driver details.

## DISPLAY SEGMENTS



92CS-31376

## TERMINAL ASSIGNMENT



92CS-31377

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

## CD40110B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$**

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
<b>Clock Up/Clock Down</b>					
Propagation Delay Time: Clock to Carry or Borrow <span style="float: right;"><math>t_{PLH}, t_{PHL}</math></span>	5	—	300	600	ns
	10	—	100	200	
	15	—	70	140	
Clock to Segment <span style="float: right;"><math>t_{PLH}, t_{PHL}</math></span>	5	—	925	1850	
	10	—	360	720	
	15	—	250	500	
Minimum Clock Pulse Width	5	—	55	110	
	10	—	20	40	
	15	—	15	30	
Maximum Clock Input Frequency (Sum of $CL_{UP}$ & $CL_{DN}$ ) <span style="float: right;"><math>f_{CL}</math></span>	5	1	2.5	—	MHz
	10	3	6	—	
	15	5	8.5	—	
Minimum Toggle Enable Pulse Width	5	—	175	350	ns
	10	—	75	150	
	15	—	55	110	
Minimum Latch Enable Pulse Width	5	—	55	110	
	10	—	15	30	
	15	—	12	24	
Output Pulse Width: Carry	5	115	230	—	
	10	60	120	—	
	15	40	75	—	
Borrow	5	140	275	—	
	10	65	130	—	
	15	45	85	—	
Transition Time: Carry or Borrow <span style="float: right;"><math>t_{TLH}, t_{THL}</math></span>	5	—	85	170	
	10	—	45	90	
	15	—	30	60	
Minimum Delay Time Between $CL_{UP}$ & $CL_{DN}$	5	—	100	—	
	10	—	80	—	
	15	—	60	—	
Maximum Clock Rise or Fall Time <span style="float: right;"><math>t_{rCL}, t_{fCL}</math></span>	5	—	—	15	$\mu\text{s}$
	10	—	—	15	
	15	—	—	15	
<b>Reset</b>					
Propagation Delay Time Reset to Output <span style="float: right;"><math>t_{PLH}, t_{PHL}</math></span>	5	—	650	1300	ns
	10	—	350	700	
	15	—	160	320	
Minimum Reset Removal Time	5	—	-275	0	
	10	—	-100	0	
	15	—	-65	0	
Minimum Reset Pulse Width	5	—	175	350	
	10	—	85	170	
	15	—	60	120	

# CD40110B Types

## TRUTH TABLE

CLOCK UP*	CLOCK DOWN*	LATCH ENABLE	TOGGLE ENABLE	RESET	COUNTER	DISPLAY
	X	0	0	0	Increments by 1	Follows Counter
X		0	0	0	Decrements by 1	Follows Counter
		X	X	0	No Change	No Change
X	X	1	X	1	Goes to 00000	Remains Fixed
X	X	0	X	1	Goes to 00000	Follows Counter (Display = 7)
X	X	X	1	0	Inhibited	Remains Fixed
	X	1	0	0	Increments by 1	Remains Fixed
X		1	0	0	Decrements by 1	Remains Fixed

X = Don't Care      1 = High State      0 = Low State

\* Typically 100 ns between clock-up and clock-down positive transitions are required to ensure proper counting.

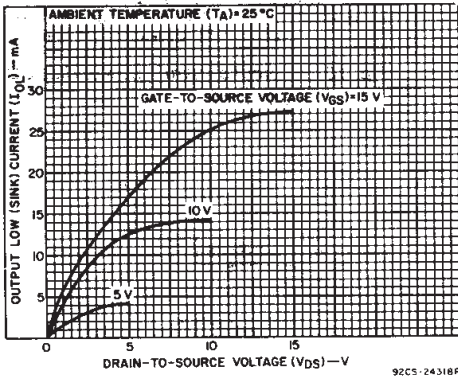


Fig. 3 - Typical carry or borrow output low (sink) current characteristics.

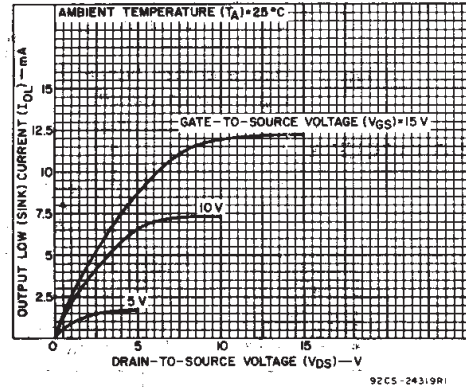


Fig. 4 - Minimum carry or borrow output low (sink) current characteristics.

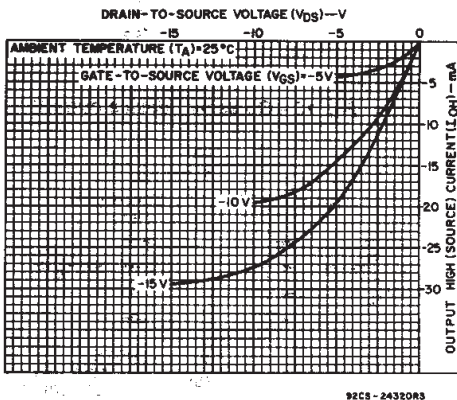


Fig. 5 - Typical carry or borrow output high (source) current characteristics.

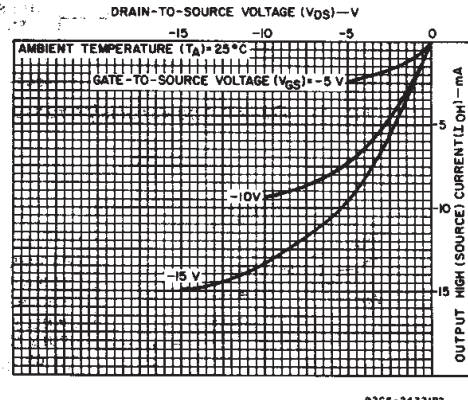


Fig. 6 - Minimum carry or borrow output high (source) current characteristics.

# CD40110B Types

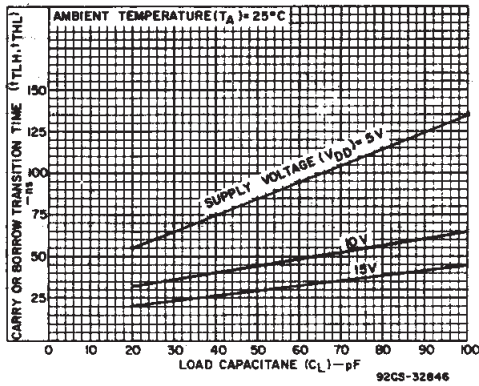


Fig. 7 - Typical carry or borrow transition time vs. load capacitance.

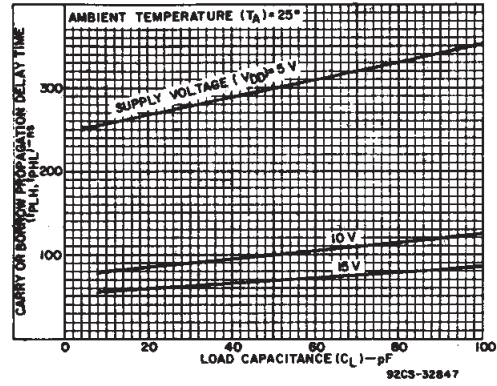


Fig. 8 - Typical carry or borrow propagation delay time vs. load capacitance.

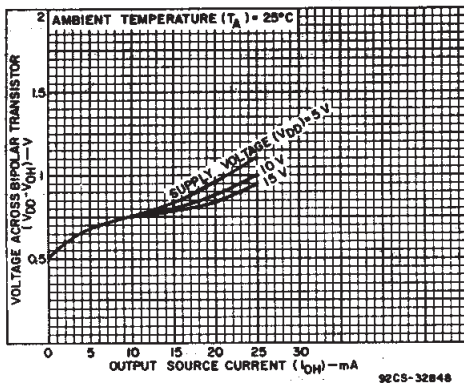


Fig. 9 - Voltage across bipolar transistor vs. output source current.

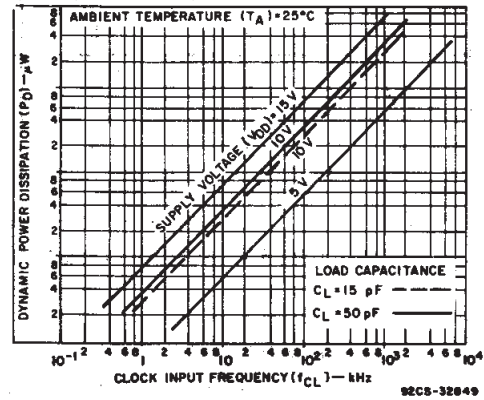


Fig. 10 - Typical dynamic power dissipation vs. frequency.

## TEST CIRCUITS

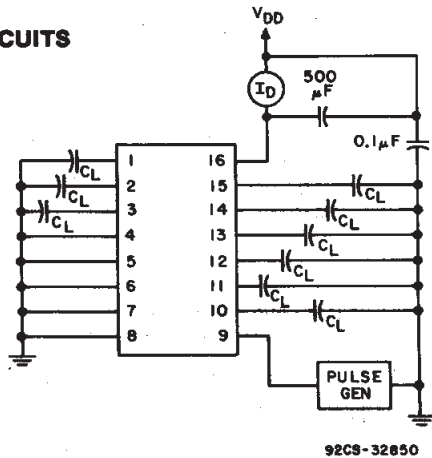


Fig. 11 - Dynamic power dissipation test circuit.

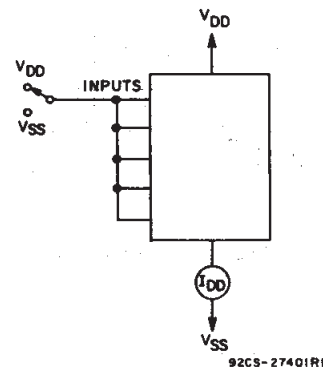


Fig. 12 - Quiescent device current.

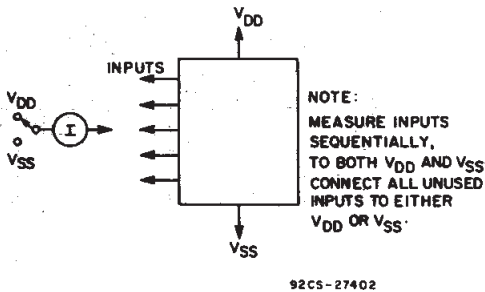


Fig. 13 - Input current.

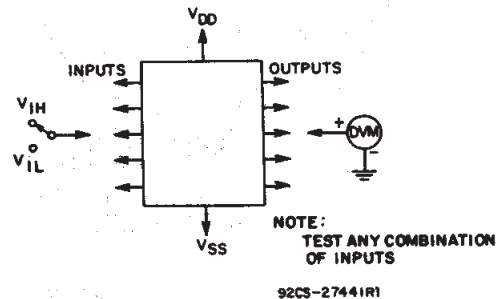


Fig. 14 - Input voltage.



## CD40110B Types

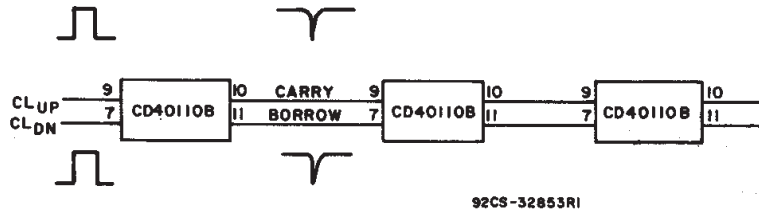
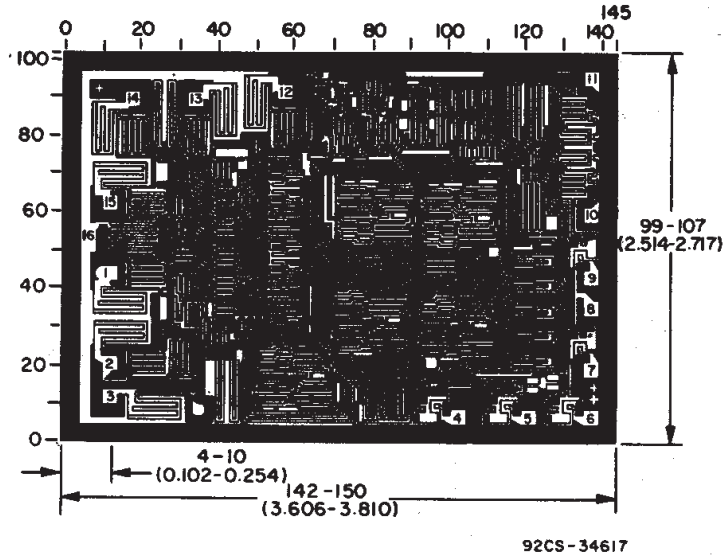


Fig. 15 - Cascading diagram.



Dimensions and pad layout for CD40110B.

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).*

**3**  
**COMMERCIAL CMOS**  
**HIGH VOLTAGE ICs**

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.