

CD4011A, CD4012A, CD4023A Types

CMOS NAND Gates

Quad 2 Input — CD4011A
Dual 4 Input — CD4012A
Triple 3 Input — CD4023A

The TI-CD4011A, CD4012A, and CD-4023A NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of CMOS gates.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Quiescent current specified to 15 μ A
- Maximum input leakage of 1 μ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

Characteristic	Min.	Max.	Units
Supply Voltage Range (over full package-temperature range)	3	12	V

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{STG})	—65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	—55 to +125°C
PACKAGE TYPE E	—40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	—0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_{Dh})	
FOR $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	—0.5 to $V_{DD} + 0.5$ V
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79 mm) from case for 10 s max	+265°C

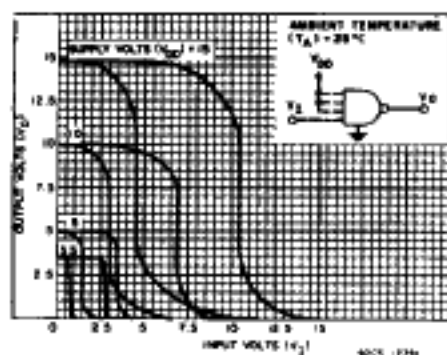


Fig. 2 — Minimum & maximum voltage transfer characteristics.

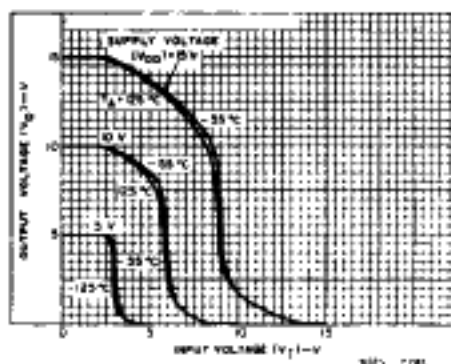


Fig. 3 — Typical voltage transfer characteristics as a function of temperature.

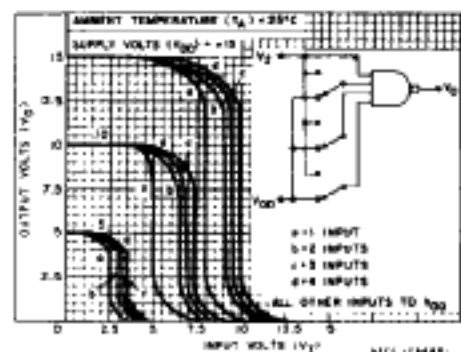


Fig. 4 — Typical multiple input switching transfer characteristics for CD4012A.

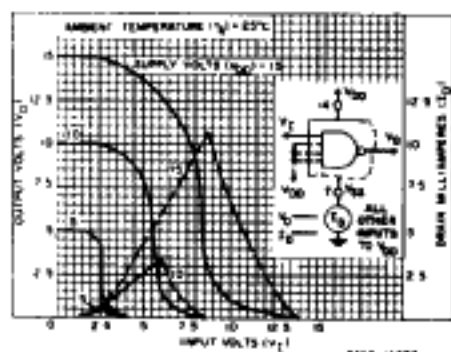


Fig. 5 — Typical current & voltage transfer characteristics.

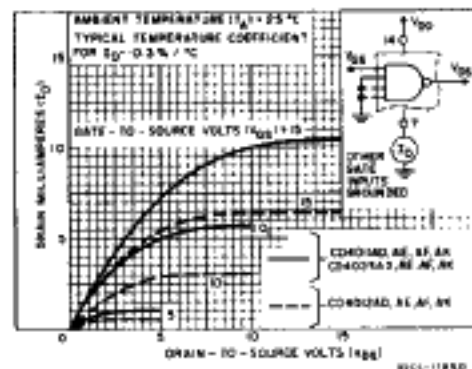
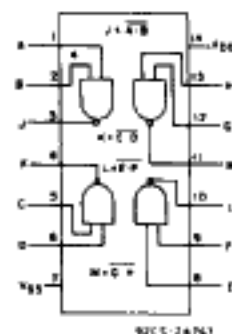
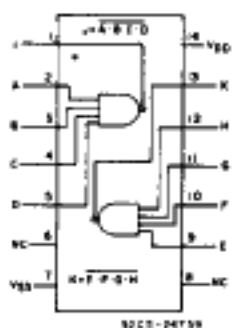


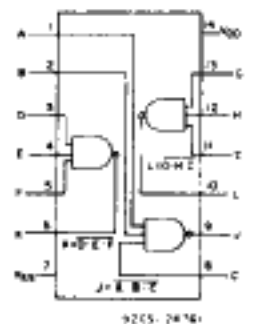
Fig. 6 — Typical n-channel drain characteristics.



CD4011A

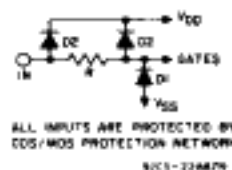


CD4012A



CD4023AH

Fig. 1 — Functional diagrams.



CD4011A

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STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	VO (V)	VIN (V)	VDD (V)	-55	+25		+125	-40	+25		+85	
Typ.					Limit	Typ.			Limit			
Quiescent Device Current, I _Q Max.	—	—	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA
	—	—	10	0.1	0.001	0.1	6	5	0.005	5	30	
	—	—	15	2	0.02	2	40	50	0.5	50	500	
Output Voltage: Low-Level VOL	—	0.5	5	0 Typ.; 0.05 Max.								V
	—	0.10	10	0 Typ.; 0.05 Max.								
High Level, VOH	—	0.5	5	4.95 Min.; 5 Typ.								V
	—	0.10	10	8.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, VNL	3.6	—	5	1.5 Min.; 2.25 Typ.								V
	7.2	—	10	3 Min.; 4.5 Typ.								
Inputs High, VNH	1.4	—	5	1.5 Min.; 2.25 Typ.								V
	2.8	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, VNML	4.5	—	5	1 Min.								V
	9	—	10	1 Min.								
Inputs High, VNMH	0.5	—	5	1 Min.								V
	1	—	10	1 Min.								
Output Drive Current: N-Channel (Sink) I _{DN} Min. CD4011A CD4023A	0.5	—	5	0.31	0.5	0.25	0.175	0.145	0.5	0.12	0.095	mA
	0.5	—	10	0.62	0.6	0.5	0.35	0.3	0.6	0.25	0.2	
CD4012A	0.5	—	5	0.15	0.25	0.12	0.085	0.072	0.25	0.06	0.05	
	0.5	—	10	0.31	0.6	0.25	0.175	0.155	0.6	0.13	0.105	
P-Channel (Source), I _{DP} Min. All Types	4.5	—	5	-0.31	-0.5	-0.25	-0.175	-0.145	-0.5	-0.12	-0.095	
	9.5	—	10	-0.75	-1.2	-0.6	-0.4	-0.35	-1.2	-0.3	-0.24	
Input Leakage Current, I _{IL} , I _{IH}	Any Input		15	±10 ⁻⁵ Typ.; ±1 Max.								μA

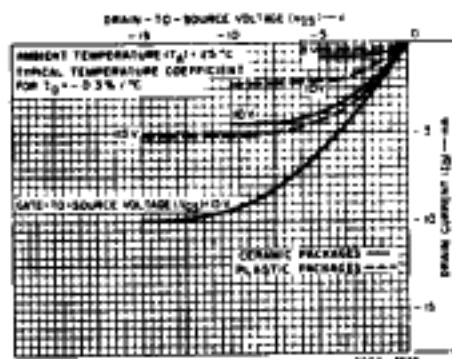


Fig. 10 — Minimum p-channel drain characteristics.

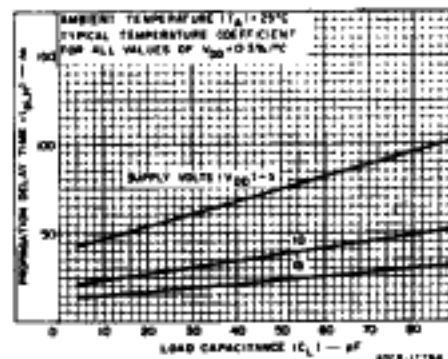


Fig. 11 — Typical low-to-high level propagation delay time vs. C_L.

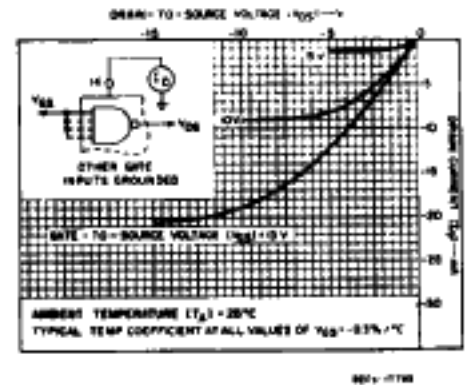


Fig. 7 — Typical p-channel drain characteristics.

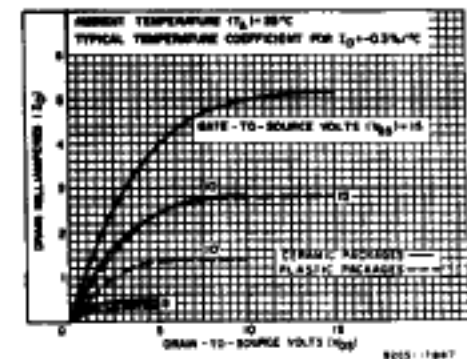


Fig. 8 — Minimum n-channel drain characteristics — CD4011A & CD4023A.

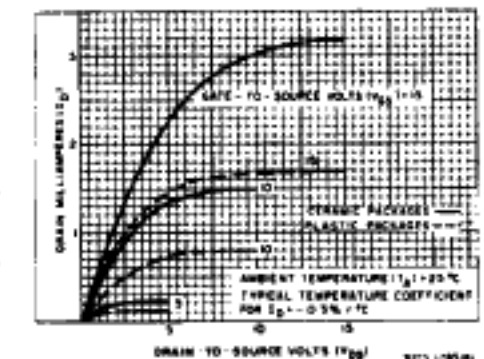


Fig. 9 — Minimum n-channel drain characteristics.

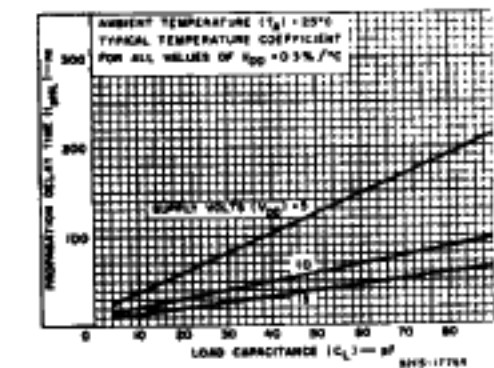


Fig. 12 — Typical high-to-low level propagation delay time vs. C_L — CD4011A, & CD4023A.

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 15\text{ pF}$, Input $t_r, t_f = 20\text{ ns}$,
 $R_L = 200\text{ k}\Omega$

CHARACTERISTICS	TEST CONDITIONS	LIMITS					UNITS
		D, F, K, H Packages			E Package		
		VDD (V)	Typ.	Max.	Typ.	Max.	
Propagation Delay Time: Low-to-High Level, t _{PLH}		5	50	75	50	100	ns
		10	25	40	25	50	
High-to-Low Level, t _{PHL} CD4011A and CD4023A		5	50	75	50	100	ns
		10	25	40	25	50	
CD4012A		5	100	150	100	200	ns
		10	50	75	50	100	
Transition Time: Low-to-High Level, t _{TLH}		5	75	100	75	125	ns
		10	40	60	40	75	
High-to-Low Level, t _{THL} CD4011A and CD4023A		5	75	125	75	150	ns
		10	50	75	50	100	
CD4012A		5	250	375	250	500	ns
		10	125	200	125	250	
Input Capacitance, C _i	Any Input		5	—	5	—	pF

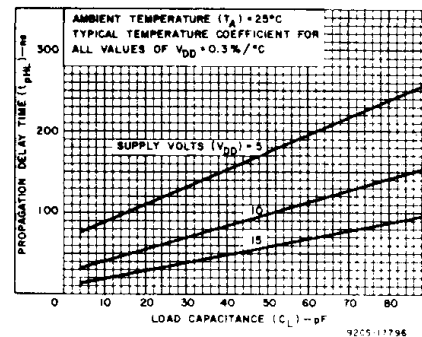


Fig. 13 — Typical high-to-low level propagation delay time vs. C_L — CD4012A.

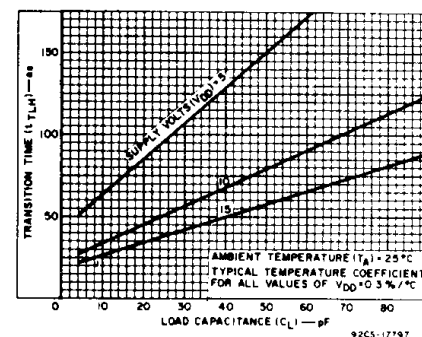


Fig. 14 — Typical low-to-high transition time vs. C_L .

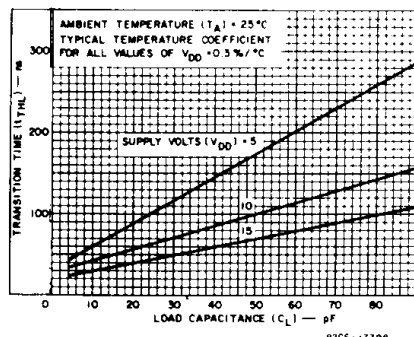


Fig. 15 — Typical high-to-low level transition time vs. C_L — CD4011A & CD4023A.

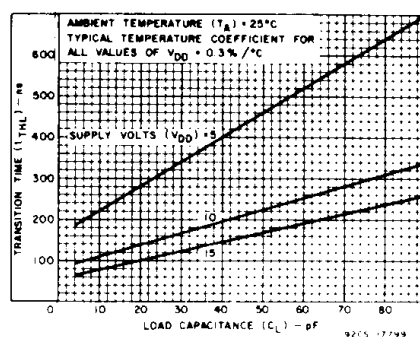


Fig. 16 — Typical high-to-low level transition time vs. C_L — CD4012A.

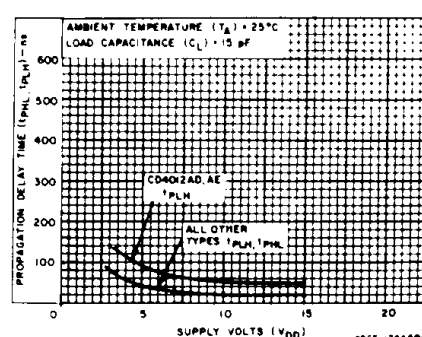


Fig. 17 — Minimum propagation delay time vs. V_{DD} .

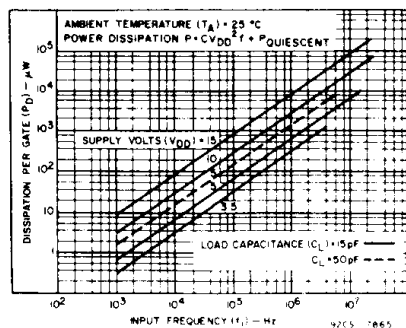


Fig. 18 — Typical dissipation characteristics.

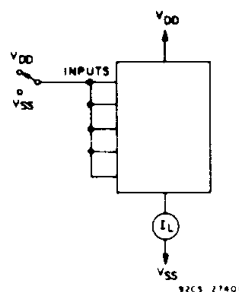


Fig. 19 — Quiescent device current test circuit.

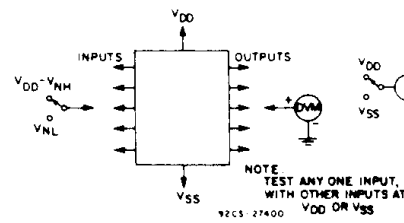


Fig. 20 — Noise immunity test circuit.

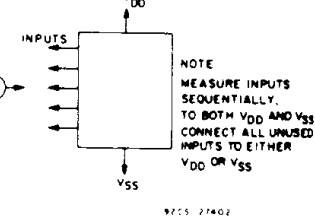


Fig. 21 — Input leakage current test circuit.

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